Code No. 3209 / S

FACULTY OF ENGINEERING

B.E. 4/4 (Civil) I-Semester (Supplementary) Examination, May / June 2017

Subject : Foundation Engineering

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1	Sketch the vertical stress distribution under a point load of 100 kN.	2
2	How do you differentiate between general and local shear failure conditions?	2
3	What is Feld's rule? What is the use of it?	2
4	Differentiate between caissons and cofferdams.	2
5	Name sampling techniques that yield undisturbed samples.	2
6	A new marks chart with 8 concentric circles and 20 radial lines was developed to find stress under an area carrying 200 kN/m^2 at a depth of 5m. Determine the vertical stress under the centre of the area if the area covered 15 parts on the chart.	3
7	Depict the effect of water table on bearing capacity. How is it accommodated in IS code method of determining bearing capacity?	3
8	A pile group has 12 piles arranged in 3 x 4 pattern. Estimate the pile group efficiency, if the diameter of the piles is 300 mm and spacing is 900 mm.	3
9	Sketch a double wall sheet pile coffer dam naming all the component parts.	3
10	Compute the area ratio of a thin walled tube sampler having an external diameter of 6cm and a wall thickness of 2.25 mm. Do you recommend the sampler for obtaining undisturbed soil samples?	3

PART – B (50 Marks)

11	a)	Differentiate between Boussinesq's and Westergaard's equations for estimating the vertical stress under a point load.	5
	b)	A rectangular area 6m x 4m carries a uniformly distributed load of 10t/m^2 at the ground surface. Estimate the vertical pressure at a depth of 6m vertically below the centre and also below the corner of the loaded area.	5
12	a)	Depict the detailed procedure to conduct a plate load test. Explain various methods of plotting load Vs penetration curves. How do you use the results obtained in estimating the bearing capacity and settlement values in field.	5
	b)	A circular footing is resting on stiff saturated clay with q_u = 250 kN/m^2. The depth of foundation is 2m. Determine the diameter of the footing if the column load is 600 kN. Assume a factor of safety of 2.5. The bulk unit weight of the soil is 20 kN/m^3.	5

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13 a) Bring out the basis for development of dynamic pile load formulae; Enumerate different dynamic pile load formulae and limitations of the same. 5

b) A group of 16 piles of 50cm diameter is arranged with a centre to centre spacing of 1.0m. The piles are 9m long and are embedded in soft clay with cohesion 30kN/m^2. Bearing resistance may be neglected. Adhesion factor is 0.6. Determine the ultimate load carrying capacity of the pile group. 5

14 a) With neat sketches explain different methods to correct tilt in well foundations. 5

b) Explain the process of sinking a well foundation in general and a pneumatic caisson in particular. 5

15 Write a detailed note on (a) circular cellular coffer dams b) Diaphragm cellular coffer dam highlighting the advantages and disadvantages of one over the other. 10

16 a) Write a note on approximate formulae for evaluating vertical stress distribution. 5

b) Explain timbering of excavations with neat sketches. 5

17 Write short notes on : 10

a) Contact pressure distribution
b) Proportioning of footings
c) Negative skin friction
d) Grip length

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Code No. 3219 / S

FACULTY OF ENGINEERING

B.E. 4/4 (EEE) I - Semester (Supplementary) Examination, May / June 2017

Subject : Electric Drives and Static Control

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1 Draw block diagram of a closed loop electric drive. 2

2 Show the circuit diagram and modified speed-torque characteristics of a dc shunt motor with reduced no-load speed. 3

3 If energy loss during starting of a 3-phase induction motor is 300 W and assuming R_1 equal to R_2, then the total energy loss during dynamic braking, plugging and speed reveral are _____ , _____ and _____ respectively. 3

4 Plot speed vs. time and torques vs. time variations of a large industrial motor during load equalization. 3

5 What are the advantages of circulating current mode of operation of dual converter over non-circulating current mode? 3

6 Draw input and output current waveforms of single phase controlled rectifier with resistive load, assuming firing angle is zero. 3

7 A 3-¤, 4-pole induction motor is fed from a 3-¤ cyclo-converter, whose ratio of output frequency to input frequency is 1/3. Assuming the supply frequency is 60 Hz. and motor operates at a constant slip speed of 20 rpm, calculate speed of the motor. 2

8 In static Krammer drive, the power flow is _____ (unidirectional / bidirectional), whereas in static Scherbious drive, the power flow is _____ (unidirectional/bidirectional). 2

9 Why BLDC motor is called brushless motor and dc motor? 2

10 List various industrial applications of synchronous motor. 2

PART – B (50 Marks)

11 a) Classify load torques based on nature of load and show their speed-torque characteristics with examples and applications. 5

b) Obtain the equilibrium points and determine their steady-state stability when motor torque and load torque are given by :

$$T_m = -1 - 2\omega_m \text{ and } T_L = -3\sqrt{\omega_m}$$ 5

12 a) How do you modify the circuit of a dc series motor to get no-load speed? Draw the speed-torque characteristic and obtain the expression for the no-load speed. 5

b) Discuss the methods to reduce the energy loss during starting. 5

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13 a) Explain how dynamic braking is performed on a dc series with neat circuit diagram and speed-torque characteristics. Derive an expression for braking torque. 5

b) A 250V, 500 rpm separately excited dc motor has an armature resistance of 0.13 Ω and takes an armature current of 60A when delivering rated torque at rated flux. If flux is maintained constant throughout, i) calculate the speed at which a braking torque equal in magnitude to full load torque, when plugging with extra resistance to limit the peak torque on changeover to 3 times the rated torque ii) What terminal voltage would be required to run the motor in reverse direction at rated torque and half rated speed? 5

14 a) Draw and explain the operation of chopper circuit arrangement with neat input and output waveforms to control the speed of a separately excited dc motor, assuming continuous armature current. 6

b) Obtain speed-torque characteristics of the above motor and comment at low chopping frequency and high chopping frequency. 4

15 a) Explain speed control of a 3-phase induction motor with ac voltage regulator and comment why range of speed control is narrow. 5

b) A 3-phase, delta connected, 6-pole, 50 Hz, 400 V, 925 rpm, squirrel cage induction motor has the following parameters : $R_1 = 0.2\Omega$, $R_2 = 0.3\Omega$, $X_1 = 0.5\Omega$, $X_2 = 0.2\ \Omega$. The motor is fed from a voltage source inverter with a constant V/f ratio from 0 to 50 Hz and constant voltage of 400 V above 50 Hz. Calculate the motor torque at 30 Hz and a slip speed of 60 rpm. 5

16 a) Explain the principle and operation of a 2-phase, 4/2 pole switched reluctance motor along with its constructional features. 8

b) What are the industrial applications of SRM? 2

17 Discuss any TWO of the following : 10

a) Separate control of 3-phase synchronous motor

b) Static Scheribius drive

c) Closed loop control of dc drive

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Code No. 3235/S

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I - Semester (Suppl.) Examination, May / June 2017

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1	How the HDLs differ from software languages?	(3)
2	What are the various data types in verilog HDL?	(2)
3	Write verilog HDL code for a transmission gate in switch level.	(3)
4	What is a Net list?	(2)
5	Draw V_{DS} vs I_D curve for nmos enhancement type MOSFET.	(3)
6	What is channel length modulation effect?	(2)
7	Draw stick diagram for CMOS inverter.	(3)
8	What is □ Cg? Give its importance.	(2)
9	Compare various adder circuits in terms of speed, area and power.	(3)
10	Neatly draw 1T DRAM cell.	(2)

PART – B (50 Marks)

11	(a) Draw and explain a typical design flow for VLSI ICs.	(8)
	(b) Explain system task with example.	(2)
12	(a) Differentiate between Task and function.	(4)
	(b) Write n-bit adder code using parameters.	(6)
13	(a) Explain the electrical properties of MOSFET.	(5)
	(b) Draw CMOS circuit for f = (a.b + c).d.	(5)
14	(a) Draw the layout for S input nor gate.	(6)
	(b) What is a super buffer? Draw the circuit.	(4)
15	(a) Draw and explain advantages of Manchester carry chain.	(5)
	(b) Draw D-Flip flop using Transmission gates.	(5)
16	(a) Explain generator loops with examples.	(5)
	(b) What are the regions of operation of CMOS inverter?	(5)
17	Write short notes on the following:	
	(a) Levels of modeling in verilog	(5)
	(b) Static RAM	(5)

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Code No. 3244 / S

FACULTY OF ENGINEERING

B.E. 4/4 (M/P/AE) I – Semester (Suppl.) Examination, May / June 2017

Subject: Metrology and Instrumentation

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A and any five questions from Part – B.

PART – A (25 Marks)

1 Classify various types of fits with neat sketch.

2 Explain the use of precision polygon with neat sketch.

3 Define the terms straightness and flatness with geometric features.

4 Sketch different chart gauges.

5 Explain the concept of best size wire in thread measurement, show by sketch.

6 List the instruments used in machine tool testing.

7 Distinguish between precision and accuracy with sketch.

8 Sketch Piezo electric load cell.

9 Explain the Bourdon tube pressure principle working with a sketch.

10 Explain the use of extension wires in thermo couples.

PART – B (5x10 = 50 Marks)

11 a) What are limit gauges? Sketch and explain any two types of limit gauges.
b) Explain the autocollimator with neat sketch and give its advantages.

12 a) Describe the working of sigma comparator with a neat sketch.
b) Explain the tool maker's microscope applications with a neat sketch.

13 a) Explain the schematic layout of Talysurf instrument.
b) Explain how gear tooth thickness is measured using gear tooth vernier callipers.

14 a) Explain the various dynamic characteristics of measuring instruments.
b) Explain the principle of operation of LVDT with its advantages.

15 a) Explain with a neat sketch the working principle of Pinani gauge.
b) Explain the various types of materials used in thermo couples.

16 a) Distinguish between hole basis system and Shaft basis system with neat sketch. .
b) Explain any five geometric tests conducted on lathe machine testing.

17 Write short notes on the following:
a) Rosette gauges with neat sketch
b) Seismic accelerometer with neat sketch.

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Code No. 3269/S

FACULTY OF ENGINEERING

B.E. 4/4 (CSE) I - Semester (Suppl.) Examination, May / June 2017

Subject : Artificial Intelligence

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1 Briefly explain iterative deepening search and its advantages. (3)

2 Consider a state space where start state is numbered as 1 and the successor function for state numbered as 'n' returns two states numbered as 2n and 2n+1. Suppose the goal state is 13. Draws search tree and list the order in which nodes will be visited using following searches. (3)
(a) Breadth First search
(b) Depth First search

3 Obtain wff representation of the statement.
Any person who has an umbrella is not wet. (2)

4 Differentiate between supervised and unsupervised learning. (2)

5 How is common sense knowledge represented? (2)

6 What is situation calculus? (2)

7 What is a fuzzy set? (2)

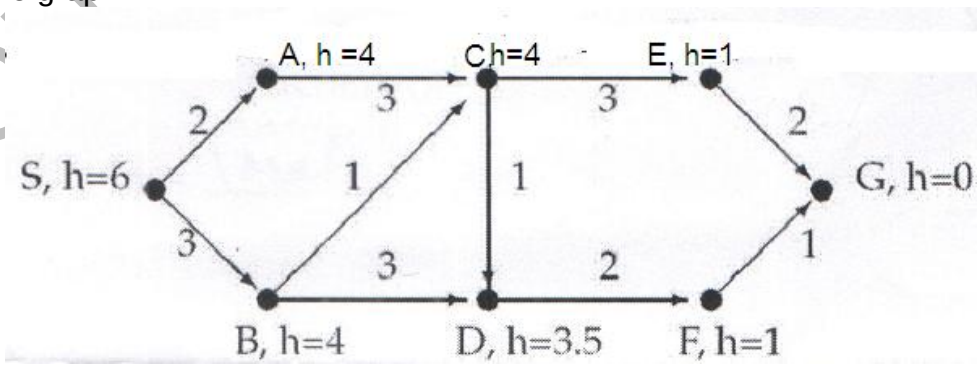
8 What is Sussman anomaly? (3)

9 List the applications of Neural networks. (3)

10 Describe briefly about expert systems. (3)

PART – B (50 Marks)

11 (a) Explain about adversarial search with an example. (5)
(b) The graph below represents the search space of a problem. Nodes are labeled with a letter and the value of a heuristic function h for the node. Edge are labeled with the cost of traversing the edge. Simulate running the A* algorithm on the graph. (5)



12 (a) Explain resolution procedure in predicate calculus. (6)
(b) Explain rules of inference in propositional calculus. (4)

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13 What is Bayes network and explain how probabilistic inference is done using it? (10)

14 (a) Explain learning in decision tree using information theory. (5)
(b) Determine the weights of the following Perception network after one iteration. (5)

- 3 inputs and 1 output
- Input : [110] [100] [001] output : [1] [1] [0]
- linear threshold activation function with threshold – 0.7
  (Output = 1 if it exceeds threshold, otherwise 0)
- Initial weight WI = 0.2 W2 = 0.4 W3 = 0.9
- Assume a learning rate of 0.2

15 What is parsing? Explain top down and bottom up parsing. Generate a parse tree for the sentence: John ate the apple. (10)

16 (a) Prove the following using resolution refutation method. (4)
(i) $\{A \wedge B, \sim A \vee C\} = B \vee C$
(ii) $\{A . B \rightarrow C. A \rightarrow C \} = A \wedge C$
(iii) $\{A \rightarrow B \wedge C. A\} = C$
(iv) $\{A \vee C, \sim B \vee \sim C\} = A \vee \sim B$
(v) $\{A \vee C, B \vee \sim C, \sim B, A \vee S, \sim U\} = \sim U \wedge S$
(b) Explain briefly the general model of learning agents, enumerate and represent the components of the performance element. (6)

17 Write short notes on the following:
(a) Recursive STRIPS (5)
(b) Back propagation in multilayer feed forward neural network (5)

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Code No. 3279/S

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I - Semester (Suppl.) Examination, May/June 2017

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1	What is Moore's law?	(2)
2	What are the different types of capacitance present in MOS transistor?	(3)
3	Draw layout of CMOS inverter and identify all the layer names.	(3)
4	Differentiate between structural modeling and switch level modeling.	(2)
5	What are lambda based design rules? Why should we follow them?	(2)
6	What are the advantages of SRAM over DRAM?	(2)
7	How delay is reduced by cascading the inverters?	(3)
8	How do you measure the sheet resistance in the MOS transistor?	(3)
9	Explain the write operation in IT DRAM cell.	(3)
10	What is the difference between simulation and synthesis?	(2)

PART – B (50 Marks)

11	(a) Explain the operation of NMOS transistor and derive its current equation in linear region.	(7)
	(b) Explain the effect of threshold voltage on body effect.	(3)
12	(a) Draw the layout of two input NOR gate.	(5)
	(b) Define active contact, poly contact and metal contact.	(5)
13	Design the following using Transmission gate logic.	
	(a) Full adder	(5)
	(b) 8XI multiplexer	(5)
14	(a) With the help of a neat sketch, explain the CMOS process flow.	(5)
	(b) Draw the layout of the function $Y = \overline{A+B}$.	(5)
15	(a) Implement a NOR based ROM memory cell.	(4)
	(b) Explain read and write operation of 6T SRAM cell.	(6)
16	(a) What is interconnect? Derive the delay modeling of an interconnect.	(5)
	(b) What is meant by crosstalk? Explain the different techniques to optimize the cross talk.	(5)
17	Write short notes on the following:	
	(a) Differential cascade voltage switch logic (CVSL)	(4)
	(b) Pre-charge sharing	(3)
	(c) Evaluation charge sharing	(3)

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