Code No. 237

FACULTY OF ENGINEERING

B.E. 4/4 (Civil) I - Semester (Main & Backlog) Examination, December 2017

Subject: Foundation Engineering

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1 "Boussinesq's theory of stress distribution is applicable for stratified soils". Answer yes or no and justify your answer. (2)

2 The ultimate bearing capacity of a footing laid on cohesion less (c=0) soil at ground level was found to be 200 kPa. All other parameters remaining same, compute q_f if size is doubled. (2)

3 What are "Batter Piles"? When they are preferred? (2)

4 "Coffer Dams are permanent structures constructed for irrigation purposes". Answer yes or no and justify. (2)

5 "The trial pit method of geotechnical investigations are ideal if the depth of investigation is more than 20 m". Answer yes or no and justify your answer. (2)

6 Define "Pressure Bulb". Determine the depth to which a 10 kPa pressure bulb extend beneath the point load of 100 kN applied on the surface. (3)

7 In a plate load test conducted at a site using 300 mm size square plate was recorded as 800 kg. Determine the ultimate bearing capacity of a 1.50 m size square footing to be laid at the same depth in this site. (3)

8 The load carrying capacity of a 300 mm diameter end bearing pile is 200 kN. All other parameters remaining same, what should be the increase in diameter required to double the capacity. (3)

9 Describe "Tilt and Shift" of Caissons during their installation. State the provisions of IS code related to the limits prescribed, beyond which correction for "Tilt and Shift" of Caisson is required. (3)

10 What is "under pinning"? Explain its necessity. (3)

PART – B (50 Marks)

11 (a) From fundamentals, derive the expression for increment in vertical stress beneath centre of a uniformly loaded circular area of diameter "2a" with a UDL of intensity "q" adopting Boussinesque's theory. (5)

(b) A over head service reservoir is provided with a ring type of foundation with outer diameter of 10m and inner diameter of 6m transmitting a uniformly distributed load of 4000 kN/sqm. Determine the increment in vertical stress at a point lying 0.50m beneath the center of ring foundation. (5)

….2.

12 (a) Explain the types of shear failure experienced by shallow foundations. Mention the parameters to decide the type of shear failure. (5)

(b) A SPT was conducted at a depth of 3m below the GL. The observations were recorded as 14/18/24. The correction for a over burden was read as 1. Apply correction for dilatancy. If a 2 m wide square footing is proposed at this level, estimate the allowable bearing pressure for a permissible settlement of 40mm based on the penetration resistance (N" value) as per IS : 6403 – 1981. (5)

13 (a) A group of 20 piles, arranged in 4x5 pattern are provided in a Clay deposit to a depth of 12m. The size of each pile is 600mm dia provided at a c/c spacing of 1.80m. The average properties of the clay are qu = 160 kPa, adhesion factor is 0.58. Determine the safe load carrying capacity of the pile group. Adopt FS = 2.50. (5)

(b) Write a detailed note on the "Pile Load Tests". (5)

14 (a) Describe the procedure of sinking of a "Pneumatic Caisson" in detail, with the help of neatly drawn sketches. (5)

(b) Describe various methods of soil stabilization including merits and demerits of each. (5)

15 (a) Write a note on methods of dewatering adopted in construction of foundations. (5)

(b) Critically compare "Earthen Cofferdam" with "Cellular Cofferdams". Support your answer with neatly drawn sketches. (5)

16 (a) Explain various methods of "Timbered Excavations" with the help of neat sketches. (5)

(b) Write a detailed note on methods of "Geotechnical Investigations" including the procedure involved, merits, demerits and suitability. (5)

17 Write short notes on any **two** of the following: (5x2=10)

(a) Proportioning of footings

(b) Negative skin friction

(c) Plate load test and its limitations

(d) Requirements of design of machine foundations

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Code No. 247

FACULTY OF ENGINEERING

B.E. 4/4 (EEE) I - Semester (Main & BL) Examination, December 2017

Subject: Electric Drives and static Control

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part A and any five questions from Part B.

PART-A (25 Marks)

1. Draw speed-torque characteristics of dc shunt motor in third and fourth quadrants with and without external resistance connected to armature. (3)
2. What is the difference between active load and passive load? Give examples. (3)
3. Derive an expression for energy loss during starting of a dc shunt motor at no-load. (3)
4. Why a 3-phase induction motor draws high current at the instant of counter current braking? (2)
5. What are the advantages of semi-converter fed dc motor over full-converter fed motor? (2)
6. A 220 V, 800 rpm, 150 A separately excited dc motor has an armature resistance of 0.06 Ω. It is fed from a single phase fully controlled rectifier with an ac source voltage of 220 V, 50 Hz. Assuming continuous conduction, calculate firing angle for rated torque at 600 rpm. (3)
7. A 3-phase, 50 Hz, 1440 rpm induction motor is fed from a 3-phase cyclo-converter. Calculate its speed at same slip, when frequency output of cyclo-converter is 12.5 Hz. (3)
8. Draw speed-torque characteristics of 3-phase induction motor fed from a 3-phase ac voltage controller for any two firing angles. (2)
9. As load torque on a BLDC motor increases, then its supply frequency _____ (increases / decreases / remain constant) and its speed _____ (increases / decreases / remain constant). (2)
10. What are the industrial applications of switched reluctance motor? (2)

PART - B (50 Marks)

11 a) What is load equalization? Derive an expression for moment inertia of a flywheel. (6)

b) A 150 HP, 800 rpm dc shunt motor has stored energy of 5000 Joules per HP. Determine the time taken to start the motor, if the load torque is equal to full load torque and the current is limited to two and half times the full load current during starting. (4)

12 a) Explain any one scheme of dc dynamic braking of 3-phase induction motor. (6)

b) Draw speed-torque characteristics of any four types of loads along with examples. (4)

13 a) Draw and explain the operation of single-phase semi converter fed separately excited dc motor with a neat circuit diagram and show input and output voltages and currents, assuming continuous load current. (6)

b) Explain briefly how energy loss can be minimized during starting of a motor. (4)

14 a) Draw and explain briefly speed-torque characteristics of 3-phase induction motor operating in reverse motoring for (i) dc dynamic braking and (ii) regenerative braking. (5)

b) A 3-phase, 440 V, 50 Hz, 10 kW, 960 rpm, 6 pole, star connected slip-ring induction motor has the following constants per phase : $R_1 = 0.4\ \Omega$, $R_2' = 0.6\ \Omega$, $X_2 = X_2' = 1.4\ \Omega$. The load torque is proportional to speed at rated speed and the motor is controlled by static rotor resistance control. The stator to rotor turns ratio is 2. Calculate the value of external resistance so that motor runs at 800 rpm for duty ratio of 0.5. (5)

15 a) Draw and explain non-circulating current mode of operation a dual converter fed dc drive. (5)

b) With neat schematic circuit diagram, explain speed control of 3-phase induction motor in both forward motoring and reverse motoring using 3-phase ac voltage controller. (5)

16 a) Draw and explain briefly any two configurations of variable voltage and variable frequency control of synchronous motor using dc link converter with a neat block diagrams. (5)

b) What is the principle of switched reluctance motor? Explain the same for a 4 phase, 4/2pole motor with a neat schematic diagram. (5)

17 Discuss the following: (10)

a) Static Scherbius drive

b) Modified speed-torque characteristics of dc shunt motor with shunted armature.

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Code No: 263

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I-Semester (Main & BL) Examination, December 2017

Subject: VLSI Design

Time: 3 Hours **Max. Marks: 75**

***Note:** Answer All Questions From Part–A. Answer any FIVE Questions From Part-B*

PART – A (25 Marks)

1) What are system tasks and compiler directives in Verilog? [3]
2) Describe looping statements. [3]
3) What is Lambda based design rules? [2]
4) Draw the stick diagram of CMOS 2 input XOR gate. [2]
5) Give the circuit diagram of inverting and non-inverting super buffers. [3]
6) Draw the schematic diagram of D-flip flop using Transmission gates. [3]
7) What is the difference between a gate instantiation and module instantiation? [2]
8) Explain procedure and function declarations in Verilog. [2]
9) Explain 1 transistor DRAM cell. [2]
10) Write the expressions for rise time, fall time, propagation delay [3]

PART – B (5x10=50 Marks)

11) (a) Describe three ways of specifying delays in continuous assignment statements.

(b) Design a 4-bit Full Adder using Gate level and data flow techniques. [4+6]

12) (a) Explain Delay back annotation Space with diagram.

(b) What is Logic Synthesis? Describe Synthesis design from RTL to Gates. [3+7]

13) (a) How a MOS transistor behaves in enhancement and depletion modes? Explain with help of n-channel MOS V-I characteristics.

(b) Derive the expression for pull up to pull down ratio of an NMOS inverter driven by another NMOS inverter. [5+5]

14) (a) Draw and explain sheet Resistance (Rs)? Give one example of delay calculation model with a neat sketch?

(b) Draw the stick diagrams and layouts of transmission gate and 3 input NAND gate. [5+5]

15) (a) With help of circuit diagram, explain 4-bit barrel shifter.

(b) What is carry skip adder? Give one example. [5+5]

16) (a) Design 8-bit NAND based ROM memory cell and explain its operation.

(b) Draw and explain 1T dynamic RAM read and write operation. [5+5]

17) (a) Write a Verilog program for Ripple counter using T-Flip-flops.

(b) Write a Verilog program for 4-bit adder in behavioural level modelling. Write test bench and draw the input-output waveforms. [5+5]

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Code No. 272

FACULTY OF ENGINEERING

B.E. 4/4 (M/P/AE) I - Semester (Main) Examination, December 2017

Subject: Metrology and Instrumentation

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1 Explain the terms: (i) Lower deviation and (ii) Upper deviation in size determination of a component.

2 What are the applications of slip gauges in industry?

3 What is unilateral and bilateral tolerance? Give a numerical example.

4 What are the advantages of differential pneumatic comparator?

5 What are different Rosette strain gauge arrangement for displacement measurement?

6 Explain the working principle of piezoelectric load cell.

7 Explain super gear features with a sketch for measurement.

8 What are the types of materials used in thermocouples?

9 Explain the term sensitivity of measuring instruments with help of neat diagrams.

10 Distinguish between tolerance and allowance.

PART – B (50 Marks)

11 (a) How are the angular measurements made? Describe the instrument for angular measurement exactly up to a seconds.

(b) Explain the working of tool makers microscope with a neat sketch and its applications.

12 (a) Explain how a precision level can be used to determine the flatness and straightness of machine tool-work table with help of a new diagram?

(b) Explain the working of soundness measuring machine with neat sketch.

13 (a) Derive an expression for best size wire in screw thread.

(b) What are the two corrections applied in the measurement of effective diameter by the method of wires?

14 (a) Discuss the classification of errors in instrumentation systems.

(b) Explain the applications wire and foil type resistance strain gauges with neat sketches.

15 (a) Explain the working of a pirani gauge with a neat sketch to measure pressure.

(b) Explain the problem in bonding of spin gauges while measuring displace.

16 (a) List the instruments used for pressure measurement and explain working principle of bourdon pressure gauge with a neat sketch.

(b) Explain the working principle of LVDT intolerance measurement of component.

17 Explain the following:

(a) Sine bar and its limitations

(b) Gear measurement procedure with a neat diagram

(c) Load cells

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Code No. 297

FACULTY OF ENGINEERING

B.E. 4/4 (CSE) I – Semester (Main & Backlog) Examination, December 2017

Subject: Artificial Intelligence

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A and any five questions from Part B.

PART – A (25 Marks)

1 What is constraint graph? (2M)

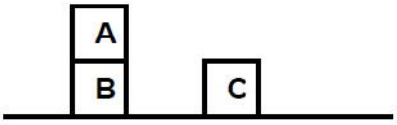
2 Briefly explain iterative deepening search and its advantages. (3M)

3 Obtain wff representation of the statement: (3M)

Any student who does not study does not pass

4 Differentiate between supervised and unsupervised learning (2M)

5 What is fluent? Write the fluents for the following state of blocks. (3M)



6 What is Sussman anamoly? (3M)

7 List the applications of Neural networks. (2M)

8 Describe briefly about expert systems. (3M)

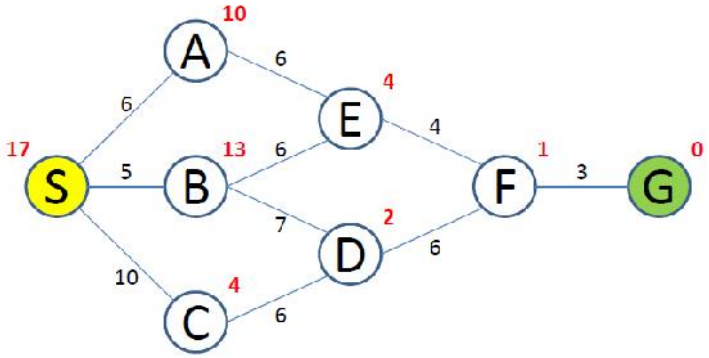
9 What is a fuzzy set. (2M)

10 What is skolemization. Give an example. (2M)

PART – B (5x10 = 50 Marks)

11 a) Explain about alpha beta pruning of adversarial search with an example. (5M)

b) The graph below represents the search space of a problem. Nodes are labeled with a letter and the value of a heuristic function h for the node. Edges are labeled with the cost of traversing the edge. Simulate running the A* algorithm on the graph. (5M)

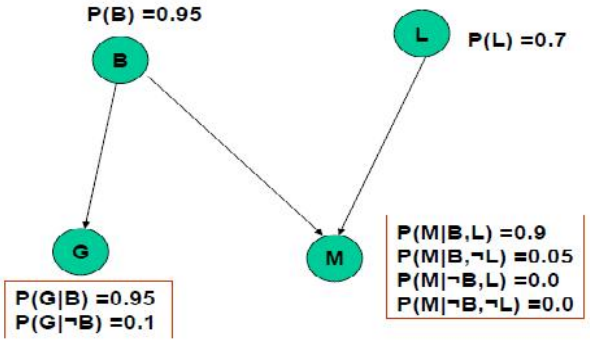


12 a) Explain resolution procedure in predicate calculus. (6M)

b) How is common sense knowledge represented? (4M)

13 a) What is STRIPS planning system? Explain different lists used in defining the operators in STRIPS. (4M)

b) Compute
i) p(B,L,M,G)
ii) p(L/B)
iii) p(M/~L) (6M)



14 Discuss briefly about the applications of Neural Networks. Describe the architecture and learning rule of Perceptron. (10M)

15 What is Natural Language Processing. Explain the various phases/steps in NLP. (10M)

16 Write short notes on
a) Recursive STRIPS (5M)
b) Backpropogation in multilayer feed forward neural network (5M)

17 a) Explain briefly about Fuzzy Inferencing. (5M)
b) Compute Information Gain of Outlook, Humidity for the given data (5M)

Outlook	Humidity	Play Tennis (class label)
Sunny	High	No
Sunny	High	Yes
Overcast	High	Yes
Rain	High	Yes
Rain	Normal	No
Overcast	Normal	Yes
Sunny	Normal	No
Sunny	High	Yes
Overcast	Normal	Yes
Overcast	Normal	No

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Code No. 307

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I-Semester (Main) Examination, December 2017

Subject: VLSI Design

Time: 3 hours **Max. Marks: 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1	What is meant by scaling? How is it related to MOS transistor?	2
2	How does threshold voltage vary with the channel length and rain to source voltage?	3
3	What are the layers used to create a MOSFET?	3
4	What are the electrical properties of MOD transistor?	2
5	What is data flow modeling? Give one example.	2
6	Define rise time, fall time and delay time.	2
7	What are the advantages of dynamic logic over static logic?	3
8	How do you calculate the delay of logic gate?	3
9	Implement XOR logic gate using CMOS logic.	3
10	Discuss the need for testing.	2

PART – B (50 Marks)

11	a)	What are different types of capacitances present in MOS transistor? Explain their variations with applied potentials.	7
	b)	Explain the MOSFET as switch.	3
12		Draw the layout of the function using CMOS logic.	
	a)	$Y = \overline{A + BC}$	5
	b)	$Y = \left(\overline{A + B}\right)(C + D)$	5
13	a)	Explain the CMOS inverter switching characteristics and derive the delay expression.	5
	b)	Explain the effect of charge storage on the floating gate.	5
14	a)	Draw the block diagram of differential cascade voltages switch logic. Design a two input XOR and XNOR logic gate using above model.	6
	b)	Implement two input AND and NAND gates using complementary pass transistor logic.	4
15	a)	Write a verilog code for 4-bit ripple carry adder using data flow modeling.	5
	b)	Implement 2X1 multiplexer using TG logic. Give its truth table.	5
16	a)	Design a 4-bit barrel shifter.	4
	b)	How to model the interconnect in physical model to circuit level model? Explain in detail.	6
17		Write a short notes on:	
	a)	Complementary Pass Transistor Logic	4
	b)	High speed adders	3
	c)	Priority encoder	3

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