Code No. 463/CBCS

FACULTY OF ENGINEERING

B.E. (Civil) IV - Semester (CBCS) (Main) Examination, May/June 2018

Subject : Fluid Mechanics - II

Time : 3 Hours **Max. Marks: 70**

Note: Answer all questions from Part-A & any five questions from Part-B.

PART – A (20 Marks)

1 Write the significance of Reynolds number. 2

2 Find the diameter of a single pipe of length 1500m to replace three pipes of length 600m, 500m and 300m and diameters 300mm, 200mm and 100mm. 2

3 Explain the terms hydraulic gradient line and total energy line. 2

4 Define water hammer phenomenon. 2

5 Differentiate between friction drag and pressure drag. 2

6 Define laminar sublayer. 2

7 Define specific energy and critical depth. 2

8 State the Froude number values for critical, subcritical and supercritical states of flow. 2

9 List the different surface profiles. 2

10 If a hydraulic jump occurs at a point where the upstream depth is 0.25m, what would be the depth after the hydraulic jump, if the discharge per unit width q=0.625 m^3/s per metre width. 2

PART - B (50 Marks)

11 (a) Derive Hagen Poisuille's equation for laminar flow through circular pipes. 5

(b) A pipe 200mm in diameter and 45m long conveys water at a velocity of 2.5 m/s. Find the head lost in friction. Take f= 0.006. 5

12 (a) Explain different types of pipes, based on pipe materials. 5

(b) Water flowing in a long pipe of diameter 150mm and thickness 6mm is suddenly stopped by closing the valve at the discharge end. The quantity of water flowing is 18 litres/sec. Find the rise in pressure, taking the modulus of elasticity of pipe material as 1.962×10^5 N/mm^2 and bulk modulus of water as 1.962×10^3 N/mm^2. 5

13 (a) Explain the drag on a flat plate, held perpendicular to the direction of flow of fluid. 5

(b) If the velocity distribution in the boundary layer is given by $\frac{u}{U} = \frac{y}{¢}$, determine the displacement thickness, momentum thickness and energy thickness. 5

14 (a) Derive Chezy's equation for uniform flow. 5

(b) A channel of trapezoidal section has sides sloping at 60^0 with the horizontal and a bed slope of 1 in 800 and conveys a discharge of $12 m^3/s$. Find the bottom width and depth of flow for most economical section. Take Chezy's constant C=70. 5

..2

15 (a) Explain specific energy diagram and determine the expression for critical depth. 5

(b) A rectangular channel 7.5m wide has a uniform depth of flow of 2m and has a bed slope of 1 in 3000. If due to weir constructed at the downstream end of the channel, water surface at a section is raised by 0.75m, determine the water surface slope with respect to the horizontal at this section. Take n=0.02. 5

16 (a) Derive an expression for the celerity of a positive surge. 5

(b) Calculate the total drag, shear drag and pressure drag exerted on 1m length of an infinite circular cylinder which has a diameter equal to 30mm, air of density 1.236 Kg/m^3 flowing past the cylinder with velocity 3.6 m/min. Take total drag coefficient equal to 1.4 and shear drag coefficient equal to 0.185. 5

17 Write short notes on 10

(i) Momentum thickness

(ii) Separation of Boundary layer.

(iii) Hydraulic jump.

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CODE NO: 473/CBCS

FACULTY OF ENGINEERING

B E IV-Semester (CBCS) (EE/Inst.) (Main) Examination, May / June 2018

Subject: Linear Integrated Circuits

TIME: 3 Hours **Max. Marks: 70**

Note: Answer All Questions From Part-A & Any Five Questions From Part-B

PART-A (20 MARKS)

1. Write the comparison of ideal and practical characteristics of an Op-Amp. (2)
2. Why the offset balancing techniques are required for an Op-Amp? Explain. (2)
3. What is Schmitt trigger? Mention few applications of the same. (2)
4. Draw the circuit diagrams of multiplier and divider. (2)
5. What are the Barkhausen's criterion for oscillations? (2)
6. Draw the functional diagram of a 555 timer. (2)
7. Define the terms with respect to voltage regulators.
   (i) Line regulation (ii) Load regulation (iii) Ripple rejection (2)
8. Why current sensing protection is required for the voltage regulator. (2)
9. Write the important parameters of a filter. (2)
10. Write the features of Monolithic power amplifier. (2)

PART-B (50 MARKS)

11. (a) Explain the following parameters of an Op-Amp.
    (i) input offset voltage (ii) input offset current (iii) power supply rejection ratio
    (iv) output voltage swing (v) common mode rejection ratio (5)
    (b) Derive the voltage gain equation for an inverting and non inverting modes of Op-Amp. (5)

12. (a) Explain the operation of inverting Schmitt trigger circuit. (5)
    (b) Explain any two applications of comparator in detail. (5)

13. (a) Explain the working of 555 timer as a monostable multivibrator. (5)
    (b) Explain the operation of voltage to frequency converter. Derive the necessary equations. (5)

14. (a) Explain the working of switching voltage regulator with a neat block diagram. (5)
    (b) Explain the current fold back feature of voltage regulator. (5)

15. Explain the operation of state variable filter. Derive the transfer functions for any two filters available in it. (10)

16. (a) Explain the frequency response of Op-Amp by drawing its high frequency model. (5)
    (b) Explain the operation of precision full wave rectifier circuit with neat diagram. (5)

17. Write short notes on
    (a) Power amplifiers. (5)
    (b) Buck-Boost voltage regulator. (5)

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FACULTY OF ENGINEERING

B.E. (ECE) IV – Semester (CBCS) (Main) Examination, May / June 2018

Subject: Pulse, Digital & Integrated Circuits

Time: 3 Hours **Max.Marks: 70**

Note: Answer all questions from Part – A & any five questions from Part – B.

PART – A (10x2 = 20 Marks)

1 Sketch the step response of a High Pass RC circuit.

2 Match the following

a) Attenuator	1. Requires diodes, resistors and capacitors
b) Differentiator	2. Requires diodes and resistors only
c) Clipper	3. Reduces the amplitude of the signal
d) Clamper	4. Low pass RC
	5. High pass RC

3 Compare the performance of series clipper with shunt clipper.

4 With reference to a binary circuit, explain the role of the commutating capacitors.

5 What is hysteresis in a Schmitt Trigger Circuit?

6 Define Fan-out of a logic Gate. What factors determine the Fan-out of a logic Gate?

7 Draw 2 input CMOS NOR gate and write its truth table.

8 Why are MOS ICs especially sensitive to static charge, list its precautions?

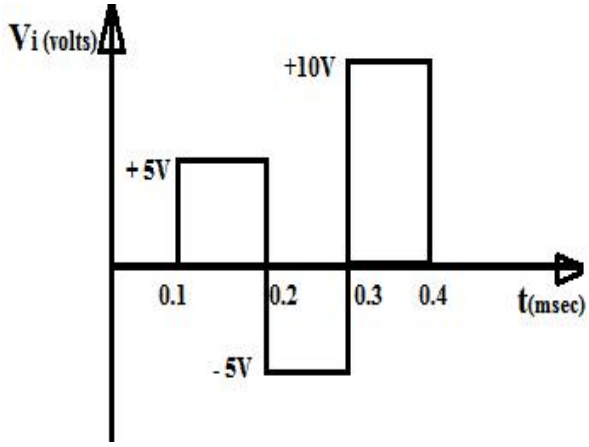
9 Totem pole outputs should not be tied together. Why?

10 What is current sinking and sourcing action in TTL Gate? Show with illustrative diagrams.

PART – B (50 Marks)

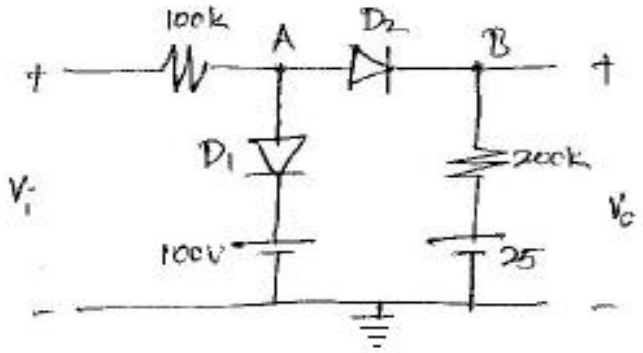
11 a) Show that for any periodic input waveform, the average level of steady state output waveform of RC High Pass circuit is always zero independent of the DC level of the input. 5

b) Assuming the capacitor to be initially uncharged, determine the response of RC Low Pass circuit with a time constant, τ = 0.05 msecs, for the given input waveform in the figure below. 5



12 a) State and Prove the Clamping theorem. 5

b) For the given two level clipper circuit, the input varies linearly from 0V to 150V. Sketch the transfer characteristics to the scale indicating the slopes. 5



13 a) Draw the circuit diagram of a collector coupled astable multi-vibrator and explain it's operation with relevant waveforms at the bases and collectors. Derive the expression for frequency of oscillation. 7

b) In the above collector coupled astable multi-vibrator, find the period of output and the frequency of oscillation if R1 = R2 = 25KΩ and C1 = C2 = 0.2 μ F 3

14 a) Draw and Explain the operation of a 2 input TTL NAND gate using Totem-pole output, for Low output state and High output state with suitable circuit diagrams. State the advantages of totem-pole output circuit. 7

b) A TTL gate is guaranteed to sink 10 mA current with out exceeding an output voltage V_{OL} = 0.4V and to source 1mA current with out dropping below V_{OH} = 2.4V. If I_{IH}= 100uA at 2.4V and I_{IL} = 0.5mA at 0.4V, Calculate the 0 state and 1 state fan out. 3

15 a) How do you interface a TTL gate to a high voltage CMOS gate? Illustrate when each is driving the other. 5

b) What is meant by open-collecter output of TTL gate? What is its utility? Draw and explain the circuit diagram of open-collector output TTL gate. 5

16 a) In a series RLC circuit obtain the transfer function and sketch it's voltage response to a step input. 5

b) Define the three types of errors that occur in time base generators. 5

17 Write short notes on: 10

a) CMOS transmission gate
b) Compensated attenuator.
c) UJT

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Code No: 483/CBCS

FACULTY OF ENGINEERING

BE IV - Semester (CBCS)(M/P) (Main) Examination, MAY /June 2018

Subject : Basic Electronics

Time: 3 Hours **Max Marks: 70**

Note: Answer all questions from Part-A & Any five questions From Part-B.

Part - A (20 Marks)

1. What do you mean by drift velocity in a semiconductor? 2
2. What is the use of filter circuits in power supply? 2
3. Why the width of the base region of a transistor is kept very small compared to other regions? 2
4. For an N- Channel JFET I_{DSS} = 8.7 mA, V_p=-3V and V_{GS} =- IV. Calculate I_D. 2
5. An amplifier has open loop gain of 1000, f1 = 50 Hz and f2 = 200 KHZ, β = 0.01
   Find f_{1f}, f_{2f} when negative feedback is applied. 2
6. Determine the frequency of an Hartley oscillator if L1 = 100 μH, L2 = 1mH and C = 20pF 2
7. List the ideal characteristics of an OP – AMP 2
8. Give the symbols of Basic gates and their truth tables 2
9. Give the symbols of LED, SCR and UJT 2
10. Mention applications of CRO 2

PART – B (50 Marks)

11. a) Explain the formation of depletion layer in a pn junction diode. 5
    b) Explain the working of a Zener voltage regulator 5

12. With the help of characteristic curves explain the operation of JFET 10

13. a) Classify negative feedback amplifiers and explain them. 8
    b) State Barkhausen criterion for oscillations 2
14. a) Draw the equivalent circuit of an OP-AMO & explain 4
    b) Realize Basic logic gates using NAND gates only 6

15. a) Explain the working of thermistor for temperature measurement 6
    b) Draw the block diagram of CRO 4
16. a) Explain the operation of center tapped FWR 5
    b) Explain the OP-AMP based summer circuit 5
17. Write short notes on (i) transistor CE Configuration (ii) LCD (5+5)

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Code No. 489 / CBCS

FACULTY OF ENGINEERING

B.E. (A.E) IV – Semester (CBCS) (Main) Examination, May / June 2018

Subject: Automotive Chassis Components

Time: 3 Hours **Max.Marks: 70**

Note: Answer all questions from Part – A & any five questions from Part – B.

PART – A (10x2 = 20 Marks)

1 Explain the term frame of an automobile.
2 List out the types of cross section used for frames.
3 Define drive line.
4 Draw the layouts of differential housings.
5 List out the types of stub axle with neat sketches.
6 Draw a steering linkage layout for integral chassis frame.
7 Explain the need of suspension system.
8 Differentiate between independent and dependent type of suspension system.
9 State the category for classification of brakes.
10 Sketch shoe and trailing shoe.

PART – B (5x10 = 50 Marks)

11 Explain the types of chassis layout with reference to number of wheels, frame, body and drive.

12 Explain briefly front wheel geometry with a neat diagram.

13 a) Explain briefly Hotchkiss drive.
b) Explain the drive system for two wheeler vehicle (Pulsar).

14 a) Explain with sketch suspension system for bus (HMV).
b) Explain with neat sketch of shock absorber.

15 a) Explain briefly air brakes for bus with sketch.
b) Draw and explain a layout for hydraulic braking system.

16 a) Explain power brakes for (LMV) vehicles.
b) Explain the different types of axle ka housing construction.

17 Explain the following:
i) Testing of chassis frame
ii) Wheel wobble
iii) Differential locks

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Code No. 493 / CBCS

FACULTY OF ENGINEERING

B.E. (CSE) IV – Semester (CBCS) (Main) Examination, May / June 2018

Subject: Computer Organization

Time: 3 Hours **Max.Marks: 70**

Note: Answer all questions from Part – A & any five questions from Part – B.

PART – A (10x2 = 20 Marks)

1 An eight bit register contains the binary value 01001101. What is the value in the register of the arithmetic shift left? Is there an over flow? 2
2 Distinguish between direct and indirect memory reference instructions and specify the number of memory access to get an operand. 2
3 Design a hardware for signed 2's complement addition and subtraction 2
4 What is the function of program counter, instruction register and micro instruction? 2
5 Explain about Direct memory access and indirect memory access. 2
6 What is meant by Pipelining? 2
7 Define Handshaking? 2
8 How super computers differ from Micro computer? 2
9 Where is the "Translation look aside buffer' used? 2
10 What is hit ratio? Explain. 2

PART – B (5x10 = 50 Marks)

11 a) Explain about fixed point representations with suitable examples? 6
b) Write about bus structure? 4

12 How is the register reference instruction different from memory referenced instruction? 10

13 a) Explain instruction cycle with the help of flow and example. 5
b) Explain about address sequencing circuit in micro programmed unit. 5

14 Compare the relative merits of the three cache memory organization
a) Direct mapping cache
b) Fully associative cache c) Set associative cache 10

15 a) Explain Arithmetic pipeline. 5
b) Explain CPU performance and its factors. 5

16 a) Distinguish between asynchronous and synchronous data transfer. 6
b) What are the steps required for pipelined processor to execute an instruction? 4

17 Write a short note on: 10
i) Virtual memory
ii) RISC VS CISC
iii) Stack Organization

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Code No. 499 / CBCS

FACULTY OF INFORMATICS

B.E. (IT) IV – Semester (CBCS) (Main) Examination, May / June 2018

Subject: Scripting Languages

Time: 3 Hours **Max.Marks: 70**

Note: Answer all questions from Part – A and any five questions from Part – B.

PART – A (10x2 = 20 Marks)

1 Define a scripting language

2 Discuss the origin of scripting

3 Describe how to run a python script

4 Differentiate between python 2.x and 3.x

5 Write about the use of break in python program

6 Write a python script to display “Hello World”

7 Give the syntax to define a function.

8 Mention any four built-in functions

9 Write a statement to close a file named “f1”

10 Illustrate with statement with an example.

PART – B (50 Marks)

11 Explain the characteristics of scripting languages.

12 Discuss python operations with an example program.

13 Write the syntax and code segment for the following:
   i) If
   ii) For
   iii) While

14 Illustrate indexing and slicing operations on lists with examples.

15 Explain how to access, update and delete tuple elements.

16 Give the syntax of “Open” function. Write a python program to write and read a file.

17 Write short notes on any two of the following:
   i) Uses of scripting language
   ii) Built-in data types
   iii) Formatting string with %.

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Code No. 237

FACULTY OF ENGINEERING

B.E. 4/4 (Civil) I - Semester (Suppl.) Examination, May / June 2018

Subject : Foundation Engineering

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A & any five questions from Part-B.

PART – A (25 Marks)

1 What are the assumptions of Boussinesq and Westergaard equations?
2 What are the advantages and disadvantages of Neumaark's chart?
3 Define Ultimate bearing capacity and Safe bearing capacity.
4 Why Terzaghi's theory is applicable for shallow foundations only?
5 What is the necessity of pile foundations?
6 Define is Negative skin function.
7 Write about cellular coffer dams.
8 What is well cap, steiming and curb in components of well foundations?
9 What is meant by dewatering?
10 State are the uses of Auger Boring.

PART – B (50 Marks)

11 (a) Derive the expression for point loads by Boussinesq's theory.
(b) Three footings are placed at a distance forming an equilateral triangle side 4m each of the footing carrying a load of 50 tonnes. Calculate vertical pressure by Boussinesq and Westergaard equations at a depth of 3m at the following locations
(i) Below the center of the triangle (ii) Below the center of the footing

12 (a) What are the assumptions made in Terzaghi's analysis ? Derive the expression for it and write its limitations.
(b) A column carries a load of 1000 kN. The soil is dry sand weighing 19kN/m^3 and having an angle of internal friction as 40^o. A minimum factor of safety of 2.5 is required. Use Terzaghi's bearing capacity factors $N_r = 42$, $N_q = 21$.
Also find the size of the footing, if it is placed at ground surface.

13 (a) What is pile foundation? What are the different types of piles? Explain.
(b) A concrete pile of 30 cm diameter is driven into a medium of dense sand having $\phi = 35^o$, $\gamma = 21$ kN/m^3, K = 1, tan $\delta = 0.7$ for a depth of 8m. Estimate the safe load taken by the pile taking a factor of safety of 2.5 Take Nq=60.

14 (a) Define Caissons. What are the different types of caissons? Explain their advantages.
(b) Write a detailed note on coffer dams including their necessity, types of coffer dams, merits, and demerits of each and their suitability with the help of neat sketches.

15 (a) Write a detailed note on methods of dewatering adopted in construction of foundations.
(b) Explain various methods of 'Timbered Excavation" with the help of neat sketches.

16 (a) Write the differences between general shear and local shear failure.
(b) Write detailed note on borehole method of geotechnical investigations.

17 Write short notes on any **two** of the following:
(a) Applications of Boussinesq equation
(b) Classification of settlement
(c) Sampling tubes and sample
(d) Plate load test

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Code No. 247

FACULTY OF ENGINEERING

B.E. 4/4 (EEE) I - Semester (Suppl.) Examination, May / June 2018

Subject: Electric Drives & static Control

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Par A & any five questions from Part B.

PART-A (25 Marks)

1. Draw speed-torque characteristics of dc series motor with shunted armature connection in first quadrant extending it to second and fourth quadrants. (3)
2. Explain briefly steady-state stability of equilibrium point by considering any one type of speed-torque characteristics of load torque and motor torque. (3)
3. Discuss how counter current braking is achieved in a separately excited dc motor. (3)
4. Explain why a 3-phase induction motor draws high current at the instant of dc dynamic braking? (2)
5. A 300 V, 100 A, separately excited dc motor operating at 600 rpm has an armature resistance of 0.25 Ωand controlled by a chopper with a chopping frequency of 1 kHz. Calculate the duty ratio, if the motor is running at 500 rpm and rated torque. (3)
6. A 3-phase, 50 Hz, 1440 rpm induction motor is under braking using plugging. Neglecting stator resistance and total reactance, find the impedance of the motor during braking, with respect to rated impedance. (2)
7. Draw the circuit diagram of a Type E chopper fed dc motor. (3)
8. Draw Voltage to frequency plot of 3-phase induction motor for constant torque and constant power operations from near zero frequency to greater than rated frequency. (2)
9. Mention industrial applications of Switched reluctance motor. (2)
10. Draw speed-torque characteristics of (i) 3-phase synchronous motor and (ii) BLDC motor

Part - B (50 Marks)

11. (a). Explain briefly four-quadrant operation of a drive showing directions of speed and motor & load torques with an example. (6)

    (b). Derive the condition for steady-state stability of a drive system. (4)

12. (a). Obtain an expression for accelerating time of a 3-ϕ induction motor up to its rated speed. (4)

    (b). A 440 V, 50 Hz, 4 pole, 1440 rpm, 3-ϕ star connected induction motor has the following data. Stator impedance per phase = (0.5 + j1.2) Ω. Standstill Rotor impedance per phase = (0.3 + j 1.0) Ω. Determine the initial braking torque soon after (i) plugging and (ii) dc dynamic braking. (6)

..2

13. (a).Draw and explain the operation of a Type B chopper fed separately excited dc motor drive with a neat circuit diagram and show input and output voltages and currents, assuming load current is continuous. (6)

(b). A separately excited dc motor has a constant load torque of 60 Nm. The motor is driven by a 1-ϕ full-wave converter connected to a 1-ϕ, 240 V ac supply. The motor constant is 2.5 V/rad./sec.and the armature resistance is 2 Ω. Calculate the firing angle for the motor to operate at 400 rpm, assuming the armature current is continuous. (4)

14. (a). Draw and explain circulating current mode of operation a dual converter fed dc drive.
(b). Describe inner current loop and outer speed loop operation of a separately excite dc motor with a neat block diagram. (5)

15. (a). With neat circuit diagram, explain how V/f control can be achieved using VSI fed 3-phase induction motor. (5)
(b).What is slip-power recovery? Describe how the slip power can be recovered using a static Krammer drive. (5)

16. (a) What are the functional similarities and dissimilarities between 3-ϕ synchronous motor and BLDC motor? (5)
(b) Explain the variable frequency control of multiple synchronous motors using a neat block diagram. (5)

17. Discuss the following. (10)
(a) 3-phase Cyclo-converter fed 3-phase induction motor
(b) Load inertia and load equalization

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Code No. 523 / N

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I – Semester (New) (Suppl.) Examination, May / June 2018

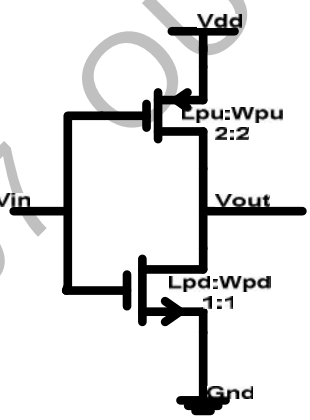
Subject: VLSI Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A & any five questions from Part – B.

PART – A (25 Marks)

1 Draw the Small Signal Model of MOSFET? (2)
2 Draw a neat sketch of transfer character tics of a CMOS Inverter? (2)
3 Distinguish between SRAM and DRAM. (3)
4 Realize two input XOR gate using transmission gates. (3)
5 Draw the schematic diagram of BiCMOS inverter. (3)
6 List out the various distance used in Lambada Based Rules. (2)
7 Draw the schematic diagram of 3 Transistor DRAM cell. (2)
8 Define sheet resistance. (2)
9 Draw the circuit of D-Flip-Flop using Transmission Gate? (3)
10 Calculate the ON Resistance from Vdd to Gnd for the given inverter circuit show in figure. If N – channel sheet resistance is $2x10^4$ Ω per square? R_{sn}= 10^4 Ω per square. (3)



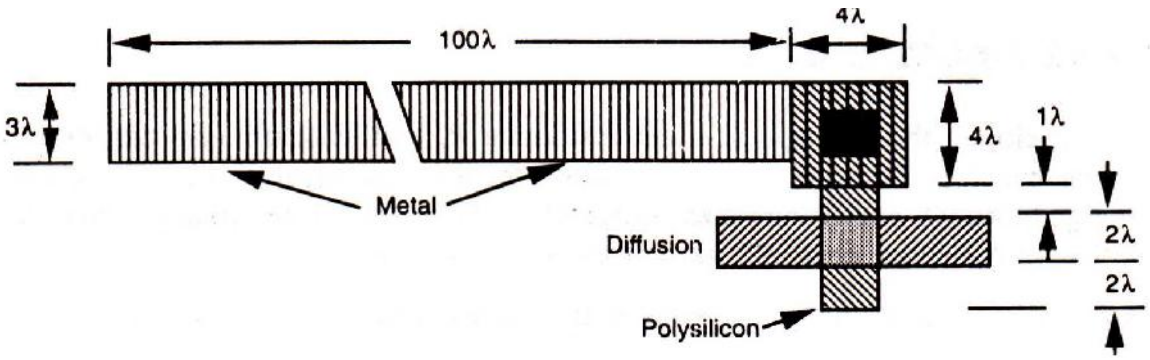
PART – B (50 Marks)

11 a) Derive the drain current expression for n channel enhancement MOSFET. (5)
b) Explain about body effect of MOS transistor. (5)

12 a) Draw the stick diagram for the given function (5)
$f = \overline{A+B+C}$
b) How to estimate propagation delay for CMOS inverter? Explain. (5)

13 a) Calculate the Total Capacitance for given layout (5 µm technology). Calculate the total area of capacitance C_T for multilayer as shown in figure. Find the C_T, C_m, C_g?

Given data capacitance across Metal1 to substrate 0.075 pF x 10^{-4}/µm^2, Polysilicon to substrate 0.1 pF x 10^{-4}/µm^2, Gate capacitance Value1Cg. (7)



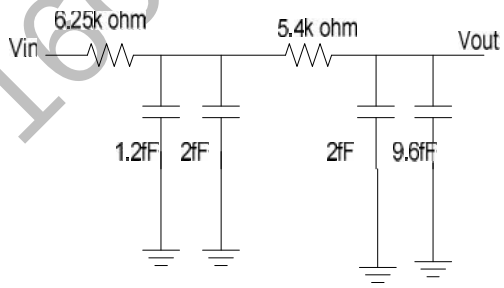
b) Calculate the gate capacitance value of 2 µm technology with relative in minimum sized transistor with gate to channel capacitance value of 8 x 10^{-4} pF / µm^2. (3)

14 a) What is shifter? Draw and explain the operation of Barrel shifter? (5)

b) Draw the structure and explain the operation of Manchester chain adder. (5)

15 a) Draw the schematic diagram of 6T SRAM cell and explain its read and write operation with a neat timing diagram. (5)

b) Explain the Interconnect RC delay? What is propagation delay as calculated by Elmore for Π model from the input to out end of wire for given diagram? (5)



16 a) Draw the small signal model for Common Source Amplifier with current mirror and Explain with its characteristics? (5)

b) Draw and Explain the Source degeneration and Cascode amplifier with Current Mirror? (5)

17 Write short notes on the following

a) Coupling effects on delay (3)

b) Wilson current mirror (3)

c) Electrical properties of MOS. (4)

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Code No: 263/O

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I-Semester (Old) Examination, May / June 2018

Subject: VLSI Design

Time: 3 Hours **Max. Marks: 75**

Note: Answer All Questions From Part–A. Answer any FIVE Questions FromPart-B

PART-A (25 Marks)

1) Describe 'Module' and 'Port' in Verilog with a small example. [3]
2) Explain the levels of abstraction available. [2]
3) Describe different Gate Delays available for specifying delays in logic circuits. [3]
4) What behavioural timing controls are available in Verilog? [2]
5) Describe looping statements. [3]
6) Explain Moore and Mealy models. [2]
7) What is Lambda based design rules? [2]
8) Differentiate clearly between stick diagram and layout diagram. [2]
9) What is the effect of threshold voltage on channel length and body effect? [3]
10) Sketch a stick diagram for a CMOS gate computing $Y = \overline{+ B + C) \cdot D}$ [3]

Part – B(5x10=50 Marks)

11) (a) Explain the two structured procedure statements- 'always' and 'initial'.
(b) Give Verilog code for a Traffic Signal Controller using finite state machine, for controlling traffic where a main road intersects residential colony road. [4+6]

12) (a) Explain Delay back annotationwith diagram.
(b) What is Logic Synthesis? Describe Synthesis design from RTL to Gates. [3+7]

13) (a) What are the continuous and procedural assignments? How these two are differed?
(b) Write a Verilog program for 8 x 3 priority encoder. Write its test bench. [4+6]

14) (a) Using 'force' and 'release' statements write a Verilog description for a negative edge D-Flip-flop.
(b) Write a Verilog program for 2 x 1 Mux in switch level modelling. [5+5]

15) (a) Explain the operation of Manchester carry adder with neat diagrams.
(b) Draw & Explain the barrel shifter? . [5+5]

16) (a) Draw the transmission gate based XOR and XNOR circuits.
(b) Explain about the CMOS inverter characteristics with different loads. [5+5]

17) (a) Draw stick diagram and layout diagram of a simple CMOS inverter, NAND, and NOR gates.
(b) Differentiate between SRAM and DRAM and explain the read and write operation of SRAM cell. [6+4]

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Code No. 272

FACULTY OF ENGINEERING

B.E. 4/4 (M/P/AE) I – Semester (Suppl) Examination, May / June 2018

Subject: Metrology and Instrumentation

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A & any five questions from Part – B.

PART – A (25 Marks)

1 Distinguish between tolerance and allowance of sizes of component.
2 Name different types of micrometers in part measurements.
3 What is a dial indicator operating principle.
4 Explain the use of optical projectors in part measurements.
5 State how surface finish is designated on drawing as per ISO standard.
6 List any five various geometric tests for testing machine tools.
7 What is a transducer? Name different types of transducers used for mechanical engineering programs.
8 What are different Rosette gauge arrangement measure strains?
9 Explain the principle of Seismic instruments.
10 How the ambient temperature change is compensated in thermocouples.

PART – B (5x10 = 50 Marks)

11 a) Distinguish between interchangeable assembly and selective assembly with suitable examples and sketches.

b) Explain the shaft basis and hole basis systems with an example neat sketches.

12 a) Explain the working principles of back pressure type pneumatic comparator with neat sketch.

b) Explain the important features of various types of CMM in component geometric feature measurement.

13 a) How is effective diameter of a screw thread measured using three wire method.

b) Explain the construction and working of Parkinson gear testing machine with neat sketch.

14 a) Explain the various static characteristics of measuring instruments.

b) Explain the principle of operation of Piezo electric load cell, state its advantages.

15 a) Explain with a neat sketch the working principle of Bourdon tube pressure gauge.

b) Discuss the thermocouple circuits principles.

16 a) Explain the working principle of strain gauge load cell to measure pressure.

b) Explain the use of proving ring with a sketch to measure load.

17 Write short notes on the following:
a) LVDT
b) Limit gauges.

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Code No. 297

FACULTY OF ENGINEERING

B.E. 4/4 (CSE) I – Semester (Suppl.) Examination, May / June 2018

Subject: Artificial Intelligence

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A& any five questions from Part B.

PART – A (25 Marks)

1 Consider a state space where start state is numbered as 1 and the successor function for state numbered as 'n' returns two states numbered as 3n and 3n+2. Suppose the goal state is 29. Draw search tree and list the order in which nodes will be visited using following searches: (3M)

a) Breadth First search

b) Iterative Deepening search.

2 Explain the importance of Turing Test. (2M)

3 Obtain wff representation of the statement

Any person who has an umbrella is not wet. (2 M)

4 Explain unification in Predicate calculus (3M)

5 Can we implement OR function using a perceptron. Justify. (2M)

6 What is Bayes network? (2M)

7 List the various phases in natural language processing. (3M)

8 How is common sense knowledge represented. (3M)

9 List out the applications where Neural networks are used. (2M)

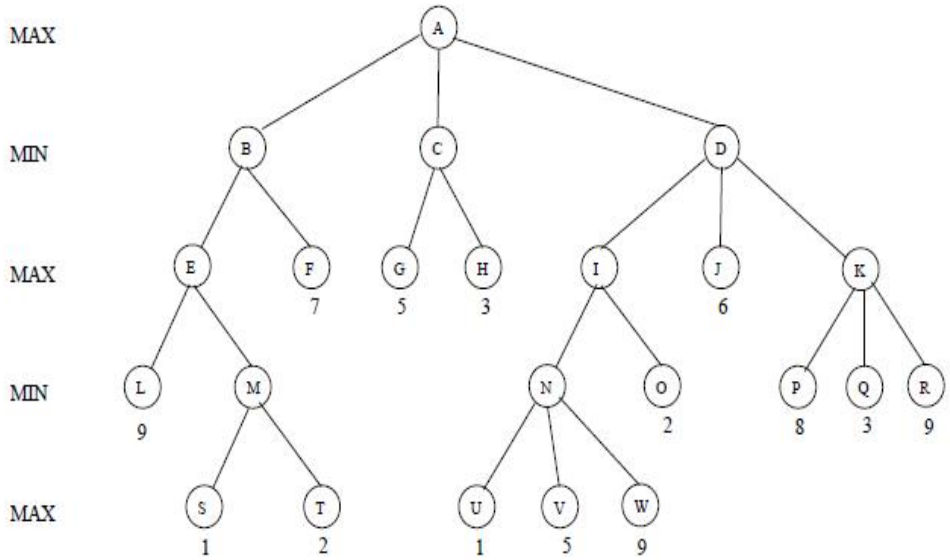
10 Distinguish between crisp set and fuzzy set (3M)

Contd. 2

PART – B (5x10 = 50 Marks)

11 a) Explain about A* algorithm. (5M)

b) Consider this game tree where the root is a maximizing node, and children are visited left to right.



i) Compute the min max game value of nodes A, B, C, and D. (2M)
ii) List the nodes (leaves or interior nodes) that alpha-beta algorithm prune. (3M)

12 a) Describe the architecture of rule based expert system. (5M)
b) Explain rules of inference in propositional calculus. (5M)

13 a) Explain how actions are described using various axioms and the corresponding problems because of such description in Situation Calculus. (6M)
b) Explain about recursive STRIPS. (4M)

14 Explain learning in decision trees using information theory. (10M)

15 What is parsing? Explain top down and bottom up parsing. Generate a parse tree for the sentence: Mary ate the orange. (10M)

16 Write short notes on:
a) Fuzzy inference processing. (5M)
b) Neuro Fuzzy Systems (5M)

17. Explain briefly about
a) General model of learning agents (5M)
b) Backpropogation in multilayer feed forward neural network. (5M)

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Code No. 529 / N

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I – Semester (New) (Suppl.) Examination, May / June 2018

Subject: VLSI Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A and any five questions from Part – B.

PART – A (25 Marks)

1. What is Moore's law? 2
2. Draw the CMOS logic diagram for a non-inverting buffer. 3
3. List out the advantages of silicon on insulator (SOI) technology over twin tub process. 2
4. What is latch up? How do you prevent latch up problem in CMOS logic? 3
5. How delay is reduced by cascading the inverters? 2
6. Define rise time, fall time and delay time. 3
7. Differentiate between SRAM and DRAM. 2
8. Implement two input AND & NAND gate using complementary pass transistor logic. 3
9. Define cross talk & write the equation for coupling capacitor. 2
10. Write Verilog HDL code for half adder. 3

PART – B (10x5 = 50 Marks)

11. a) Derive current equation of an nMOS transistor in saturation region. 5

    b) Implement the logic function $f = \overline{a.(b+c)}$ using CMOS logic and explain with the help of its truth table. 5

12. a) With the help of neat structure, explain how to make the transistors in series and parallel Connections. 5

    b) Difference between active contact and poly contact. Draw stick diagram of the function $f = \overline{A+BC}$ 5

13 a) Draw and explain CMOS process flow. 5

   b) With a neat sketch, explain the CMOS inverter switching characteristics. 5

14 a) Draw the block diagram of differential cascade voltage switch logic. Design a two input XOR & XNOR logic gate using above model. 5

   b) Explain Read & Write operation of 6T SRAM cell. 5

15 a) Draw & Explain VLSI design flow. 5

   b) Implement 4x4 array multiplier & Give one example. 5

16 a) Illustrate the concept of Bubble Pushing. 5

   b) Draw CMOS schematic and layout diagram for CMOS inverter. 5

17 a) With the help of neat sketch, explain cell concepts and cell based design. 5

   b) Explain about Floor planning and routing. 5

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Code No. 307/ O

FACULTY OF INFORMATICS

B.E. 4/4 (IT) I-Semester (Old) Examination, May / June 2018

Subject : VLSI Design

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1	Draw the transmission gate structure of 2 input XNOR gate.	3
2	Write about pass characteristics of PFET.	2
3	Obtain the layout of CMOS NOR2 gate.	3
4	List the rules associated with stick diagram representation.	2
5	Draw the basic cells of NOT2, NAND2 using cell based design.	3
6	Write about extension design rule with an example.	2
7	What is refresh operation in DRAM.	2
8	Draw the CPL structure of AND/NAND gate.	3
9	List the tri-state primitives used in verilog.	2
10	Differentiate between initial and always blocks.	3

PART – B (50 Marks)

11	a)	Obtain the CMOS circuits of the following : i) XOR2 gate ii) XNOR2 gate	5
	b)	Explain the drain and transconductance characteristics of NFET.	5
12	a)	Obtain the layouts for series and parallel connected FETS.	5
	b)	Draw the stick diagram representation of 4 i/p AOI gate.	5
13	a)	Draw the RC switch model equivalent circuit for the CMOS inverter and derive the expression for rise and fall times of the inverter.	7
	b)	To drive a load capacitance C_L = 10 PF and to minimize the delay in a cascade of inverters find the number of stages 'N' and scaling factor 'S' of each stage if the input capacitance C_1 = 20fF.	3
14	a)	Discuss the operation of basic IT DRAM cell.	5
	b)	What is pseudo NMOS logic? Obtain the expression for the low output voltage V_{OL} of a CMOS inverter using pseudo NMOS logic.	5
15	a)	Write verilog code for a 4-bit ripple carry adder.	5
	b)	What is cross talk. What are its effects. Write the expression for coupling capacitance C_C between two interconnect lines.	5
16	a)	What is Domino logic? Draw the domino AND and OR gates.	5
	b)	Obtain the expression for time constant of a m-rung ladder structure of a interconnect line interms of line resistance and capacitance.	5
17	Write short notes :		
	a)	Scaling theory	3
	b)	Layout of a Transmission gate	3
	c)	Photolithiography	4

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