Code No. 28

FACULTY OF ENGINEERING

B.E 2/4 (Civil) I-Semester (Backlog) Examination, May / June 2018

Subject : Engineering Material and construction

Time : 3 Hours **Max Marks : 75**

Note: Answer all questions from Part – A & Any five questions from Part – B.

Part – A (10 X 2 ½ = 25 MARKS)

1. Write the Precautions in blasting
2. What is meant by blending?
3. What is setting time of cement?
4. What are the precautions to be exercised while using motars.
5. Write a short note on recycled aggregates.
6. Draw a neat sketch of horse shoe arch
7. What are the types of floors?
8. Write the procedure of white washing
9. What are the methods in energy conservation in buildings
10. Write the importance of scaffolding

PART B (50 Marks)

11. a) Explain physical and chemical classification of stones. (5)
    b) Explain the composition of good brick in detail (function of each constituent) (5)

12. a) Define water cement Ratio. Discuss the importance of water cement ratio in preparing concrete (5)
    b) Explain the significance of grades of aggregates (5)

13. a) Why is curing necessary? Describe in brief various methods of curing (5)
    b) What are the factors affecting workability and also mention to improve the workability of concrete (5)

14. a) What are the characters of good timber? What are the common uses of timber in construction industry? (5)
    b) Explain in detail about smart materials and explain its importance in construction industry (5)

15. a) What are the different types of tiles and also Explain the characteristics of good tiles? (5)
    b) Explain Indian standard specifications for form work (5)

16 a) Explain the preparation of concrete by 1. Hand mixing 2. Machine mixing (5)
    b) Explain the method of constructing of concrete and terrazzo flooring (5)

17. Write short notes on the following:
    a) blended cement b) storage of reinforcing steel c) smart materials (3+4+3)

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Code No. 32

FACULTY OF ENGINEERING

B.E. 2/4 (EEE) I – Semester (Backlog) Examination, May / June 2018

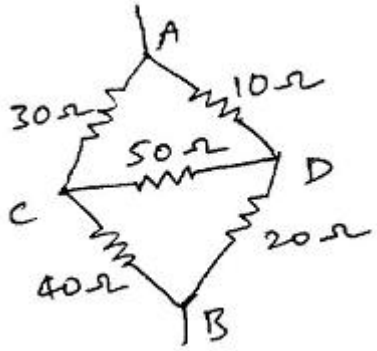
Subject: Electrical Circuits – I

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part A & any five questions from Part B.

PART – A (25 Marks)

1 Find the equivalent resistance of the network shown below between A and B. 3



2 Find the capacitance of a circuit in which an applied voltage of 20V gives an energy store of 0.3 J. 2

3 What are the average value and RMS value of a sinusoidal quantity? 2

4 Draw the impedance locus of parallel connected RL elements. 3

5 What are the advantages of three-phase system? 3

6 The power input to a three-phase induction motor is measured by the two-wattmeter method. The wattmeter read 700 kW and 300 kW, both positive. Find the total power input and the power factor. 3

7 What are the properties of a tree? 3

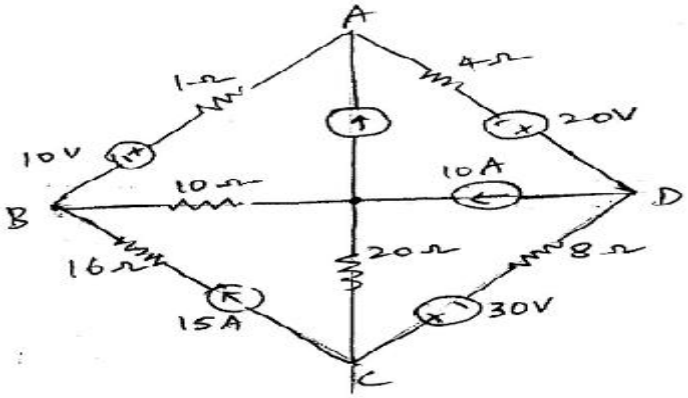
8 What is compensation theorem? 2

9 Write the expression for half power frequencies of RLC series circuit. 2

10 Define bandwidth of series RLC circuit. 2

PART – B (5x10 = 50 Marks)

11 Determine the loop currents for the circuit shown below using mesh analysis. 10



12 When a voltage of 100 V at 50 Hz is applied to a choking coil A the current taken is 8A and the power is 120W (Fig. a), when applied to coil B, the current is 10A and the power is 500 W (Fig. b). What current and power will be taken when 100 V is applied to the two coils connected in series? 10

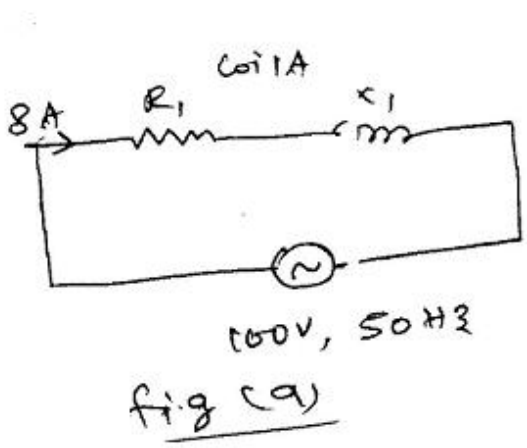


fig (a)

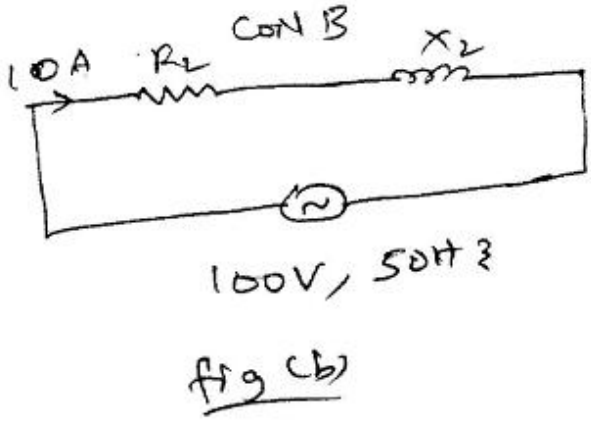
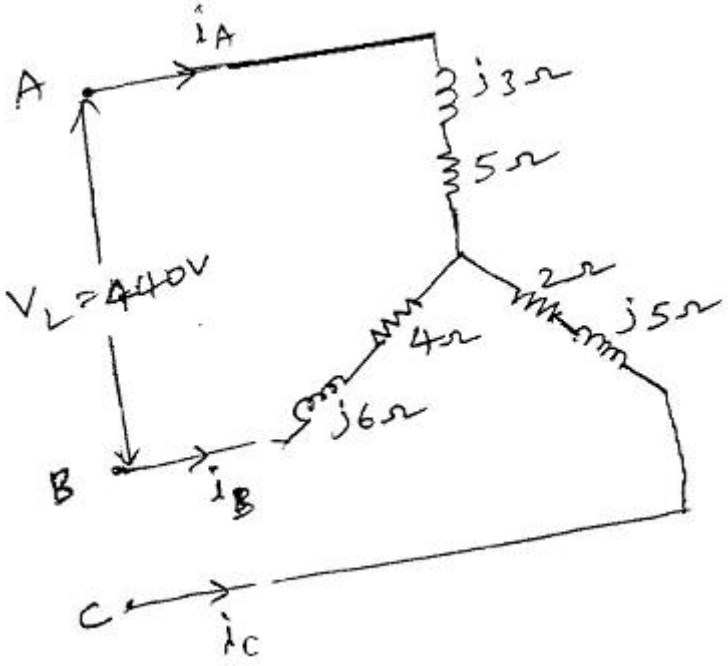
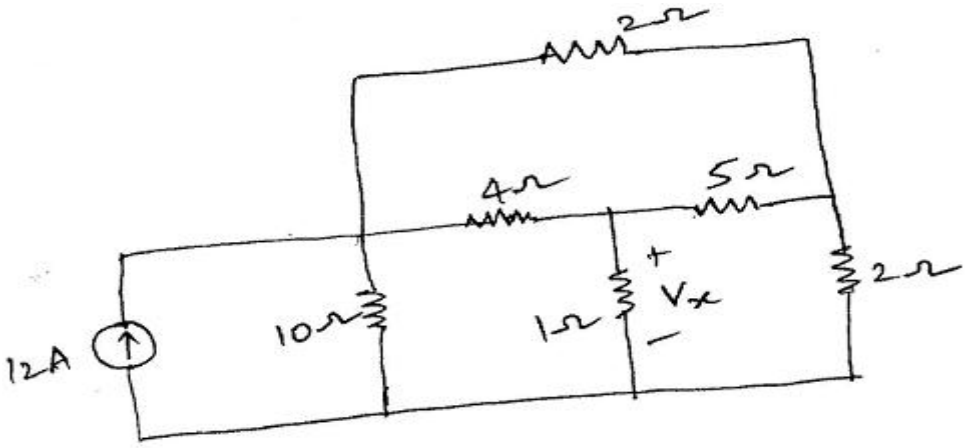


fig (b)

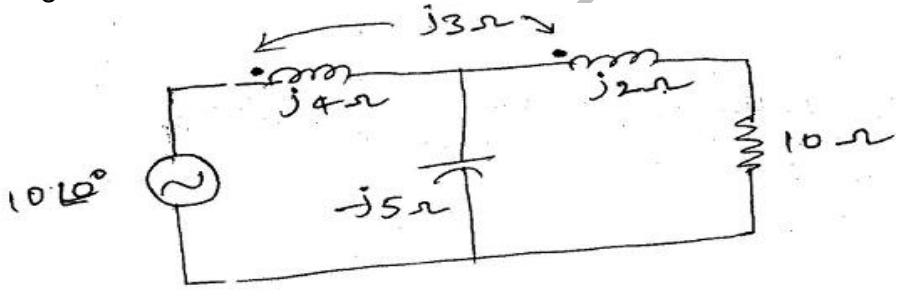
13 Three impedances are connected in star across a three-phase, 440 V supply as shown in figure below. Find the three line currents. Assume ABC as phase sequence. 10



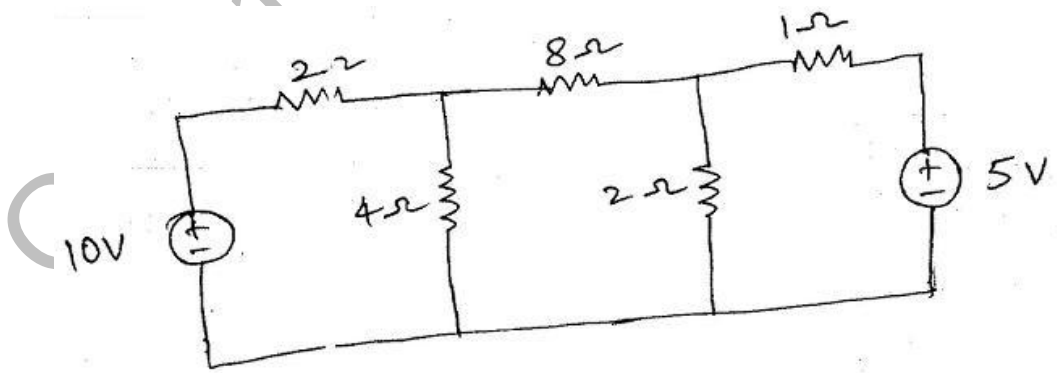
14 Prove reciprocity theorem in the network shown below by interchanging the positions of 12A source and Vx. 10



15 Find the voltage across the 10Ω resistor for the network shown below. 10



16 Determine the branch currents of the circuit shown below by using tie-set schedule. 10



17 Write short notes on:

a) Millman's theorem 5

b) Parallel resonance 5

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Code No: 36

FACULTY OF ENGINEERING

B.E. 2/4 (Inst.) I Semester Backlog Examination, May/June 2018
Subject: Network Theory

Time: 3 Hours **Max. Marks: 75**

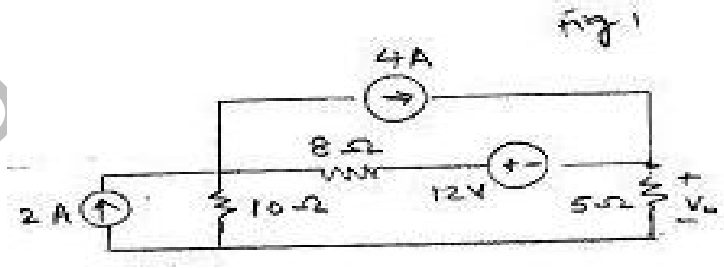
Note: Answer all questions from Part A and any five from Part B

PART – A (25Marks)
(Answer all questions)

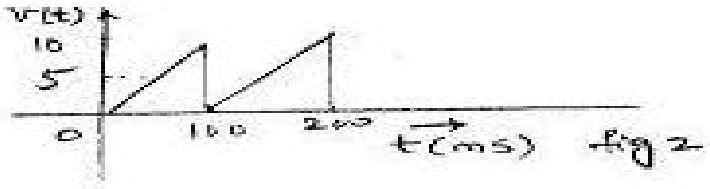
1. What is a dependent(or controlled) source?
2. State Kirchhof's voltage law.
3. State the principle of voltage division.
4. Define coefficient of coupling.
5. Derive the expression for energy stored in a capacitor.
6. What is a unit ramp function?
7. Draw the power triangle for a capacitive load.
8. What is bandwidth of a resonant circuit?
9. If V_{ab}= 400V in a balanced star connected. Three phase generator, find the phase voltages assuming the phase sequence is "abc"
10. What is a two-port Network?

.PART – B (5x10=50 Marks)
(Answer any five questions)

11. (a) State the superposition principle.
    (b) Using super position principle find "V_o" in the circuit shown



12. (a) What is the RMS value of the waveform shown in fig 2.



Contd…2..

(b) Obtain the equivalent inductance at terminals a-b for the circuit shown in a-b for the circuit shown in fig 3.

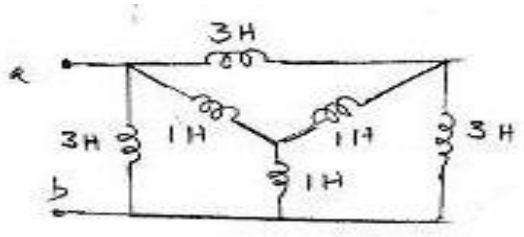


fig:3

13. Two relaxed inductors for fig 4 are connected at t=0 Determine the expression for i(t) for t>0 and sketch it. There is no mutual coupling between the inductors.

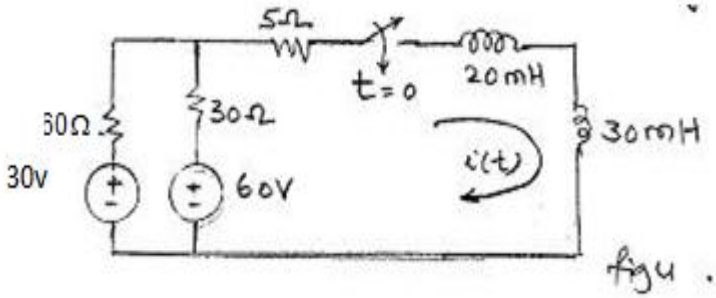


fig 4.

14. Determine the value of capacitance shown in fig 5, such that the total current in the circuit shown will be in phase with the applied voltage.

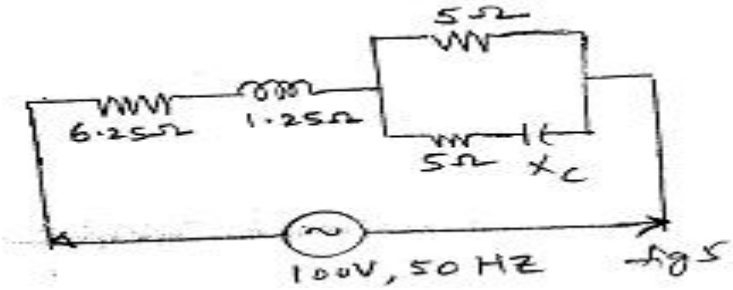


fig 5

15. (a) Find the total inductance of the three series connected coupled coils, given M_{12}=0.5H M_{23}=1H and M_{13}=1H for fig6

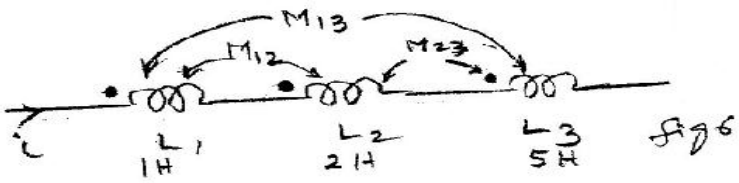


fig 6

contd….3..

(b) A delta connected load has a parallel combination of resistance 5 ohms and capacitive reactance (-j5) ohms in each phase. If a balanced three phase 400V supply is connected between lines find the phase currents and line currents.

16. Find the Z parameters of the network shown in fig 7.

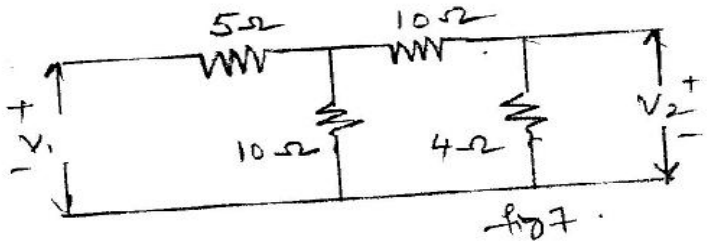


fig 7.

17. Write short notes on:

(a) Maximum Power Transfer Theorem.

(b) Initial conditions in networks.

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Code No. 39

FACULTY OF ENGINEERING

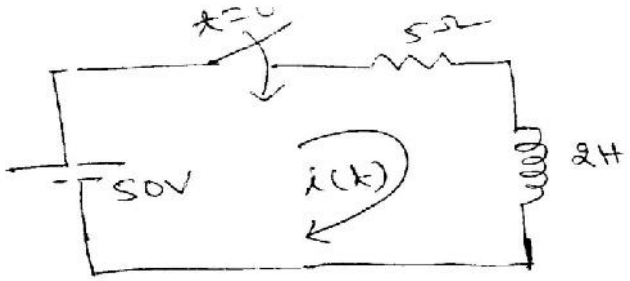
B.E 2/4 (ECE) I-Semester (Backlog) Examination, May/June 2018
Subject : Basic Circuit Analysis

Time : 3 Hours **Max Marks : 75**

Note: Answer all questions from Part – A & Any five questions from Part – B.

Part - A (25 Marks)

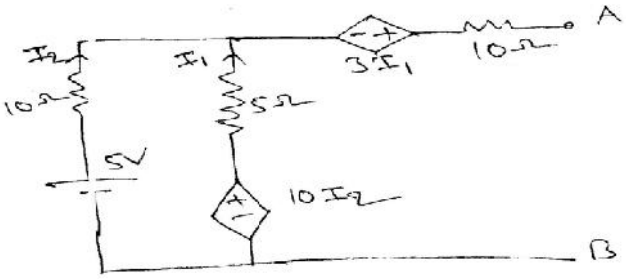
1. State and explain super position theorem? (3)
2. Write the properties of a tree drawn from a electrical network (2)
3. In the given network switch is closed at t = 0, with zero current in the inductor, Find i (t) $\frac{di(t)}{dt}, \frac{d^2i(t)}{dt^2}$ at t = 0^+ (3)



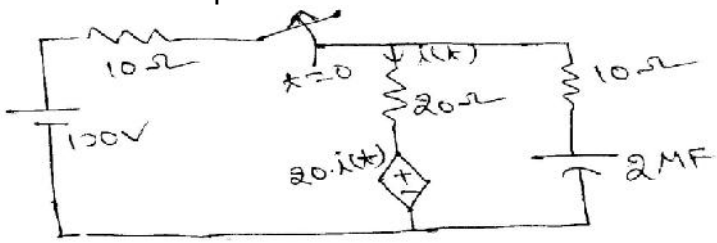
4. An alternating voltage of 100+j80 Volts is applied to a circuit and current flowing through it is 8-j4 Amps. Find impedance, phase angle, power factor, power consumed by the network (2)
5. What is resonance? Derive resonant frequency of a parallel RLC network (3)
6. What is the behavior of circuit impedance of series RLC at low and high frequencies? (2)
7. Derive the condition for symmetry of a two port network (3)
8. The Z-parameters of a two port network are z_{11}=10Ω, z_{22}=20Ω, z_{21}=z_{12}= 5Ω find equivalent T- network (2)
9. What are practical and ideal transformers (3)
10. Define kirchoff's laws (2)

Part - B (50 Marks)

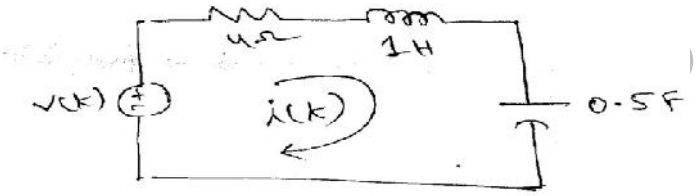
11. Find Thevenin's equivalent network across terminals A and B (10)



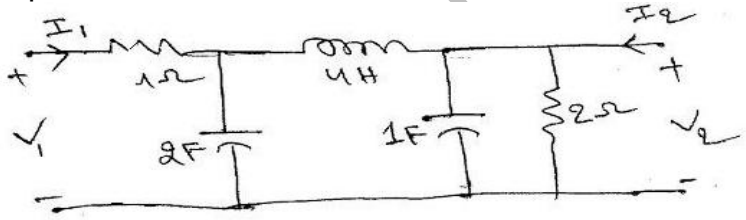
12 Find current i(t) when switch is opened at t=o (10)



13. Determine i(t) assuming zero initial condition when V(t)=sin(t), V(t) = $8e^{-2t}$ (10)



14. Determine ABCD parameters for ladder network shown below (10)



15. A coil having a resistance of 20Ω and an inductance of 200μ*H* is connected in parallel with a variable capacitor. This parallel combination is connected in series with a resistance of 8000Ω. A voltage of 230V at a frequency of 10^6 Hz is applied across the circuit. Find a) capacitance at resonance b) Q-factor of circuit c) total circuit current (10)

16. a) An exponential signal v(t) = e^{jwt} is applied to a series RC network, obtain response i(t). (7)

    b) Define oriented graph, twig, f- cutset and rank of the graph (3)

17. Explain the following

    a) Maximum power transfer theorem with one example (4)

    b) ABCD parameters of ideal transformer (4)

    c) Super node and super mesh (2)

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Code No. 45

FACULTY OF ENGINEERING

B.E. 2/4 (M/P/AE) I - Semester (Backlog) Examination, May / June 2018

Subject : Metallurgy and Materials Science

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A and answer any five questions from Part-B.

PART – A (25 Marks)

1 What is critical Resolved shear stress (CRSS)?
2 Differentiate between slip and Twinning.
3 What is Hall-petch Equation?
4 What methods are useful in improving the fatigue life of material?
5 List out the applications of diffusion.
6 Differentiate a pure metal and on alloy.
7 What is the effect of Nikel chromium and silicon on the properties of steel?
8 What is carburizing?
9 What is Marten site?
10 List out the methods of production of steel.

PART – B (50 Marks)

11 (a) List out different types of crystal dislocations and explain about their impact on mechanical properties.
(b) Differentiate between ductile and brittle fracture.

12 (a) Explain the fatigue behaviour with a neat sketch by R-R-Moore test.
(b) Explain creep behaviour with the help of a creep curve.

13 (a) Explain the method of construction of a phase diagram for isomer phons system.
(b) Differentiate Eutectic, Eutectoid and Peritectic Reactions.

14 Explain the method of construction of a TTT diagram for Eutectoid steel.

15 (a) Explain the manufacturing of steel by Bessemer process.
(b) Explain about Kaldo process.

16 (a) What is powder metallurgy and list out the sequential steps in the process?
(b) List out the types of composites and advantages of composite materials.

17 Write short notes on :
(a) Recrystallization
(b) Austempening
(c) Flame hardening

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CODE NO: 52

FACULTY OF ENGINEERING

B.E 2/4 (CSE) I-semester (Backlog) EXAMINATION, May / June 2018

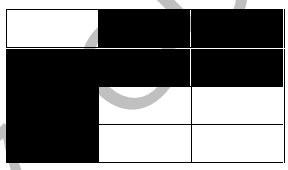
Subject: Discrete Structures

Time: 3 Hours **Max. Marks : 75**

Note: Answer All Questions From Part-A, & Any Five Questions From Part-B**.**

Part-A (25Marks)

1. Write logical equivalence to (pvqvr) ∧ (pvtv~q) ∧(pv~tvr) 3
2. Define the Rule of Universal Generalization 2
3. Define Tautology and Contradiction 2
4. Find the co-efficient of x^5 in $1/(1- 2x)^8$ 3
5. Define POSET 3
6. Define groups and monoids with examples. 3
7. Define Graph coloring 2
8. What is complete bipartite graph 2
9. Find the rook polynomial for shaded board? 3



10. What is Monoid Homomorphism? 2

Part-B (50Marks)

11. (a) Show that from set of premesis 6
    (i) P → q
    (ii) q → (r∧s)
    (iii) ~rv(~tvu)
    (iv) p∧t
    The conclusion is “u”.

    (b) Construct the truth table for (p∧(p->q))->q 4

12. (a) Explain about glb,lub and Lattice 4

    (b) A = {2, 3, 6, 12, 24, 36, 72} R: {(x,y) / x,y ε A, x divides y} write the partial order and draw the hasse diagram for R and compute lower bounds, upper bounds, greatest lower bound, least upper bound for {2,12, 24}. 6

13. (a) Find the coefficient of x^{12} in $(1-x^6)^4/(1-x)^4$ 6
    (b) Explain about generating functions 4

14. Solve recurrence relation $a_{n+2}-4a_{n+1}+3a_n=-200, n>=0, a_0=3000, a_1=3300$. 10

15. (a) What is Isomorphic graphs? Explain various conditions for proving the given groups are isomorphic. 5

(b) Explain about minimum spanning trees with example? 5

16. Explain Ring and Cosets with suitable example? 10

17. Write short notes on : 10
    (i) Groups
    (ii) Recurrence relation
    (iii) Cartesian product

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Code No: 58

FACULTY OF ENGINEERING

B.E. II/IV (IT) I Semester (Backlog) Examination, May/June 2018

Subject: Digital Electronic and Logic Design

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part A and Any Five questions from Part B

PART – A (25 Marks)

1.	Define minimum and Maximum	2
2.	Draw the truth table and logic circuit of Universal gates.	2
3.	Write the difference between PAL and PLA	3
4.	Implement XOR gates using NAND gates	2
5.	Write about 2-input LUT	3
6.	Write the VHDL code for D-latch	3
7.	Give the function of SR-Latch	2
8.	What is state minimization? Explain	3
9.	Explain about dynamic Hazards	3
10.	Write a brief note on Clock-skew	2

PART – B (10x5=50 Marks)

.11. (a) Explain the design process of digital Hardware with the help of Flowchart 5

(b) Reduce the expression to minimum cost SOP from $f(x_1, x_2, x_3) = \sum m(0,1,3,7)$ 5

12. a) Explain the structure of FPGA 5

b) Explain the operation of 4x1 multiplexer and write the VHDL code. 5

13. (a) Write the VHDL code for Full-Addr Circuit. 5

(b) Explain the operation of Basic SR_Latch 5

14. (a) Design a 3-bit up-counter and explain. 5

(b) Give the state reduction procedure with an example. 5

15. (a) What is synthesis? How it is different from Analysis? 5

(b) Give the state reduction procedure with an example. 5

16. Explain FSM as an Arbiter Circuit. 10

17. Write short notes on the following 10

(a) Structure of CPLD

(b) Asynchronous sequential circuits.

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