Code No. 11173

FACULTY OF ENGINEERING

B.E. 4/4 (Civil) I-Semester (Main & Backlog) Examination,

November / December 2018

Subject : Foundation Engineering

Time : 3 hours **Max. Marks : 75**

Note: Answer all questions from Part-A. Answer any FIVE questions from Part-B.

PART – A (25 Marks)

1 Sketch the vertical pressure distribution on horizontal plane at a depth 'Z' from point load Q. 2

2 Determine the vertical stress under the centre of a rectangular area 8 m x 6 m at 5m depth, if the stress under the corner of 4m x 3m area at the same depth is 5 KN/m^2. 3

3 Describe "Refusal" in standard penetration test. 2

4 Differentiate general and local shear failures. 3

5 What is the effect of negative skin friction on load carrying capacity of files? 2

6 Classify pile foundations based on method of installation. 3

7 What are the various components of a well foundation? 2

8 What is meant by caisson sickness? 3

9 Draw the pressure distribution diagram of supported excavation in sand. 3

10 Explain Bore leg. 2

PART – B (50 Marks)

11 a) Write the construction and uses of Newmark's influence chart. 5

b) A over head water tank is provided with a ring type foundation with OD = 10m and 1D = 6m. Compute $\pm_7$ at a depth of 1.5m below center of the ring foundation, if it transmits a UDL of 3000 kPa. 5

12 a) Bring out clearly the effect of ground water table on bearing capacity equation. 5

b) Determine the safe bearing capacity of a 1.2m circular footing located at a depth of 1m below ground level in a soil having C = 30 kN/m^2, ϕ =27^0 and r = 18 kN/m^3. Take FOS = 2.5 and assume water table is present at foundation level. Consider N_c = 32, N_2 = 18, N_q = 16. 5

13 a) Write Hiley's dynamic pile formula and explain the symbols used. 5

b) A group of 20 piles, arranged in 4 x 5 pattern are provided in a clay deposit to a depth of 12m. The size of each pile is 450mm dia. provided at a c/c spacing of 1.05m. The average properties of the clay along the shaft are q_u = 100 kPa, adhesion factor = 0.58. the unconfined compressive strength of the clay at the tip of piles in q_u = 160 kPa, determine the safe load carrying capacity of the pile group. Adopt FS = 2.50. 5

14 a) What is a Coffer dam? Discuss the various types of Coffer dams with their relative advantages and disadvantages. 5

b) Explain the measures for rectification of tilts of well foundations with neat sketches. 5

..2

15 a) Explain in detail about well point method of dewatering. 5
b) Discuss the types of braced excavations with sketches. 5

16 a) Write short notes on proportioning of footings. 5
b) A present concrete pile is driven with a 50 kN hammer, having a free fall of 1m. If the penetration in the cast below is 0.5 cm, determine the load carrying capacity of the pile using engineering news record formula (F.S. = 6.0) 5

17 a) Discuss the comparative merits and demerits of open caissons and pneumatic caissons. 5
b) Discuss various stages in sub surface exploration. 5

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Code No. 11183

FACULTY OF ENGINEERING

B.E. 4/4 (EEE) I - Semester (Main & Backlog) Examination,
November / December 2018

Subject : Electric Drives and Static Control

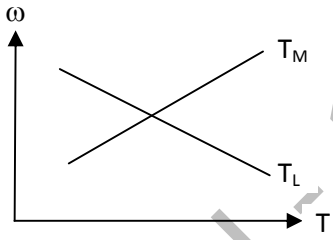
Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A & any five questions from Part-B.

PART – A (25 Marks)

1 Draw closed loop block diagram of an electric drive. (2)

2 Assess whether the following system is stable or unstable from the speed-torque characteristics of motor and load. (2)



3 Derive energy relation during starting for a dc shunt motor. (3)

4 Draw the circuit diagram to show plugging of a (i) dc series motor (ii) dc shunt motor. (3)

5 A separately excited dc motor fed from a 3-phase six pulse fully controlled bridge converter runs at rated speed at 400 V dc supply when firing angle is zero. Find the rms value of supply voltage. (3)

6 What are the advantages of a circulating current mode of operation of a Dual converter fed dc motor drive? (2)

7 Why speed control range of ac voltage controller fed induction motor low? (2)

8 A 3-phase, 400 V, 50 Hz, 4-pole, delta connected squirrel cage induction motor runs at 1425 rpm under constant flux operation. If its equivalent stator and rotor impedances are (1 + j2.6) Ω and (0.5 + j2.4) Ω respectively, then calculate its slip and impedance at 5^{th} harmonic frequency. (3)

9 Draw speed-torque characteristics of switched reluctance motor showing three modes of operation. (3)

10 What are the similarities between brushed dc motor and brushless dc motor? (2)

PART – B (50 Marks)

11 (a) Explain with neat circuit diagram how speed – torque characteristics of a dc series motor can be modified to get definite no-load speed.

(b) A 200 V, 7.46 kW, 600 rpm dc shunt motor has a full load efficiency of 90% and has an armature resistance of 0.25 Ω. Calculate speed of the motor when a series resistance of 1.525 Ω is inserted with armature and armature current is reduced to 20 A.

..2

12 (a) Describe how plugging is performed on 3-phase induction motor showing its speed-torque characteristics in three quadrants.
(b) Explain the process of load equalization and derive an expression for moment of inertia of flywheel.

13(a) A separately excited dc motor is controlled by a single-phase full wave converter. Assuming continuous conduction, draw the following waveforms. (i) supply voltage (ii) supply current (iii) load voltage (iv) load current (v) device current
(b) A 230 V, 1200 rpm, 15 A, separately excited dc motor having an armature resistance of 1.2 Ω is under dynamic braking with chopper control. If braking resistance is 20 Ω and braking torque equal to 1.5 times the rated motor torque, calculate duty ratio of chopper for a motor speed of 1000 rpm.

14 (a) Discuss briefly operation of Cyclo-converter fed 3-phase induction motor drive.
(b) A 3-phase, 400 V, 50 Hz, 4 pole, 1400 rpm, star connected wound rotor induction motor has the following parameters referred to the stator: Rs = 2 Ω ; R'r = 3 Ω ; Xs = 3.5 Ω ; X'r = 3.5 Ω; The stator to rotor turns ratio is 2. If the motor is controlled by Static Scherbius drive, determine the speed range when maximum firing angle is 165^{o}.

15 (a) Discuss briefly the closed loop V/f control of a separate controlled 3-phase synchronous motor.
(b) Explain the construction and control strategy of a 2/4 pole Switched reluctance motor with neat waveforms.

16 (a) Derive an expression for energy relation during starting and plugging of a 3-phase induction motor.
(b) Enumerate the merits and demerits of VSI controlled ac motor over CSI control.

17 Discuss any two of the following
(a) Closed loop control of dc drive
(b) Static Krammer drive
(c) Type A Chopper control of dc motor

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Code No. 11198 / N

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I – Semester (New) (Main & Backlog) Examination,

November / December 2018

Subject: VLSI Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A and any five questions from Part – B.

PART – A (25 Marks)

1	Design OR gate using transmission gates.	(3)
2	Draw the circuit of a BiCMOS inverter.	(2)
3	List various layers in fabrication of CMOS IC.	(3)
4	Draw the stick diagram of a 2-input NOR gate.	(2)
5	Compare Carry Select adder and Carry Skip Adder.	(3)
6	Construct D flip flop using transmission gates	(2)
7	What an interconnect delay is?	(2)
8	Define crosstalk.	(3)
9	Draw the small signal model for a Common Gate amplifier with current mirror Load.	(2)
10	What are high output impedance current mirrors? Draw the circuit diagrams.	(3)

PART – B (50 Marks)

11	a)	Design 2 x 1 MUX using transmission gates.	(3)
	b)	Derive the expressions for the drain current in saturated and non saturated regions	(7)
12	a)	Describe the various steps involved in the fabrication of MOSFET.	(5)
	b)	Draw the layout of a 2-input NAND gate.	(5)
13	a)	Explain the design and operation of a barrel shifter.	(5)
	b)	Explain the operation of a 6T SRAM cell.	(5)
14	a)	What is Elmore delay model. Derive the expression for the RC delay in interconnects.	(6)
	b)	What is interconnect inductance? How is it modeled?	(4)
15.	a)	Derive the expression for the output impedance of a source degenerated current mirror.	(6)
	b)	Derive the expression for the output current of a basic BJT current mirror.	(4)
16	a)	Explain the NOR based and NAND based ROM design.	(7)
	b)	What is latch up? How can it be eliminated?	(3)

17 Write Short notes on: (10)

a) Buffer insertion for very long interconnect wires
b) 3T DRAM cell
c) Body effect.

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Code No. 11198/O

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I-Semester (Old) Examination, November / December 2018

Subject: VLSI Design

Time: 3 Hours **Max. Marks: 75**

Part – A (25 Marks)

1. Difference between verilog HDL and C-Programming language. 2
2. Define inertial delay. Give an example. 2
3. What are the conditional statements in verilog HDL? 3
4. Give the differences between simulation and synthesis. 2
5. What is threshold voltage? How it is depends on channel length? 3
6. Draw Bi-CMOS inverter? Give its truth table. 3
7. How lambda depends on the technology? What is the importance of lambda? 3
8. What is the effect of delay and power as technology is scaling down? 3
9. Draw dynamic RAM cell structure 2
10. What are the advantages of barrel shifter? Draw shifter logic cell to shift left and right. 2

Part – B (50 Marks)

11. a) Develop a verilog code for full adder using HDL. 5

    b) List out concurrent statements and sequential statements in verilog HDL and explain any two from each group in detail. 5

12. a) Differentiate between Tasks and functions. 5

    b) Develop a verilog code for 3 to 8 decoder. 5

13. a) Draw a CMOS inverter? Explain its operation with various loads 5

    b) What is transmission gate logic? Design half adder using this logic. 5

14. a) What are ^{a} -based design rules? Explain in detail. 5

    b) Draw the layout diagram of the function $F = \overline{AB + C}$ 5

15. Derive the drain to source current equation of nMOS transistor is non saturation region, explain. 10

16. a) Design a 4-bit Manchester Carry chain adder and explain its operation. 5

    b) Design a 6T SRAM cell? Explain its write operation. 5

17. Write a short note on
    a) Barrel shifter 3
    b) ROM Memory Design 3
    c) Bi-CMOS inverter stick diagram 4

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Code No. 11213

FACULTY OF ENGINEERING

B.E. 4/4 (M/P/AE) I-Semester (Main & Backlog) Examination,

November / December 2018

Subject : Metrology and Instrumentation

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1. Distinguish between accuracy & precision
2. Explain briefly about the uses of precision polygon
3. Differentiate between roughness and wariness
4. Discuss about chart Gauges application finish of surface
5. What are the various type of plug gauges? Sketch any one of them
6. What are instruments used for machine tool testing?
7. State the conditions for the application of foil, rosette gauges in strain measurement
8. Describe static calibration in pressure gauges
9. List of five thermo couple materials
10. What is rosette gauge?

PART – B (5x10 = 50 Marks)

11 a) What are the basic principles that should be observed in the design of instruments
   b) How slip gauges are manufactured? Give detailed

12 a) What is CMM and explain its important features? Explain the various types of accuracies in CMM.
   b) Explain and Draw the schematic layout of Talysurf.

13 a) Explain the Taylors principle and when does it desirable to take deviations from it?
   b) How do you measure the gear tooth thickness and describe the gear tooth caliper?

14 a) Explain the principle of operation of LVDT and List the advantages & disadvantages.
   b) Describe the principle of torque measurement with a strain gauge torsion meter.

15 a) Explain with help of neat diagram the working of accelerometer using seismic transducer.
   b) Derive the mathematical relation ship between displacement and electrical resistance for simple tension loading for a given gauge factor ‘f’

16 a) Explain the types of errors that occurs measuring instrument
   b) Explain about optical projectors magnification errors

17 Explain the following with suitable sketches
   a) Pirani gauge b) Roundness measurement method
   c) Piezoelectric local cell

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Code No. 11239

FACULTY OF ENGINEERING

B.E. 4/4 (CSE) I-Semester (Main & Backlog) Examination,

November / December 2018

Subject : Artificial Intelligence

Time: 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part A. Answer any five questions from Part B.

PART – A (25 Marks)

1. Define an agent. What is meant by rational agent? 2
2. It Artificial Intelligence is our future? Will it save or destroy humanity? Discuss your perception 3
3. Represent in predicate calculus the knowledge contained the following sentences 3
   (i) Everyone likes someone (ii) All men are mortal
4. Define skolemn function. Give an example 2
5. What is sussman Anamoly? 2
6. Define Situation Calculus? 2
7. Draw a two-layer, feed forward network with 2-inputs, 2-hidden nodes and 2-output nodes 3
8. Write a short note on Bayesian Belief networks? 3
9. Distinguish between crispest and fuzzy set 2
10. What is meant by speechact? List the various categories of seech act. 3

PART – B (5x10 = 50 Marks)

11 Write short notes on :
   a) The minmax procedure 5
   b) The Alpha-beta procedure 5

12 a) Explain Rule Based Learning 5
   b) Write a short notes on unification problem 5

13 Illustrate the three different pattern of inferences using Baye's Network with example 10

14 Apply Decision tree learning algorithm with your own example 10

15 Write short notes on :
   a) Perception in neural network? 5
   b) Fuzzy inference processing 5

16 What is STRIPS planning system? Explain different lists used in defining the operators in STRIPS. Discuss the formal search methods, and recursive STRIPS 10

17 What is a Fuzzy logic system? Explain the various applications of Neuro Fuzzy systems 10

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Code No. 11249/O

FACULTY OF INFORMATICS

B.E. 4/4 (I.T.) I - Semester (Old) Examination, November / December 2018

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions from Part-A & any five questions from Part-B.

PART – A (25 Marks)

1	Define Moores Law.	2
2	Write in brief about the FET threshold voltages.	3
3	Draw the logic diagram and layout of non inverting buffer.	2
4	Write about Design rules.	2
5	What is latchup?	3
6	Write in brief about Domino Logic.	2
7	Write about the pseudo nMOS logic and draw the pseudo nMOS nand gate.	3
8	What is propagation delay and write the expression for the same.	3
9	Write about procedural blocks.	2
10	Write in brief about testing.	3

PART – B (50 Marks)

11	(a) Explain about the pass characteristics of FET.	5
	(b) Design a $NAND_3$ gate using an 8:1 Multiplexer.	5
12	(a) Draw the layout of three input NAND.	5
	(b) Write about photolithography.	5
13	(a) Draw and explain the Inverter Switching Characteristics.	5
	(b) Explain Dynamic CMOS Logic circuit and what is precharge.	5
14	(a) Explain the operating modes of 6T SRAM.	5
	(b) Draw the CVSL of NOR/OR.	5
15	(a) Write about the carry look ahead adder.	5
	(b) Write the verilog code for priority encoder.	5
16	(a) Write about floor planning.	5
	(b) Write about the various routing techniques.	5
17	(a) Write about transmission gates.	5
	(b) Draw and explain VLSI Design Hierarchy.	5

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Code No. 11249 / N

FACULTY OF ENGINEERING

B.E. 4/4 (IT) I – Semester (New) (Main & Backlog) Examination,

November / December 2018

Subject: VLSI Design

Time: 3 Hours **Max.Marks: 75**

Note: Answer all questions from Part – A and any five questions from Part – B.

PART – A (25 Marks)

1. Explain the operation of transmission gate logic? Give its truth table. 2M
2. Implement the logic function of $f = \overline{ab + \overline{C}}$ using CMOS logic. 3M
3. What is meant by Bubble Pushing? 2M
4. Draw the Layout of a CMOS inverter. 3M
5. Draw RC equivalent circuit of a CMOS NAND gate. 2M
6. What are lambda based design rules? Why they should be followed? 3M
7. Write the advantages of pseudo NMOS over CMOS. 2M
8. Draw DRAM cell and explain its Read / Write operation. 3M
9. What are modelling styles in Verilog HDL? 2M
10. What is meant by floor planning? How routing is different from floor planning? 3M

PART – B (10x5 = 50 Marks)

11 a) Derive current equation of an nMOS transistor in linear region. 5M

b) Design 4 to 1 multiplexer using transmission gate logic. 5M

12 a) What are the different layers present in MOSFET? Explain. 5M

b) What is latch up? What are its disadvantages & give prevention techniques? 5M

13 a) With the help of neat sketch, explain cell concepts and cell based design. 5M

b) Draw & explain the CMOS inverter DC characteristics. 5M

14 a) Explain Charge leakage and charge sharing mechanism in dynamic CMOS logic. 5M

b) Explain the operation of SRAM cell and DRAM cell. 5M

15 a) Design a Full adder using CMOS logic. Give its truth table. 5M

b) What are High speed adders? Implement carry look-ahead adder. 5M

16 a) Explain TG base exclusive-OR & exclusive-NOR circuits. 5M

b) Explain the inverter switching characteristics and derive the delay expression. 5M

17 a) Derive the expressions for rise time and fall time. 5M

b) What is meant by crosstalk? Explain the different techniques to optimize it. 5M

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