Code No. 2175/AICTE

FACULTY OF ENGINEERING

B. E. (ECE)VI – Semester (AICTE) Examination, March / April 2022

Subject: Digital System Design with Verilog HDL

Time: 3 hours **Max. Marks: 70**

(Missing data, if any, may be suitably assumed)

PART – A

Note: Answer all questions. **(10 x 2 = 20 Marks)**

1. Explain types of design methodology in Verilog.
2. Write the Verilog module to describe 2 Bit comparator in data flow model.
3. Differentiate between initial and always statement in Verilog.
4. Write the Verilog code for 2:4 decoder in behavioral model.
5. Write the Verilog code for parity generator in behavioral model.
6. Draw blocks of ASM chart.
7. Implement the full Adder using PROM.
8. Differentiate between Full custom and semicustom ASIC.
9. Define Melay and Moore machine.
10. What are races?

PART – B

Note: Answer any five questions. **(5 x 10 = 50 Marks)**

11 (a) Explain system task and compiler directives in Verilog HDL with example.

(b) Write Verilog code for 8 bit comparator using hierarchical modeling and show sample outputs.

12 (a) Write Verilog code for CMOS AND gate in switch level modeling.

(b) Explain VLSI design flow.

13 (a) Minimize the given state table as shown in table1 using partitioning method.

Table 1:state Table

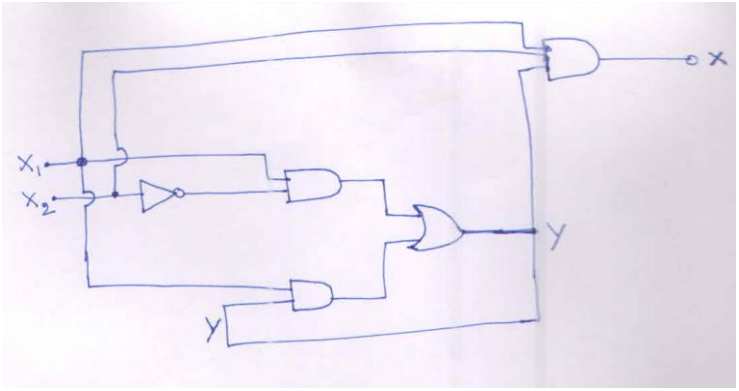
Present state	Input X=0	Input X=1
A	B/0	E/0
B	E/0	D/0
C	D/1	A/0
D	C/1	E/0
E	B/0	D/0

(b) Explain one hot encoding with example.

14 Design synchronous sequential circuit for state table using D flip flop given state assignment A=00, B=01, C=11, D=10.

Present state	NZ, Z	
	X=0	X=1
A	B,0	A,0
B	B,0	C,0
C	D,0	A,0
D	B,0	C,1

15 (a) Analyze the given asynchronous sequential circuit.



(b) Differentiate between ASM and ASMD chart.

16 (a) Realize binary to gray code converter with four input and four output PROM.

(b) Draw and explain operation of 6T SRAM cell.

17 Write a short notes on:

(a) Hazards with design examples

(b) CAD tools.

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