**Code No.ES301EC**

**METHODIST COLLEGE OF ENGINEERING & TECHNOLOGY (An Autonomous Institution)**

**B.E. (CSE/AI&DS) III-Semester (AICTE) (Supplementary) Examination, August-2023**

**Subject: SWITCHING THEORY AND LOGIC DESIGN**

**Time: 3 hours Max.Marks:60**

**Note: Missing data, if any, maybe suitably assumed.**

**PART-A**

**Answer All the questions.**

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| **Q.No.** | **Questions** | **Marks** |  |  |
| **1. a** | **BCD addition of 0110 0111 and 0101 0011** | **2** |  |  |
| **b** | **Perform (E39)16 + (3F9)16** | **2** |  |  |
| **c** | **State and prove De-morgan’s Law** | **2** |  |  |
| **d** | **Find the compliment of x’y’z+x’yz+xy’** | **2** |  |  |
| **e** | **What are the applications of multiplexer?**  | **2** |  |  |
| **f** | **Write verilog code for full adder using gate level modelling** | **2** |  |  |
| **g** | **Compare combinational and sequential logic circuits.**  | **2** |  |  |
| **h** | **Difference between synchronous and asynchronous counter .**  | **2** |  |  |
| **i** | **What is meant by Hamming code?**  | **2** |  |  |
| **j** | **Differentiate between combinational PLD and sequential PLD.**  | **2** |  |  |

**PART-B**

**Answer Any Five questions.**

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| **Q.No.** |  |  **Questions** | **Marks** |  |  |
| **2.** |  | **a) Subtract (01110110)2 from (10110110)2 using 1’s and 2’s complement method.****b) Subtract 366 from 170 in BCD using 10’s complement addition.****c) Perform (417)8 – (232)8 using *8’s complement addition*.** | **3****2****3** |  |  |
|  |  |  |  |  |
| **3. (a)** **(b)** |  |

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|  **Simplify the given Boolean function using Karnaugh Map and obtain the minimum Sum Of Products expression.** **F(WXYZ)=Σ(3,5,6,7)+d(10,11,12,13,14,15)**  |

 | **5** |  |  |
|  | **Determine Canonical POS form for the function T(x, y, z) = x(y’+ z).**  | **3** |  |  |
| **4.** |  | **Write an HDL code for a full adder in all three modelling styles.** | **8** |  |  |
| **5. (a)** **(b)** |  | **Given below is a sequential circuit using D flip-flop. Write the state table and draw a state diagram.** | **4** |  |  |
|  | **What is race around condition? Why does it occur? Discuss how master-slave flip-flop eliminates it.** | **4** |  |  |
| **6. (a)** **(b)** |  | **Generate Hamming code for the given 11-bit message 10001110101 and rewrite the entire message with Hamming code.** | **4** |  |  |
|  | **Explain the construction of a 32 X 4 ROM with a logic diagram.** | 4 |  |  |
| **7.** |  | **Perform subtraction of the following using r’s complement and (r-1)’s****complement methods:****i) (7235)10- (346)10 ii) (1000100)2- (1110100)2** | **8** |  |  |
|  |  |  |  |  |
| **8.** | **a**b  | **Implement full adder using 3x8 decoder. Write verilog code for 3x8 decoder in gate level modeling****Write verilog code for half adder in gate level modeling.** | **6**2 |  |  |
|  |  |  |  |  |
| **9.** | **a** | **Explain PLA with a block diagram.** | **8** |  |  |
| **b** | **A combinational circuit is defined by the functions:****F1(A,B,C)=Ʃ(3,5,6,7) F2= Ʃ(0,2,4,7)****Implement the circuit with a PLA having 3 inputs, four product terms and 2 outputs.** |  |  |  |

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