**Code No.ES301EC**

**METHODIST COLLEGE OF ENGINEERING & TECHNOLOGY (An Autonomous Institution)**

**B.E. (CSE/AI&DS) III-Semester (AICTE) (Regular) Examination, Feb -2023**

**Subject: SWITCHING THEORY AND LOGIC DESIGN**

**Time: 3 hours Max.Marks:60**

**Note: Missing data, if any, maybe suitably assumed.**

**PART-A**

**Answer All the questions.**

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| **Q.No.** | **Questions** | **Marks** |  |  |
| **1. a** | **Discuss 1’s and 2’s complement methods of subtraction.** | **2** |  |  |
| **b** | **Perform conversion (AF9.0C)16 to binary** | **2** |  |  |
| **c** | **Define K-map?** | **2** |  |  |
| **d** | **Use Boolean Algebra to show that A’BC’+AB’C’+AB’C+ABC’+ ABC = A+BC’** | **2** |  |  |
| **e** | **Implement half adder using NAND gate** | **2** |  |  |
| **f** | **Write 1-bit magnitude comparator** | **2** |  |  |
| **g** | **What is a Flip-Flop?** | **2** |  |  |
| **h** | **Difference between synchronous and asynchronous counters** | **2** |  |  |
| **i** | **Classify error detection codes.** | **2** |  |  |
| **j** | **Compare PROM, PLA, PAL** | **2** |  |  |

**PTO**

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**PART-B**

**Answer Any Five questions.**

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| **Q.No.** |  | **Questions** | **Marks** |  |  |
| **2.** |  | **Add the following numbers without converting them to decimal.**  **(i) Binary numbers 1011 and 101.**  **(ii) Octal numbers 62 and 37**  **(iii) Hexadecimal numbers 2E and 34.**  **(iv) Represent the unsigned decimal numbers 791 and 658 in BCD, and then show the steps necessary to form their sum.** | 2  2  2  2 |  |  |
|  |  |  |  |  |
| **3.** | **a** | **Given F(A, B,C,D)= Σm(1, 4, 6, 7, 8, 9, 10, 11, 15). Simplify using K- map method and determine the prime implicants.** | **4** |  |  |
| **b** | **Given F(A, B,C,D)= (1, 4, 6, 7, 8, 9, 10, 11, 15). Simplify using K- map method.** | **4** |  |  |
| **4.** | **a** | **Implement F= A(B+CD) +B’C with NAND gates.** | **4** |  |  |
| **b** | **Implement f(A,B,C,D)= Σ(0,2,3,6,8,9,13,14) using 8 x 1 MUX .** | **4** |  |  |
| **5.** |  | **Design a synchronous counter using JK flip-flops to count the sequence**  **0, 5, 6,7,3,2 and then repeats.** | **8** |  |  |
|  |  |  |  |  |
| **6.** |  | **Implement the following Boolean functions using a 3×4×2 PLA F1 = Σ (0, 1, 3, 4) F2 = Σ (1, 2, 3, 4, 5)** | **8** |  |  |
|  |  |  |  |  |
| **7.** |  | **Using K-map, simplify the Boolean function F in sum of products form, using the don’t care conditions d:**  **F(w, x, y, z) = w’ (x’y + x’y’ + xyz) + x’z’(y+w)**  **d(w, x, y, z)= w’x (y’z + yz’) + wyz** | **8** |  |  |
|  |  |  |  |  |
| **8.** |  | **Design and implement 3 to 8 decoder using gate level modeling** | **8** |  |  |
| **9.** | **a** | **Compare RAM and ROM** | **4** |  |  |
| **b** | **Design a combinational circuit using ROM that accepts a 3-bit binary number and generates output equal to the square of the input number. Use decoder of suitable size to implement ROM.** | **4** |  |  |

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