**Code No.PC407EC**

**METHODIST COLLEGE OF ENGINEERING & TECHNOLOGY**

**(An Autonomous Institution)**

**B.E. (ECE) IV-Semester (Supplementary) Examination, FEB-2024**

**Subject: COMPUTER ORGANIZATION AND ARCHITECTURE**

**Time: 3 hours Max.Marks:60**

**Note: Missing data, if any, maybe suitably assumed.**

**PART-A**

**Answer All the questions.(10X2M=20M)**

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| **Q.No.** | **Questions** | **Marks** |  |  |
| **1. a** | Draw and explain single and double precision IEEE 754 format. | **2** |  |  |
| **b** | Convert (+124.15)10 into normalized floating-point binary. | **2** |  |  |
| **c** | List the Arithmetic instruction set. | **2** |  |  |
| **d** | Differentiate between Hardwired and Microprogrammed control Unit? | **2** |  |  |
| **e** | Write a short note on Parallel Processing. | **2** |  |  |
| **f** | Explain importance of Indirect addressing mode | **2** |  |  |
| **g** | Describe Handshaking Asynchronous transfer with neat timing diagram? | **2** |  |  |
| **h** | Draw and explain the block diagram of I/O processor. | **2** |  |  |
| **i****j** | Write a short note on Memory Hierarchy.Differentiate between virtual address, Logical Address and Physical Address.  | **2****2** |  |  |

**P.T.O**

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**PART-B**

**Answer Any Five questions**.**(5X8M=40M)**

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| **Q.No.** |  | **Questions** | **Marks** |  |  |
| **2.** | **a** | Define floating point representation and draw Floating point addition and Subtraction flow chart.  | **10** |  |  |
| **b** | Solve (-3 X 2) with Booth’s algorithm |  |  |  |
| **3.** | **a** | List the Input output Instructions and explain I/O configuration. | **10** |  |  |
| **b** | Explain micro programmed address sequencer with neat diagram. |  |  |  |
| **4.** | **a** | Explain 4096X16 common Bus system. | **10** |  |  |
| **b** | Explain different types of addressing modes with examples. |  |  |  |
| **5.** | **a** | Define Priority interrupt and serial priority interrupt techniques with neat diagram.  | **10** |  |  |
| **b** | Explain the block diagram of DMA controller. |  |  |  |
| **6.** | **a** | Draw and explain K-Set Associative cache mapping technique. Convert 3FFEFE physical address into logical address with K-set associative mapping. | **10** |  |  |
| **b** | Describe the concept of memory table in paged system. |  |  |  |
| **7.** | **a** | Explain associate memory in detail.  | **10** |  |  |
| **b** | Generate Microoperation sequence for instruction fetch operation. |  |  |  |
| **8.** | **a** | List RISC and CISC features. | **10** |  |  |
| **b** | Write a short note on Input-Output processor and explain CPU-IOP communication. |  |  |  |
| **9.** | **a** | Explain stack organization and solve (3\*4)+(5\*6) using stack with neat diagram. | **10** |  |  |
| **b** | Explain Instruction pipeline and list different types of hazards in instruction pipelining. |  |  |  |

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