**Code No.PC407EC**

**METHODIST COLLEGE OF ENGINEERING & TECHNOLOGY**

**(An Autonomous Institution)**

**B.E. (ECE) IV-Semester (AICTE) Regular Examination, AUGUST-2023**

**Subject: COMPUTER ORGANIZATION AND ARCHITECTURE**

**Time: 3 hours Max.Marks:60**

**Note: Missing data, if any, maybe suitably assumed.**

**PART-A**

**Answer All the questions.(10X2M=20M)**

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| **Q.No.** | **Questions** | **Marks** |  |  |
| **1. a** | Explain difference between ripple carry adder and carry look-ahead adder? | **2** |  |  |
| **b** | Convert (+108.24)10 into normalized floating-point binary. | **2** |  |  |
| **c** | Draw basic computer instruction formats. | **2** |  |  |
| **d** | Differentiate between Hardwired and Microprogrammed control Unit? | **2** |  |  |
| **e** | Write a short note on vector Processing. | **2** |  |  |
| **f** | Explain importance of one bit in addressing mode | **2** |  |  |
| **g** | Compare Isolated Versus Memory Mapped I/O? | **2** |  |  |
| **h** | Explain Asynchronous serial transmission. | **2** |  |  |
| **i**  **j** | Write a short note on Memory interleaving  Differentiate between virtual address, Logical Address and Physical Address. | **2**  **2** |  |  |

**P.T.O**

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**PART-B**

**Answer Any Five questions**.**(5X8M=40M)**

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| **Q.No.** |  | **Questions** | **Marks** |  |  |
| **2.** | **a** | Define floating point representation and draw Floating point addition and Subtraction flow chart. | **10** |  |  |
| **b** | Solve (-12÷ 2) with Restoration algorithm with tabular method |  |  |  |
| **3.** | **a** | Explain Instruction cycle flow chart with timing and control input. | **10** |  |  |
| **b** | Draw and explain design of control unit |  |  |  |
| **4.** | **a** | Explain stack organization and solve (5\*2)-(3\*2) using stack with neat diagram. | **10** |  |  |
| **b** | Explain different types of addressing modes with examples. |  |  |  |
| **5.** | **a** | Draw flow charts and explain different mode of transfers. | **10** |  |  |
| **b** | Explain the block diagram of DMA transfer. |  |  |  |
| **6.** | **a** | Draw and explain Associative cache mapping technique. Convert 3FFEFE physical address into logical address with Associative cache mapping. | **10** |  |  |
| **b** | Explain segment page memory mapping and list hardware for memory management unit? |  |  |  |
| **7.** | **a** | Explain common bus and interconnections between the registers in CPU. | **10** |  |  |
| **b** | Generate Micro operation sequence for instruction Decode operation. |  |  |  |
| **8.** | **a** | Define program control instructions and explain BR and BRA | **10** |  |  |
| **b** | List the need of Interface and explain Interface block diagram. |  |  |  |
| **9.** | **a** | Explain associative memory in detail. | **10** |  |  |
| **b** | Explain Instruction pipeline and list different types of hazards in instruction pipelining. |  |  |  |

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