**Code No.PC409EC**

**METHODIST COLLEGE OF ENGINEERING & TECHNOLOGY**

**(An Autonomous Institution)**

**B.E. (ECE) IV-Semester (AICTE) Regular Examination, AUGUST-2023**

**Subject: INTEGRATED CIRCUITS AND APPLICATIONS**

**Time: 3 hours Max.Marks:60**

**Note: Missing data, if any, maybe suitably assumed.**

**PART-A**

**Answer All the questions. (10X2M=20M)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q.No.** |  **Questions** | **Marks** | **CO** | **BTL** |
| **1. a** | What is Level Translator circuit? Why it is used with cascaded differential amplifiers | **2** | **1** | **II** |
| **b** | Define PSRR, Slew Rate  | **2** | **1** | **I** |
| **c** | Derive the gain of non inverting OPAmp | **2** | **2** | **II** |
| **d** | Develop first order butterworth filter having fh=2KHz | **2** | **2** | **III** |
| **e** | List any four applications of PLL | **2** | **3** | **I** |
| **f** | Explain the features of fixed voltage regulators | 2 | **3** | **II** |
| **g** | Define the terms resolution and conversion time of A/D converters | 2 | **5** | **I** |
| **h** | How do open collector outputs differ from totem pole outputs | 2 | **4** | **I** |
| **i****j** | Design a 4:2 priority encoderList the applications of Shift registers  | 22 | **6****6** | **VI****I** |

**P.T.O**

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**PART-B**

**Answer Any Five questions**. **(5X8M=40M)**

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| **Q.No.** |  | **Questions** | **Marks** | **CO** | **BTL** |
| **2.** | **a** | Evaluate the voltage gain of single input balanced output differential amplifier | **4** | **1** | **V** |
| **b** | Draw and explain the block diagram of an OPAMP | **4** | **1** | **II** |
| **3.** | **a** | Prove that OPAMP can be used as a differentiator. Plot the output of the differentiator, if the input is an sinusoidal signal | **4** | **2** | **V** |
| **b** | Develop a second order HP Butterworth filter for a cutoff frequency of 1KHz? Plot its frequency response  | **4** | **2** | **III** |
| **4.** | **a** | Determine the Monostable mode of operation of IC 555 timer? Derive the pulse width? | **4** | **3** | **V** |
| **b** | Explain the block diagram of PLL and the function of each block | 4 | **3** | **II** |
| **5.** | **a** | Compare TTL, ECL, CMOS logic families with respect to fan-out, noise margin, tpd and Pd | **4** | **4** | **V** |
| **b** | Explain the operation of Flash type ADC with neat diagram | **4** | **5** | **II** |
| **6.** | **a** | Explain the operation of a Carry look ahead adder  | **4** | **6** | **II** |
| **b** | Build a 3bit Synchronous up counter using JK flip flops. | **4** | **6** | **VI** |
| **7.** | **a** | Define input bias current, input offset current, input offset voltage, output offset voltage and also write their typical values | **4** | **1** | **I** |
| **b** | Explain the operation of Schmitt trigger using OPAMP | **4** | **2** | **II** |
| **8.** | **a** | Explain the working of IC 723 as low voltage regulator | **4** | **3** | **III** |
| **b** | Explain CMOS transmission gate with neat diagrams | **4** | **4** | **II** |
| **9.** | **a** | Implement F (a, b, c, d) = ∑m (2, 4, 6, 7, 9, 10, 11, 12, 15) using 8:1 mux. | **4** | **6** | **VI** |
| **b** | Explain the operation of a PLL as Frequency Multiplier | **4** | **3** | **IV** |

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