COURSE FILE

5PC301EC – Electronic Devices

ACADEMIC YEAR 2022-23

III SEMESTER

BY

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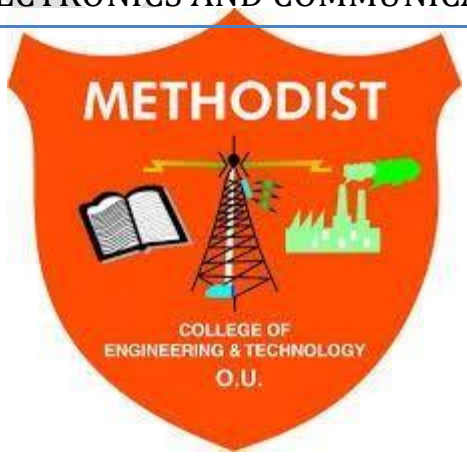
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION

To strive to become center of excellence in Education, Research with moral, ethical values and serve society.

DEPARTMENT MISSION

M1: To provide Electronics and Communication Engineering, knowledge for successful career either in industry or research.

M2: To develop Industry-Interaction for innovation, product oriented research and development.

M3: To facilitate value added education combined with hands-on trainings.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROGRAMME EDUCATIONAL OBJECTIVES

After 3-5 years of graduating, the graduates will be able to:

- **PEO 1:** Apply the knowledge of Basic sciences and Engineering in designing and implementing the solutions in emerging areas of Electronics and Communication Engineering.
- **PEO 2:** pursue the research or higher education and practice profession.
- **PEO 3:** Adapt to the technological advancements for providing the sustainable engineering solutions to meet organization/society needs.
- **PEO 4:** Work as an individual or in a team with professional ethics and values.

PROGRAM SPECIFIC OUTCOMES (PSOs)

1. **PSO1: Professional Competence**: Apply the knowledge of Electronics & Communication Engineering principles in VLSI, Signal processing, Communication, Embedded system & Control Engineering
2. **PSO2: Technical Skills:** Design and implement products using the cutting- edge software and hardware tools
3. **PSO3: Social consciousness**: Demonstrate the leadership qualities and strive for the betterment of organization, environment and society

HOD (ECE)

PROGRAM OUTCOMES (POs)

A. PO1: Engineering Knowledge
B. PO2: Problem Analysis
C. PO3: Design/Development of Solutions
D. PO4: Conduct investigations of complex problems
E. PO5: Modern Tool usage
F. PO6: Engineer & Society
G. PO7: Environment & Sustainability
H. PO8: Ethics
I. PO9: Individual & Team work
J. PO10: Communication
K. PO11: Project Management & Finance
L. PO12: Lifelong learning

Upon the completion of program , the student will be able to

A. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and engineering specialization to the solution of complex engineering problems.

B. **Problem analysis:** Identify, formulate, research literature, and analyze engineering problems to arrive at substantiated conclusions using first principles of mathematics, natural, and engineering sciences.

C. **Design/development of solutions:** Design solutions for complex engineering problems and design system components, processes to meet the specifications with consideration for the public health and safety, and the cultural, societal, and environmental considerations.

D. **Conduct investigations of complex problems:** Use research-based knowledge including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

E. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

F. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

G. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

H. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice

I. **Individual and team work:** Function effectively as an individual, and as a member or leader in teams, and in multidisciplinary settings.

J. **Communication:** Communicate effectively with the engineering community and with society at large. Be able to comprehend and write effective reports documentation. Make effective presentations, and give and receive clear instructions.

K. **Project management and finance:** Demonstrate knowledge and understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team. Manage projects in multidisciplinary environments.

L. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

SCHEME OF INSTRUCTION & EXAMINATION

B.E. (ELECTRONICS AND COMMUNICATION ENGINEERING) IV – SEMESTER

Course Code	Course Title						Core/ Elective
5PC301EC	**Electronic Devices**						**Core**
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	**3**	**0**	**-**	**0**	**40**	**60**	**3**

Course Objectives

This course aims to familiarize:

1. The concepts of semiconductor devices like PN junction diode, Transistor, and special diodes.
2. The applications of diodes.
3. To familiarize the students with various two terminal and three terminal electronic devices working and usein the design of real time electronic products.
4. Design DC biasing techniques and evaluate A.C parameters for BJT in Amplifier Applications.
5. Explore V-I characteristics of FETs, MOSFETs and study IC fabrication techniques

Course Outcomes

1. Demonstrate understanding of the characteristic behavior of various electronic devices such as Diodes, Transistors etc, and applying them for understanding variouscircuits
2. Evaluate the performance parameters of various diode circuits (rectifiers, clippers and clampers) Identify the merits and demerits of various filters, formulate and design rectifier circuits with filters Calculate ripple factor, efficiency and percentage regulation of rectifier circuits.
3. Discriminate the BJT configurations to recognize appropriate transistor configuration for any given application and design the biasing circuits with good stability.
4. Analyze and design various circuits for different applications in Engineering Field.

UNIT-I

Semiconductor Diode Characteristics: The p-n junction Diode, Energy band diagram, Current equations, V-I characteristics, Temperature dependence, Diode resistance-Static and Dynamic, Transition capacitance, Diffusion capacitance, Zener diode, Avalanche breakdown, Zener breakdown mechanisms – Zener diode as voltage Regulator, Hall effect.

UNIT-II

Diode Applications: Diode as a circuit element, Clipping and clamping circuits, clamping circuit theorem. Half wave, Full wave and Bridge Rectifiers - their operation, performance characteristics- ripple factor calculations, and analysis; Filters (L, C, LC and CLC filters).

Special Purpose Semi-Conductor Devices: Elementary treatment of Sillicon controlled rectifier (SCR), UJT,Tunnel diode. Schottky diode,LED, Photodiode, Solar cell.

UNIT – III

Bipolar Junction Transistor:

Construction and Operation of Bipolar Junction Transistor, current components, Modes of transistor operation, BJT input and output characteristics of CB, CE, CC configuration, early effect

Biasing and Stabilization: Biasing techniques**,** Stabilization factors, Compensation techniques, Thermal run away, Thermal Stability

UNIT –IV

Small Signal Transistors equivalent circuits: Small signal low frequency h-parameter model of BJT,

Approximate model, Analysis of BJT amplifiers using approximate model for CB, CE and CC configurations

UNIT-V

Field Effect Transistor: Junction Field Effect Transistor: Principle of Operation - the Pinch-off Voltage VP, V-I Characteristics of JFET.

MOSFETs: Enhancement & Depletion mode MOSFETs, V-I characteristics, CMOS inverter. Small signal model analysis for FET

Text Books:

1. Millman and Halkias, "Electronic Devices and Circuits", 2nd Edition, McGraw Hill Publication, 2007.
2. Robert L. Boylestad, "Electronic Devices and Circuit Theory", 10th Edition, PHI, 2009.
3. S.K. Gandhi, "VLSI Fabrication Principles: Silicon and Gallium Arsenide", Wiley India Pvt. Ltd., New Delhi,2nd Edition. 1994.

Suggested Reading:

1. Jacob Millman, Christos Halkias, Chetan Parikh, "Integrated Electronics", 2nd Edition, McGraw Hill Publication,2009.
2. David Bell, "Fundamentals of Electronic Devices and Circuits", 5th Edition, Oxford University Press, 2008.
3. Christian Piguet, "Low Power CMOS Circuits Technology, Logic Design and CAD Tools" 1st Indian Reprint, CRCPress, 2010.

E – RESOURCES

NPTEL VIDEOS on Electronic Devices

1. https://onlinecourses.nptel.ac.in/noc19_ee54/unit?unit=24&assessment=82https://www.youtube.com/watch?v=cAu_Qv6rsM8 for unit-1
2. https://www.youtube.com/watch?v=G-BvuL5IDLw for unit-2
3. https://onlinecourses.nptel.ac.in/noc19_ee54/unit?unit=5&lesson=8
4. https://onlinecourses.nptel.ac.in/noc19_ee54/unit?unit=42&lesson=44
5. https://www.youtube.com/watch?v=1fgw-ONlAcc for unit-3
6. https://www.youtube.com/watch?v=X2lqQzi4b9w. for unit-5

Course Objectives

1. The concepts of semiconductor devices like PN junction diode, Transistor, and special diodes.
2. The applications of diodes.
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IMPORTANCE OF THE COURSE AND HOW IT FITS INTO THE CURRICULUM

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Course Overview:

History and overview of electronics from vacuum tubes to large scale integration, including reasons for studying electronics, selected important areas of application, role of electronics in computer engineering. Semi-conductivity: materials and properties, electrons and holes, concept of doping, acceptors and donors, p and n-type materials, conductivity and resistivity. Diodes and Circuits: symbol and representation, diode operation and characteristics, region of operation and limitations, zener and SCR diodes, diode circuit and load line, diode application in rectifier and dc/dc converter. Bipolar Junction Transistors (BJT): physical structure of BJT, symbol and circuit representation, NPN and PNP transistor operation, voltage-current characteristics of transistors, transistor region of operation and limitation, transistor circuit analysis, biasing for logic application,

The objectives of this course are to impart to the following to the students:

The objective of this course is to equip students with the required mathematical tools necessary to analyze and understand basic analog and digital electronic components and circuits such as diodes, transistors etc. A student who completes the course successfully will be able to demonstrate among other things:

- Keen understanding of what basic electronic components are: their device structure, principle of operations, mathematical modelling and analysis, circuit representations and integrations
- Technical know-how of system behaviour based on device characteristics and models
- Analyze the behaviour of Semiconductor diodes in Forward and Reverse bias
- Good understanding Half wave and Full wave rectifiers with L,C,LC & CLC Filters
- Technical know-how V-I characteristics of Bipolar Junction Transistor in CB,CE & CC configurations
- Design Operational Amplifier circuits , Oscillators and linear & non linear Applications
- State Boolean laws and theorems. State and explain the different logic gates using truth table. Analyze and design different adder circuits.

Instructional learning outcomes

Subject: Electronic Devices

UNIT-I

Semiconductor Diode Characteristics: The p-n junction Diode, Energy band diagram, Current equations, V-I characteristics, Temperature dependence, Diode resistance-Static and Dynamic, Transition capacitance, Diffusion capacitance, Zener diode, Avalanche breakdown, Zener breakdown mechanisms – Zener diode as voltage Regulator, Hall effect.

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COURSE MAPPING WITH CO'S

CO-PO MAPPING TABLE:

PO / CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PS0 1	PSO 2	PSO 3
5PC301EC	2	1	-	-	1	-	-	-	-	-	-	-	2	-	-
5PC301EC	3	3	-	-	1	-	-	-	-	-	-	-	3	-	-
5PC301EC	3	3	-	-	1	-	-	-	-	-	-	-	3	-	-
5PC301EC	3	3	1	1	1	-	-	-	-	-	-	-	3	2	-
5PC301EC	3	3	2	2	1	-	-	-	1	-	-	-	3	2	-
5PC301EC	3	3	2	2	1	-	-	-	1	-	-	-	3	2	-
301	2.8	2.7	1.7	1.7	1.0	-	-	-	1	-	-	-	2.8	2.0	-

Gaps identified based on the mapping:

1. The syllabus covers theory, concepts and problem solving using fundamental principles related to engineering knowledge only. The Program Outcomes from 6 to 8 and 10 to 12 are not directly addressed.

Plan of Action / Corrective measures:

1) Teaching the Electronic Devices concepts through video animations and virtual learning sites, will help in using modern ICT tools in learning the subject effectively. The following websites are provided for the students to watch and learn.
2) Teaching of professional ethics can be integrated in the course by encourage to students to do the assignments and quizzes honestly and to teach them to report the experimental observation without manipulation.
3) Team work and technical communication is encouraged by giving the student group assignments and group tasks to solve a complex problem in parts.
4) In addition to the above, simple topics of the subject were assigned to the students to present it in the class and this encouraged the students to communicate effectively to the students of the class. This practice indirectly helped the students in preparing the document on the topic he/she is going to address to the class and this intern helped in making use of modern tools to present the topic.

Revised Mapping closing the gaps:

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PS01	PSO2	PSO3
5PC301EC.1	3	3	2					1	1	1			3	2	
5PC301EC.2	3	2	1	2	2			1	1	1			3	2	
5PC301EC.3	3	2	1	2	3			1	1	1			3	2	
5PC301EC.4	3	2	1	1	2			1	1	1			3	2	
5PC301EC.5	3	2	2	2	3			1	1	1			3	2	
5PC301EC.6	3	3	3	2	3			1	1	1			3	3	
5PC301EC	3.00	2.33	1.67	1.80	2.60			1.00	1.00	1.00			3.00	2.17	

1.96

CO-PO/PSO mapping Justification

Mapped POs & PSOs (Direct): PO1, PO2, PO3, PO4, PSO1 and PSO2
Mapped POs & PSOs (Corrective measures): PO8, P09 and P10

Course outcomes:

1. 5PC301.1: Demonstrate understanding of the characteristic behavior of various electronic devices such as Diodes, Transistors etc, and applying them for understanding variouscircuits **(Understanding)**

	Mapping Level	Justification
PO1	2	Definitions of doping, intrinsic and extrinsic semiconductors, energy band theory – type of bonding in semiconductor materials, effect of temperature on the behaviour of semiconductors- fundamental principle of operation of semiconductors in forward bias and reverse bias and their applications- directly contribute to engineering knowledge.
PO2	1	The above definitions and concepts are directly supportive in understanding the problem analysis of Electronic Devices and circuits
PO5	1	Encouraging learning of basic concepts through ICT teaching-Learning resources
PO8	1	Indirect but practical approach to teach honesty in learning process
PO9	1	Group assignments and tasks
PO10	1	Group assignments and mutual presentations

5PC301EC.2 : Evaluate the performance parameters of various diode circuits (rectifiers, clippers and clampers) Identify the merits and demerits of various filters, formulate and design rectifier circuits with filters Calculate ripple factor, efficiency and percentage regulation of rectifier circuits. **(Applying)**

	Mapping Level	Justification
PO1	3	Characterization of current flow in the semiconductor devices , applying proper dc voltages and currents to the device/device based circuits to set up the Quiescent point –setting up of Quiescent point helps in application of the device in circuits are all directly related to engineering knowledge and needs understanding of Fundamental Electronic Devices & mathematical principles.
PO2	2	Directly supportive for problem analysis
PO5	1	Encouraging learning from ICT learning tools and useful videos
PO8	1	Indirect but practical approach to teach honesty in learning process
PO9	1	Group assignments and tasks
PO10	1	Group assignments and mutual presentations

5PC301EC.3 **Make use of** knowledge on design trade-offs in various digital electronic families with a view towards reduced power consumption **(Applying)**

	Mapping Level	Justification
PO1	3	Applying the physical principles and mathematical formulations to evaluate various digital electronic families with a view towards reduced power consumption.This is directly enhancing engineering knowledge for problem solving.
PO2	2	The above is directly supportive in understanding the problem analysis of Basic electronics.
PO5	1	Encouraging learning from ICT material and videos
PO8	1	Indirect but practical approach to teach honesty in learning process
PO9	1	Group assignments and tasks
PO10	1	Group assignments and mutual presentations

5PC301.4 : **Examine** Operational Amplifier circuits as Summer, differentiator, integrator, inverting and non inverting amplifiers as ideal and practical.**(Analyzing)**

	Mapping Level	Justification
PO1	3	Directly contributing to engineering knowledge and analyzing to make appropriate choice of analog mathematical operations in engineering applications
PO2	3	Directly dealing with enhancing problem analysis skills
PO3	1	Directly supportive in designing of structural members based on analysis and suitable interpretation of the available data.
PO4	1	Forms foundation principles to solve complex problems.
PO5	1	Encouraging learning from ICT material and educational videos & animations
PO8	1	Indirect but practical approach to teach honesty in learning process
PO9	1	Group assignments and tasks
PO10	1	Group assignments and mutual presentations

5PC301.5. **Evaluate** Boolean laws and theorems. State and explain the different logic gates using truth table. Analyze and design different adder circuits **(Evaluating)**

	Mapping Level	Justification
PO1	3	Directly enhancing engineering knowledge
PO2	3	Directly dealing with enhancing problem analysis skills
PO3	2	Encourages comparison of volume material used and the safety criteria in design.
PO4	2	Involves interpretation skills from comparison of engineering data.
PO5	1	Encouraging learning from ICT material and educational videos & animations
PO8	1	Indirect but practical approach to teach honesty in learning process
PO9	1	Group assignments and tasks
PO10	1	Group assignments and mutual presentations

5PC301.6: **Design of** half wave and full wave rectifiers without and with filters **(Creating)**

	Mapping Level	Justification
PO1	3	Directly enhancing engineering knowledge but analyses and appropriate graphical representation of the engineering data
PO2	3	Directly dealing with enhancing problem analysis skills
PO3	2	Essential pre-requisite in designing of half wave and full wave rectifiers without and with filters based on analysis and suitable interpretation of the available data.
PO4	2	Form foundation principles to solve complex problems in real life situations
PO5	1	Encouraging learning from ICT material and educational videos & animations
PO8	1	Indirect but practical approach to teach honesty in learning process
PO9	1	Group assignments and tasks
PO10	1	Group assignments and mutual presentations

I. TEACHING-LEARNING METHODOLOGY ADOPTED

1. Chalk and Talk
2. PPTs, Animations and Videos for illustrations
3. Learning by doing
4. Collaborative Learning (Think Pair Share)
5. Group Assignment – Project

II. METHOD OF ASSESSMENT OF COs and POs:

COs	Relevant POs	Mode of Assessment
5PC301.1- 5PC301.6	PO1: ENGINEERING KNOWLEDGE PO2: PROBLEM ANALYSIS PO3: DESIGN/ DEVELOPMENT OF SOLUTIONS PO4: CONDUCT INVESTIGATION ON COMPLEX PROBLEMS PSO1: PROFESSIONAL COMPETENCE	Assignments, Quizzes, Internal Examinations and External Examination result
5PC301.1- 5PC301.6	PO5: MODERN TOOL USAGE	Exercises to learn through ICT tools and internet websites, Usage of Excel worksheets for problem solving
5PC301.1- 5PC301.6	PO8: ETHICS	Assignments, Quizzes
5PC301.1- 5PC301.6	PO9: IINDIVIDUAL AND TEAM WORK PO10: COMMUNICATION	Group Assignments, Writing skills in documenting assignments, Presentations

FINAL COURSE ATTAINMENT

CO Attainment	Internal I	Internal II	University Examination	Overall Direct (%)	Overall Direct (Rubric)	Overall Indirect (Rubric)	Overall CO Attainment
CO 1	**78.26**		77.778	78.02	3	2.6	2.92
CO 2	**69.74**		77.778	73.76	3	2.51	2.902
CO 3		**56.08**	77.778	66.93	3	2.56	2.912
CO 4		**79.84**	77.778	78.81	3	2.53	2.906
CO 5		**78.81**	77.778	78.30	3	2.51	2.902
CO 6		**75.78**	77.778	76.78	3	2.51	2.902
Overall Course Attainment					**3.00**	**2.54**	**2.91**
Set Target for the course					1.96	1.96	1.96
Course Attainment Status(Yes/No)					**Yes**	**Yes**	**Yes**

Note:

1. Direct Method Attainment = 50% of Internals + 50% of University Exams
2. The University Exam Results includes the Internals, thus its Weightage is reduced to 50% instead of 70%
3. Overall Attainment = 80% Direct Method + 20% Indirect Method.

CO Percentage Score	CO Attainment Rubric
%CO >= 60%	3
50% <= %CO < 60	2
40 <= %CO < 50	1

CLASS TIME TABLE (2022-23)

Day	9:30-10:30	10:30-11:30	11:30-12:30	12:30-1:15	1:15-2:15	2:15-3:15	3:15-4:15
MON		IC LAB B2		**L U N C H**		ED & LD LAB A1	
TUE						ED & LD LAB B1	
WED	ED						
THU		ED				ED & LD LAB B2	
FRI						ED	
SAT					ED		

LECTURE SCHEDULE: (2022-23)

LESSON PLAN (2022-23)

S.No	No.of Classes	Topics	Learning activities	Assessment methods
1	1	**Unit-1: Semiconductor Diode Characteristics**: Introduction to Semi conductor Materials	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
2	1	The p-n junction Diode, Energy band diagram	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz/Seminar
3	1	Current equations	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
4	1	V-I characteristics of PN Junction Diode, Temperature dependence	Chalk & Talk	Exam/Assignment/Quiz
5	1	Diode resistance-Static and Dynamic, Transition capacitance, Diffusion capacitance	Chalk & Talk,Student Seminars	Exam/Assignment/Quiz
6	2	Zener diode, Avalanche breakdown, Zener breakdown mechanisms	Chalk & Talk	Exam/Assignment/Quiz
7	2	Zener diode as voltage Regulator	Chalk & Talk	Exam/Assignment/Quiz
8	1	Hall effect, Problems on current equations	Chalk & Talk	Exam/Assignment/Quiz/Seminar
9	1	Revision of above topics with student participation with more with Ex	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
10	1	**Unit-II Diode Applications:** Diode as a circuit element, Clipping Circuits	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
11	1	Different type of Clipping Circuits design and operation	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz

12	1	clamping circuit theorem Clamping Circuits	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
13	1	Different type of Clamping Circuits design and operation	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
14	1	Half wave Rectifier construction and operation with performance characteristics- ripple factor calculations, and analysis	Chalk & Talk,Student Seminars	Exam/Assignment/Quiz
15	1	Full wave Rectifier construction and operation with performance characteristics- ripple factor calculations, and analysis	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
16	1	Bridge wave Rectifier construction and operation with performance characteristics- ripple factor calculations, and analysis	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
17	1	Filters (L, C, LC and CLC filters).	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
18	1	**Special Purpose Semi-Conductor Devices:** Silicon controlled rectifier (SCR) Construction and operation	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
19	1	Schottky diode, LED, Photodiode, Solar cell Construction and operation	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
20	1	Revision of above topics with student participation and seminars with more examples	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
21		**ASSIGNMENT-I**	Group Tasks/ Assignments	Exam/Assignment/Quiz
22	1	**Unit-III Bipolar Junction Transistor:** Construction and Operation of Bipolar Junction Transistor	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz/Seminar
23	1	current components of BJT	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
24	1	Modes of transistor operation of BJT, BJT input and output characteristics of CB Configuration	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz/Seminar

25	1	Early Effect, BJT input and output characteristics of CE Configuration	Chalk & Talk;Power point presentation by Students	Exam/Assignment/Quiz
26	1	BJT input and output characteristics of CC Configuration	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz/Seminar
27	1	**Biasing and Stabilization:** Biasing techniques**,** Thermal run away Stabilization factors	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
28	1	Stabilization factors	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
29	1	Various Compensation techniques, Thermal Stability	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
30	1	Revision of above topics with student participation with more examples	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
31	1	**Unit IV Small Signal Transistors equivalent circuits:-** Introduction to Z-parameters,	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
32	1	Introduction to Y-parameters,	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
33	1	Introduction to h-parameters,	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
34	1	Small signal low frequency h-parameter model of BJT.	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
35	1	Approximate model of BJT,	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
36	1	Analysis of BJT amplifiers using approximate model for CB.	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
37	1	Analysis of BJT amplifiers using approximate model for CE	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
38	1	Analysis of BJT amplifiers using approximate model for CC Configurations	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz

39	1	Revision of above topics with student participation	Chalk & Talk;Power point presentation by Students	Exam/Assignment/Quiz
40		**Assignment 2 in the form of PPT/DOC/PDF**	**Group Tasks/ Assignments**	Exam/Assignment/Quiz
41	1	**Unit V Field Effect Transistor** Junction Field Effect Transistor: Principle of Operation	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
42	1	the Pinch-off Voltage VP, V-I Characteristics of JFET	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
43	1	**MOSFETs:** Enhancement **MOSFET** Principle of Operation V-I characteristics	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
44	1	Depletion mode MOSFETs, Principle of Operation V-I characteristics	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
45	1	CMOS inverter	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
46	1	. Small signal model analysis for FET	Chalk & Talk; Power point presentation	Exam/Assignment/Quiz
47	1	Revision of above topics with student participation with more examples	Power point presentation; Video Lecture; Student seminar	Exam/Assignment/Quiz/Seminar
Total class	**47**			

SIGNATURE OF ACULTY

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INNOVATIVE TEACHING METHODS

1. Hands-on teaching method
2. ICT Enabling teaching: Use of information and communication technology to teach technical ideas. In this method we, integrate
3. Telecommunication, computers, relevant software and Audio –Visualization systems to handle the topics
4. Pee-to-peer teaching/Active teaching method: In this method students are really encouraged in the content by discussing the topics, generating questions and working in team to explore new information.
5. Power point (PPT) method: Instead of the conventional Chalk method, teaching now include PPT in their class room session to make it more interaction.
6. Field trip/Industry visit
7. Flipped classroom teaching method: students are asked to go through video instructions or tutorials in the initial stage (digital learning), in the second stage will be in classroom they involve in challenging tasks and assignments based on the information gathered through video assignments.
8. Mini-Projects: students to take part in hands-on activity inside the classrooms to illustrate a concept, build up the circuit, test for conditionality and solutions in model the information of topic.
9. Research Books method: teacher can promote the use of research books in classroom rather than just text books and lecture notes.
10. Real-world teaching method: Link the lessons or topics to real world learning. Infusing world experiences into instructions will make teaching moments fresh and enrich class learning, reality and demonstrating through real life situations.

TEACHING-LEARNING METHODOLOGY ADOPTED

1. Chalk and Talk
2. PPTs, Animations and Videos for illustrations
3. Learning by doing
4. Collaborative Learning (Think Pair Share)
5. Group Assignment – Project

METHOD OF ASSESSMENT OF COs and POs:

Cos	Relevant POs	Mode of Assessment
ES214.1-ES214.6	PO1: ENGINEERING KNOWLEDGE PO2: PROBLEM ANALYSIS PO3: DESIGN/ DEVELOPMENT OF SOLUTIONS PO4: CONDUCT INVESTIGATION ON COMPLEX PROBLEMS PSO1: PROFESSIONAL COMPETENCE	Assignments, Quizzes, Internal Examinations and External Examination result
ES214.1-ES214.6	PO5: MODERN TOOL USAGE	Exercises to learn through Nptel videos and internet websites, Usage of Excel worksheets for problem solving
ES214.1-ES214.6	PO8: ETHICS	Assignments, Quizzes
ES214.1-ES214.6	PO9: IINDIVIDUAL AND TEAM WORK PO10: COMMUNICATION	Group Assignments, Writing skills in documenting assignments, Presentations

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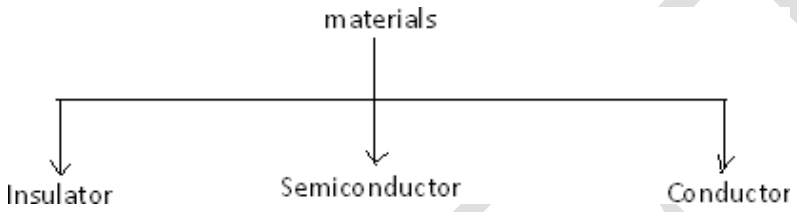
UNIT-I

PN JUNCTION DIODE

INTRODUCTON

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.

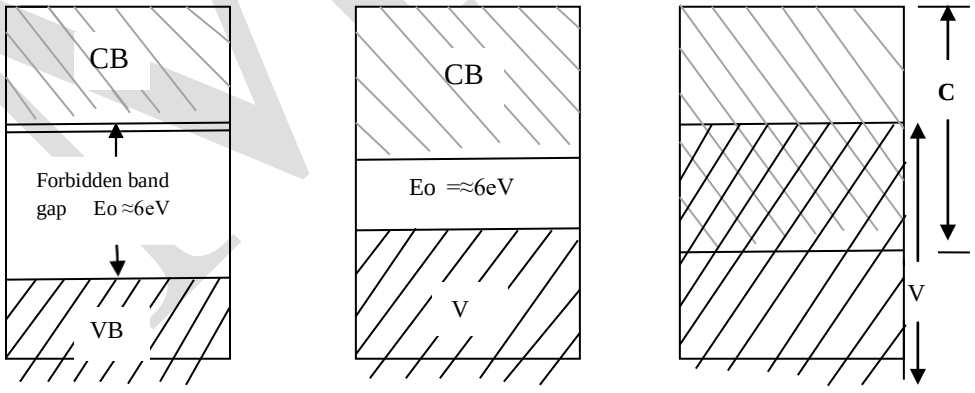


Insulator: An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Eg: Paper, Mica, glass, quartz. Typical resistivity level of an insulator is of the order of 10^{10} to 10^{12} Ω-cm. The energy band structure of an insulator is shown in the fig.1.1. Band structure of a material defines the band of energy levels that an electron can occupy. Valance band is the range of electron energy where the electron remain bended too the atom and do not contribute to the electric current. Conduction bend is the range of electron energies higher than valance band where electrons are free to accelerate under the influence of external voltage source resulting in the flow of charge.

The energy band between the valance band and conduction band is called as forbidden band gap. It is the energy required by an electron to move from balance band to conduction band i.e. the energy required for a valance electron to become a free electron.

$$1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$$

For an insulator, as shown in the fig.1.1 there is a large forbidden band gap of greater than 5Ev. Because of this large gap there a very few electrons in the CB and hence the conductivity of insulator is poor. Even an increase in temperature or applied electric field is insufficient to transfer electrons from VB to CB.



Insulator Semiconductor Conductor

FiG:1.1 Energy band diagrams insulator, semiconductor and conductor

Conductors: A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity. Eg: Copper, Aluminum, Silver, Gold. The resistivity of a conductor is in the order of 10^{-4} and 10^{-6} **Ω**-cm. The Valance and conduction bands overlap (fig1.1) and there is no energy gap for the electrons to move from valance band to conduction band. This implies that there are free electrons in CB even at absolute zero temperature (0K). Therefore at room temperature when electric field is applied large current flows through the conductor.

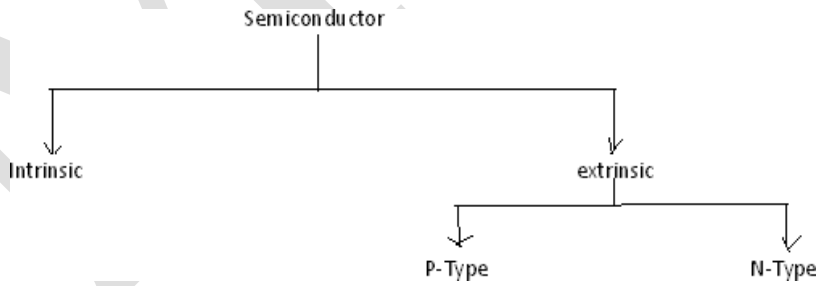
Semiconductor: A semiconductor is a material that has its conductivity somewhere between the insulator and conductor. The resistivity level is in the range of 10 and 10^4 **Ω**-cm. Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons. The forbidden band gap is in the order of 1eV. For eg., the band gap energy for Si, Ge and GaAs is 1.21, 0.785 and 1.42 eV, respectively at absolute zero temperature (0K). At 0K and at low temperatures, the valance band electrons do not have sufficient energy to move from V to CB. Thus semiconductors act a insulators at 0K. as the temperature increases, a large number of valance electrons acquire sufficient energy to leave the VB, cross the forbidden bandgap and reach CB. These are now free electrons as they can move freely under the influence of electric field. At room temperature there are sufficient electrons in the CB and hence the semiconductor is capable ofconducting some current at room temperature.

Inversely related to the conductivity of a material is its resistance to the flow of charge or current. Typical resistivity values for various materials' are given as follows.

Insulator	Semiconductor	Conductor
10^{-6} Ω-cm (Cu)	50Ω-cm (Ge)	10^{12} Ω-cm (mica)
	$50x10^3$ Ω-cm (Si)	

Typical resistivity values

Semiconductor Types



A pure form of semiconductors is called as intrinsic semiconductor. Conduction in intrinsic sc is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used. Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.

Let us consider the structure of Si. A Si atomic no. is 14 and it has 4 valance electrons. These 4 electrons are shared by four neighboring atoms in the crystal structure by means of covalent bond. Fig. 1.2a shows the crystal structure of Si at absolute zero temperature (0K). Hence a pure SC acts has poor conductivity (due to lack of free electrons) at low or absolute zero temperature.

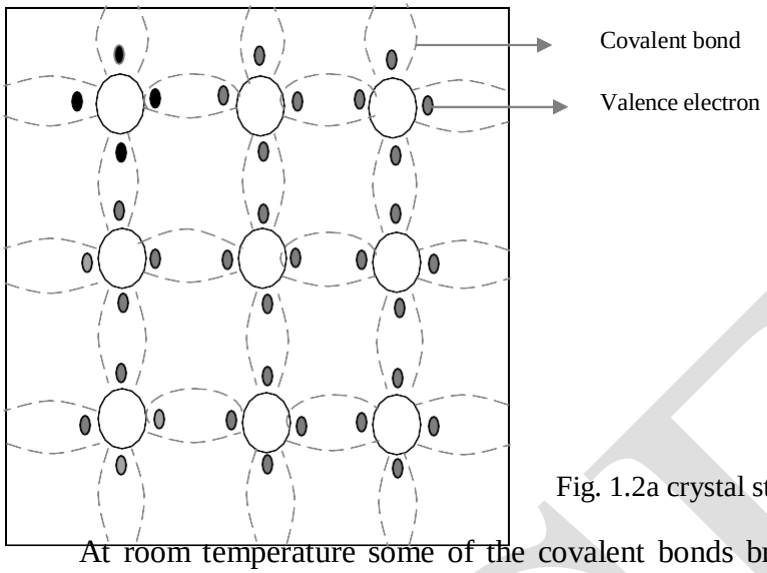


Fig. 1.2a crystal structure of Si at 0K

At room temperature some of the covalent bonds break up to thermal energy as shown in fig 1.2b. The valance electrons that jump into conduction band are called as free electrons that are available for conduction.

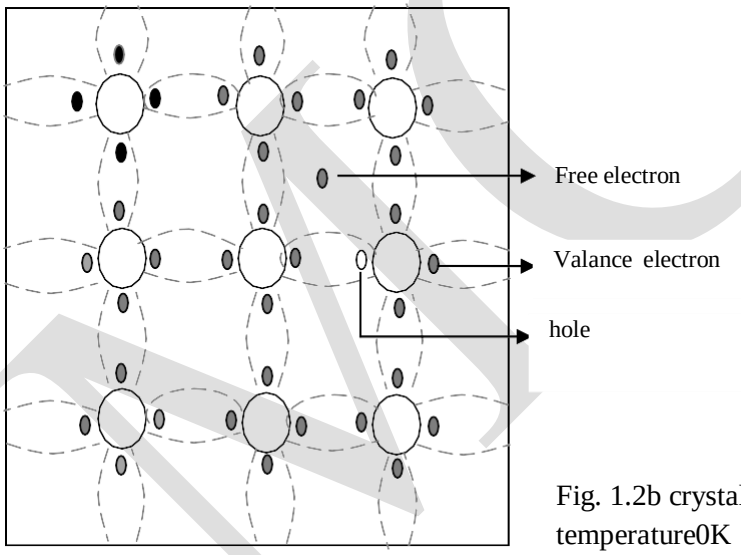


Fig. 1.2b crystal structure of Si at room temperature0K

The absence of electrons in covalent bond is represented by a small circle usually referred to as hole which is of positive charge. Even a hole serves as carrier of electricity in a manner similar to that of free electron.

The mechanism by which a hole contributes to conductivity is explained as follows:

When a bond is in complete so that a hole exists, it is relatively easy for a valance electron in the neighboring atom to leave its covalent bond to fill this hole. An electron moving from a bond to fill a hole moves in a direction opposite to that of the electron. This hole, in its new position may now be filled by an electron from another covalent bond and the hole will correspondingly move one more step in the direction opposite to the motion of electron. Here we have a mechanism for conduction of electricity which does not involve free electrons. This phenomenon is illustrated in fig1.3

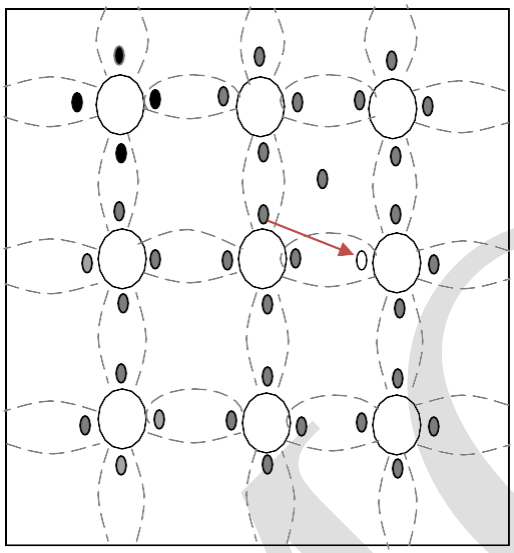


Fig. 1.3a

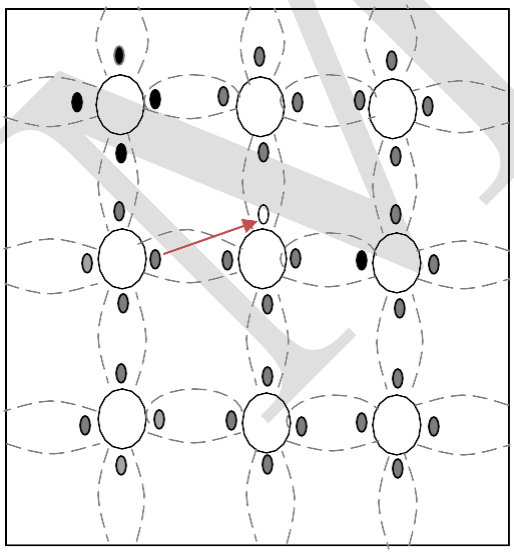


Fig. 1.3b

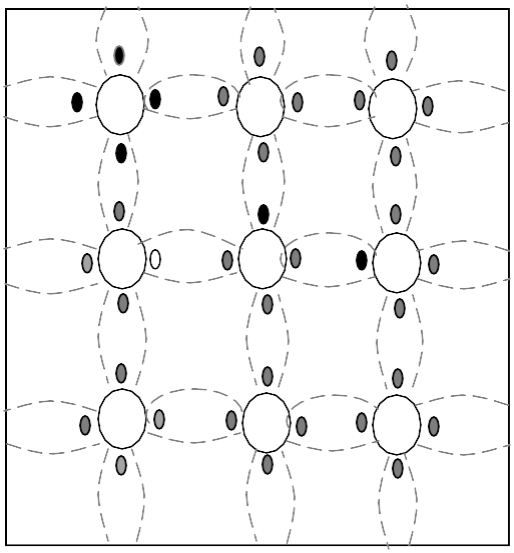


Fig. 1.3c

Fig 1.3a show that there is a hole at ion 6.Imagine that an electron from ion 5 moves into the hole at ion 6 so that the configuration of 1.3b results. If we compare both fig1.3a &fig 1.3b, it appears as if the hole has moved towards the left from ion6 to ion 5. Further if we compare fig 1.3b and fig 1.3c, the hole moves from ion5 to ion 4. This discussion indicates the motion of hole is in a direction opposite to that of motion of electron. Hence we consider holes as physical entities whose movement constitutes flow of current.

In a pure semiconductor, the number of holes is equal to the number of free electrons.

EXTRINSIC SEMICONDUCTOR

Intrinsic semiconductor has very limited applications as they conduct very small amounts of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor. By adding impurities it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping. The amount of impurity added is 1 part in 10^6 atoms.

N type semiconductor: If the added impurity is a pentavalent atom then the resultant semiconductoris called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.

A pentavalent impurity has five valance electrons. Fig 1.4a shows the crystal structure of N-type semiconductor material where four out of five valance electrons of the impurity atom(antimony) forms covalent bond with the four intrinsic semiconductor atoms. The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily

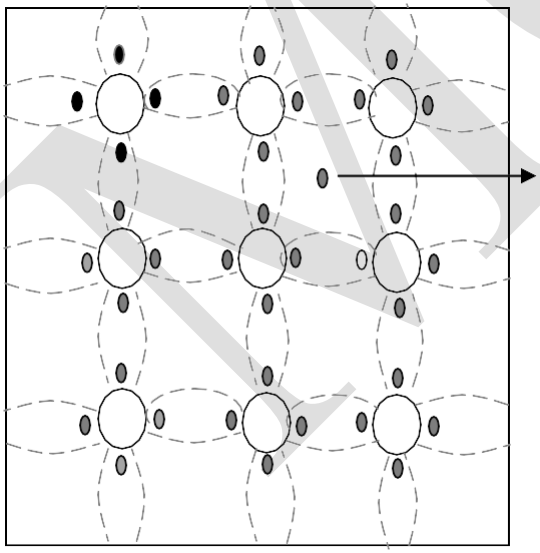


Fig. 1.4a crystal structure of N type SC

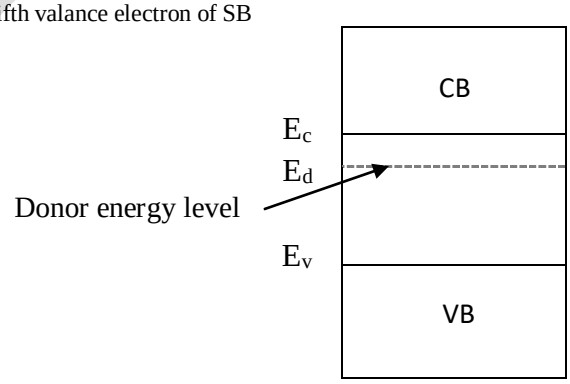


Fig. 1.4bEnergy band diagram of N type

Excited from the valance band to the conduction band by the application of electric field or increasing the thermal energy. The energy required to detach the fifth electron form the impurity atom is very small of the order of 0.01ev for Ge and 0.05 eV for Si.

The effect of doping creates a discrete energy level called donor energy level in the forbidden band gap with energy level E_d slightly less than the conduction band (fig 1.4b). The difference between the energy levels of the conducting band and the donor energy level is the energy required to free the fifth valance electron (0.01 eV for Ge and 0.05 eV for Si). At room temperature almost all the fifth electrons from the donor impurity atom are raised to conduction band and hence the number of electrons in the conduction band increases significantly. Thus every antimony atom contributes to one conduction electron without creating a hole.

In the N-type sc the no. of electrons increases and the no. of holes decreases compared to those available in an intrinsic sc. The reason for decrease in the no. of holes is that the larger no. of electrons present increases the recombination of electrons with holes. Thus current in N type sc is dominated by electrons which are referred to as majority carriers. Holes are the minority carriers in N type sc

P type semiconductor: If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium , indium etc.

The crystal structure of p type sc is shown in the fig1.5a. The three valance electrons of the impurity (boon) forms three covalent bonds with the neighboring atoms and a vacancy exists in the fourth bond giving rise to the holes. The hole is ready to accept an electron from the neighboring atoms. Each trivalent atom contributes to one hole generation and thus introduces a large no. of holes in the valance band. At the same time the no. electrons are decreased compared to those available in intrinsic sc because of increased recombination due to creation of additional holes.

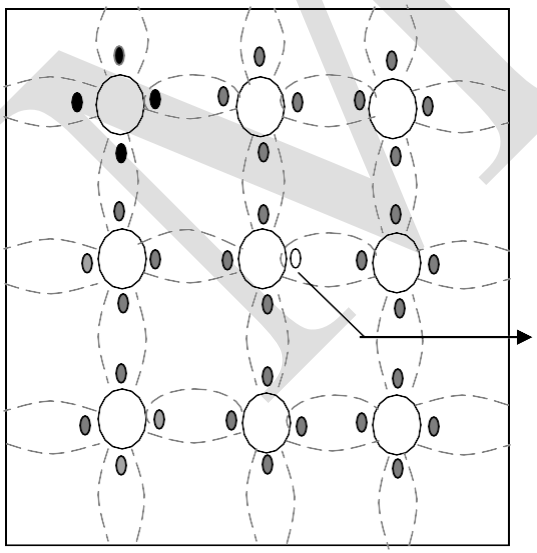


Fig. 1.5a crystal structure of P type sc

Thus in P type sc , holes are majority carriers and electrons are minority carriers. Since each trivalent impurity atoms are capable accepting an electron, these are called as acceptor atoms. The following fig 1.5b shows the pictorial representation of P type sc

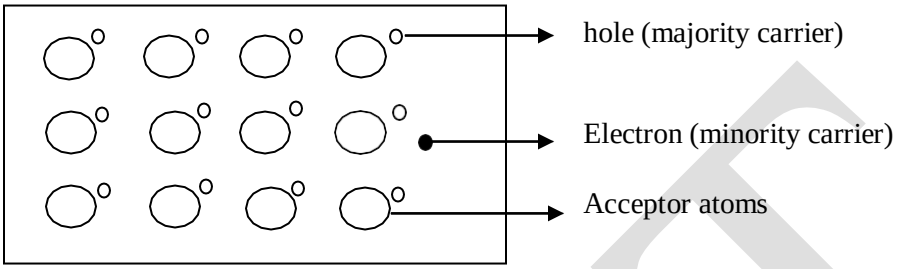


Fig. 1.5b crystal structure of P type sc

- The conductivity of N type sc is greater than that of P type sc as the mobility of electron is greater than that of hole.
- For the same level of doping in N type sc and P type sc, the conductivity of an Ntype sc is around twice that of a P type sc

CONDUCTIVITY OF SEMICONDUCTOR

In a pure sc, the no. of holes is equal to the no. of electrons. Thermal agitation continue to produce new electron- hole pairs and the electron hole pairs disappear because of recombination. with each electron hole pair created , two charge carrying particles are formed . One is negative which is a free electron with mobility μ_n . The other is a positive i.e., hole with mobility μ_p . The electrons and hole move in opppsitte direction in a an electric field E, but since they are of opposite sign, the current due to each is in the same direction. Hence the total current density J within the intrinsic sc is given by

$J = J_n + J_p$

$=q\, n\, \mu_n E + q\, p\, \mu_p E$

$= (n\, \mu_n + p\, \mu_p) qE$

$=\varsigma E$

Where n=no. of electrons / unit volume i.e., concentration of free electronsP=

no. of holes / unit volume i.e., concentration of holes

E=applied electric field strength, V/m

q= charge of electron or hole I n Coulombs

Hence, ς is the conductivity of sc which is equal to (n μ_n + p μ_p)q. he resistivity of sc is reciprocalof conductivity.

P = 1/ ς

It is evident from the above equation that current density with in a sc is directly proportional to applied electric field E.

For pure sc, n=p= n_i where n_i = intrinsic concentration. The value of n_i is given

by $n_i^2 = AT^3 \exp(-E/KT)$

therefore, J= n_i (μ_n + μ_p) q E

Hence conductivity in intrinsic sc is $\varsigma_i = n_i (\mu_n + \mu_p) q$

Intrinsic conductivity increases at the rate of 5% per ^{o} C for Ge and 7% per ^{o} C for Si.

Conductivity in extrinsic sc (N Type and P Type):

The conductivity of intrinsic sc is given by $\varsigma_i = n_i (\mu_n + \mu_p) q = (n \mu_n + p \mu_p)q$For N type , n>>p

Therefore $\varsigma = q n \mu_n$

For P type ,p>>n

Therefore $\varsigma = q p \mu_p$

CHARGE DENSITIES IN P TYPE AND N TYPE SEMICONDUCTOR:

Mass Action Law:

Under thermal equilibrium for any semiconductor, the product of the no. of holes and the concentration of electrons is constant and is independent of amount of donor and acceptor impurity doping.

$n.p = n_i^2$

where n= eleetron concentration p

= hole concentration n_i^2=

intrinsic concentration

Hence in N type sc , as the no. of electrons increase the no. of holes decreases. Similarly in P type as the no. of holes increases the no. of electrons decreases. Thus the product is constant and is equal to n_i^2 in case of intrinsic as well as extrinsic sc.

The law of mass action has given the relationship between free electrons concentration and hole concentration. These concentrations are further related by the law of electrical neutrality as explained below.

Law of electrical neutrality:

Sc materials are electrically neutral. According to the law of electrical neutrality, in an electrically neutral material, the magnitude of positive charge concentration is equal to tat of negative charge concentration. Let us consider a sc that has N_D donor atoms per cubic centimeter and N_A acceptor atoms per cubic centimeter i.e., the concentration of donor and acceptor atoms are N_D and N_A respectively. Therefore N_D positively charged ions per cubic centimeter are contributed by donor atoms and N_A negatively charged ions per cubic centimeter are contributed by the acceptor atoms. Let n, p is concentration of free electrons and holes respectively. Then according to the law of neutrality

$N_D + p = N_A + n$ ..... eq 1.1

For N type sc, $N_A = 0$ and $n >> p$. Therefore $N_D \approx n$ ..... eq 1.2

Hence for N type sc the free electron concentration is approximately equal to the concentration of donor atoms. In later applications since some confusion may arise as to which type of sc is under consideration a the given moment, the subscript n or p is added for Ntype or P type respectively. Hence eq1.2 becomes $N_D \approx n_n$

Therefore current density in N type sc is $J = N_D \mu_n q$

EAnd conductivity $\varsigma = N_D \mu_n q$

For P type sc, $N_D = 0$ and $p >> n$. Therefore $N_A \approx p$

Or $N_A \approx p_p$

Hence for P type sc the hole concentration is approximately equal to the concentration ofacceptor atoms.

Therefore current density in N type sc is $J = N_A \mu_p q$

EAnd conductivity $\varsigma = N_A \mu_p q$

Mass action law for N type, $n_n p_n = n_i^2$

$p_n = n_i^2 / N_D$ since $(n_n \approx N_D)$

Mass action law for P type, $n_p\ p_p = n_i^2$

$$n_p = n_i^2 / N_A \quad \text{since } (p_p \approx N)$$

QUANTITATIVE THEORY OF PN JUNCTION DIODE

PN JUNCTION WITH NO APPLIED VOLTAGE OR OPEN CIRCUIT CONDITION:

In a piece of sc, if one half is doped by p type impurity and the other half is doped by n type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. As shown in the fig the n type material has high concentration of free electrons, while p type material has high concentration of holes. Therefore at the junction there is a tendency of free electrons to diffuse over to the P side and the holes to the N side. This process is called diffusion. As the free electrons move across the junction from N type to P type, the donor atoms become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filing the holes. Therefore a negative charge is developed on the p –side of the junction..This net negative charge on the p side prevents further diffusion of electrons into the p side. Similarly the net positive charge on the N side repels the hole crossing from p side to N side. Thus a barrier sis set up near the junction which prevents the further movement of charge carriers i.e. electrons and holes. As a consequence of induced electric field across the depletion layer, an electrostatic potential difference is established between P and N regions, which are called the potentialbarrier, junction barrier, diffusion potential or contact potential, Vo. The magnitude of the contact potential Vo varies with doping levels and temperature. Vo is 0.3V for Ge and 0.72 V for Si.

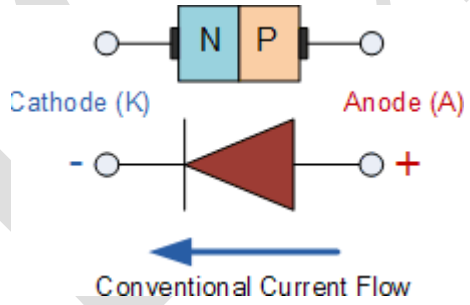


Fig 1.6: Symbol of PN Junction Diode

The electrostatic field across the junction caused by the positively charged N-Type region tends to drive the holes away from the junction and negatively charged p type regions tend to drive the electrons away from the junction. The majority holes diffusing out of the P region leave behind negatively charged acceptor atoms bound to the lattice, thus exposing a negatives pace charge in a previously neutral region. Similarly electrons diffusing from the N region expose positively ionized donor atoms and a double space charge builds up at the junction as shown in the fig. 1.7a

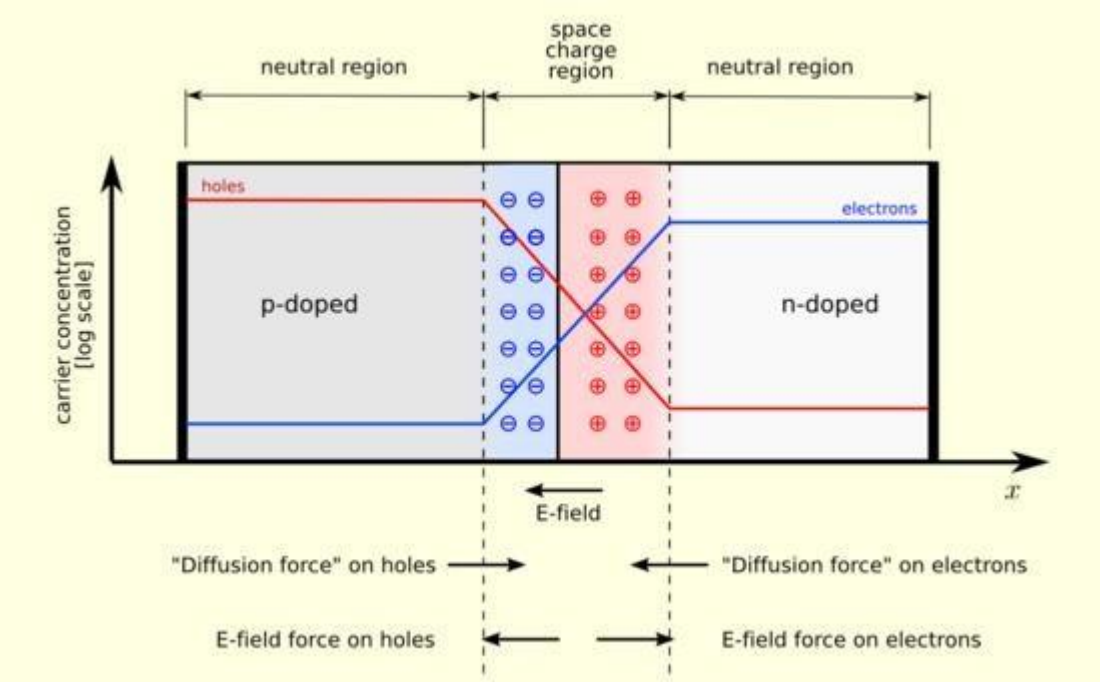


Fig 1.7a

It is noticed that the space charge layers are of opposite sign to the majority carriers diffusing into them, which tends to reduce the diffusion rate. Thus the double space of the layer causes an electric field to be set up across the junction directed from N to P regions, which is in such a directionto inhibit the diffusion of majority electrons and holes as illustrated in fig 1.7b. The shape of the chargedensity, ρ, depends upon how diode id doped. Thus the junction region is depleted of mobile charge carriers. Hence it is called depletion layer, space region, and transition region. The depletion region isof the order of 0.5μm thick. There are no mobile carriers in this narrow depletion region. Hence no current flows across the junction and the system is in equilibrium. To the left of this depletion layer, the carrier concentration is p= N_A and to its right it is n= N_D.

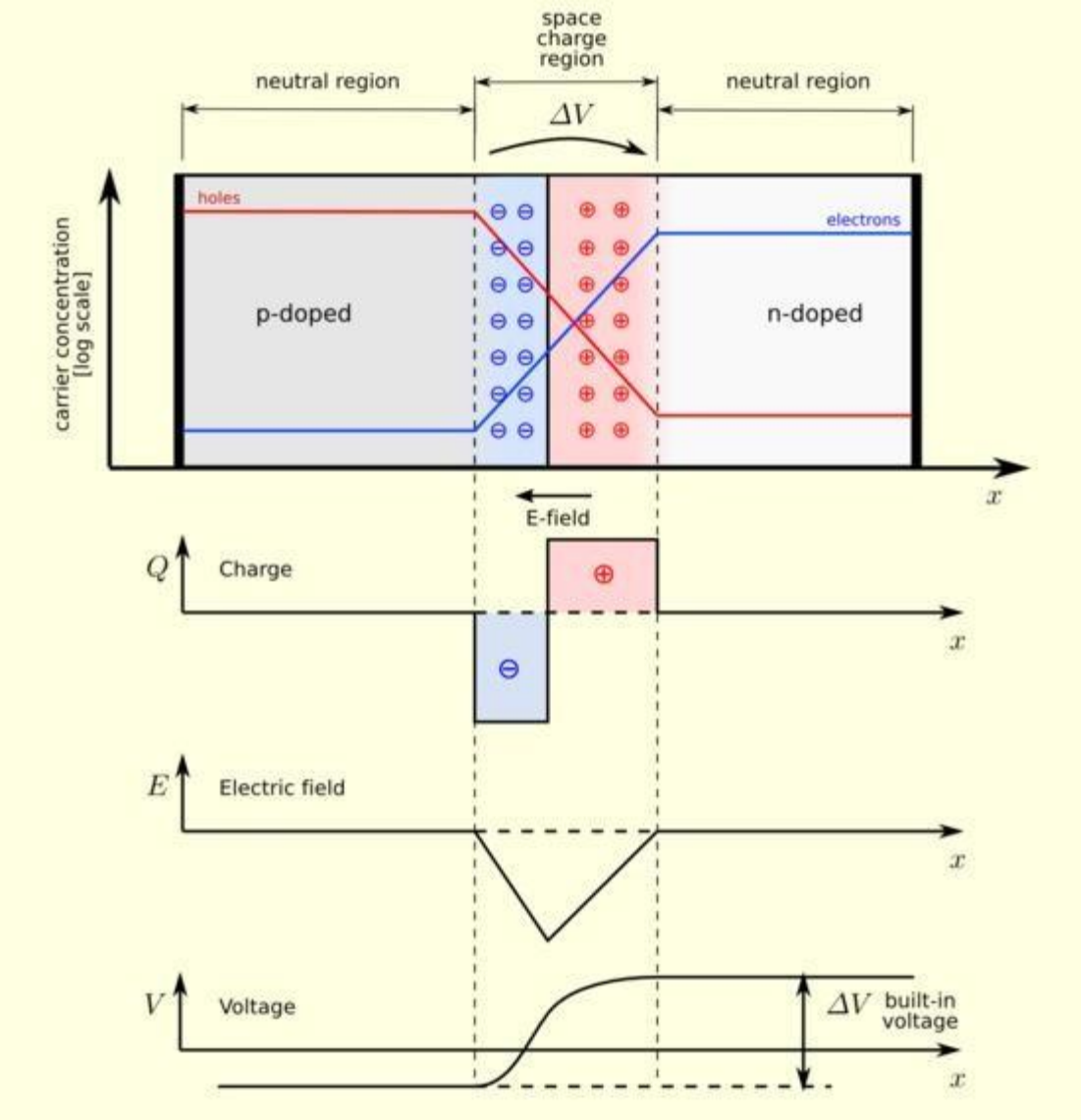


Fig 1.7b

FORWARD BIASED JUNCTION DIODE

When a diode is connected in a **Forward Bias** condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow. This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point,

called the "knee" on the static curves and then a high current flow through the diode with littleincrease in the external voltage as shown below.

Forward Characteristics Curve for a Junction Diode

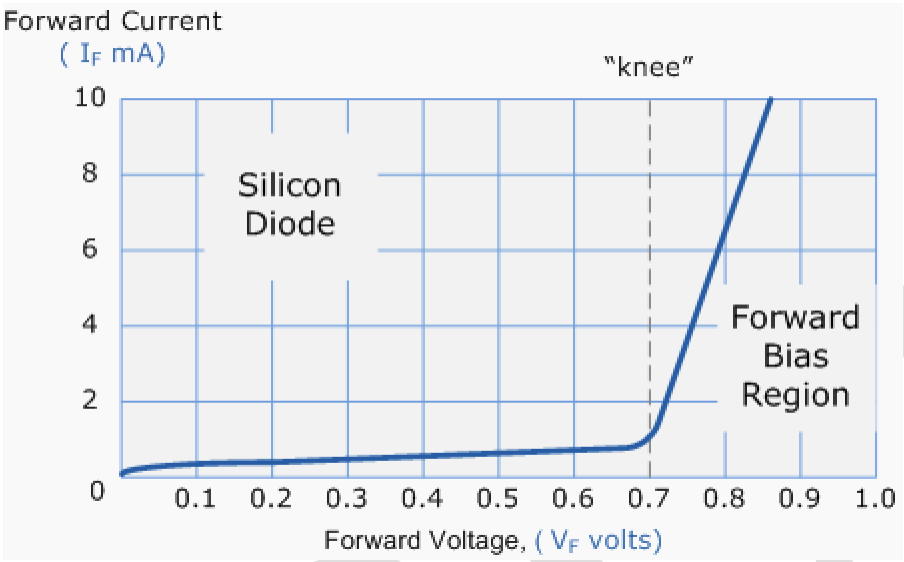


Fig 1.8a: Diode Forward Characteristics

The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow. The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.

Forward Biased Junction Diode showing a Reduction in the Depletion Layer

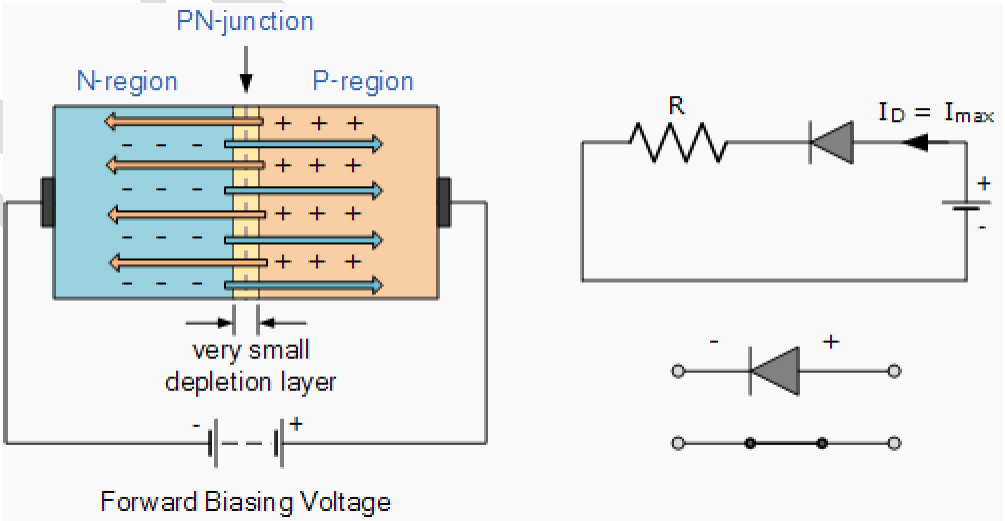


Fig 1.8b: Diode Forward Bias

This condition represents the low resistance path through the PN junction allowing very large currents to flow through the diode with only a small increase in bias voltage. The actual potential difference across the junction or diode is kept constant by the action of the depletion layer at approximately 0.3v for germanium and approximately 0.7v for silicon junction diodes. Since the diode can conduct "infinite" current above this knee point as it effectively becomes a short circuit, therefore resistors are used in series with the diode to limit its current flow. Exceeding its maximum forward current specification causes the device to dissipate more power in the form of heat than it was designed for resulting in a very quick failure of the device.

1.1.2 PN JUNCTION UNDER REVERSE

BIAS CONDITION:Reverse Biased

Junction Diode

When a diode is connected in a **Reverse Bias** condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode. The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

Reverse Biased Junction Diode showing an Increase in the Depletion

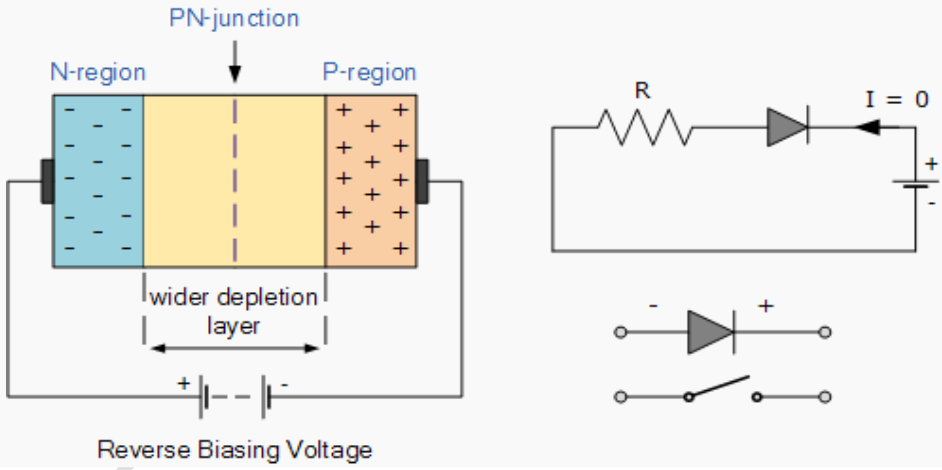


Fig 1.9a: Diode Reverse Bias

This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in microamperes, (μA). One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will

cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve below.

Reverse Characteristics Curve for a Junction Diode

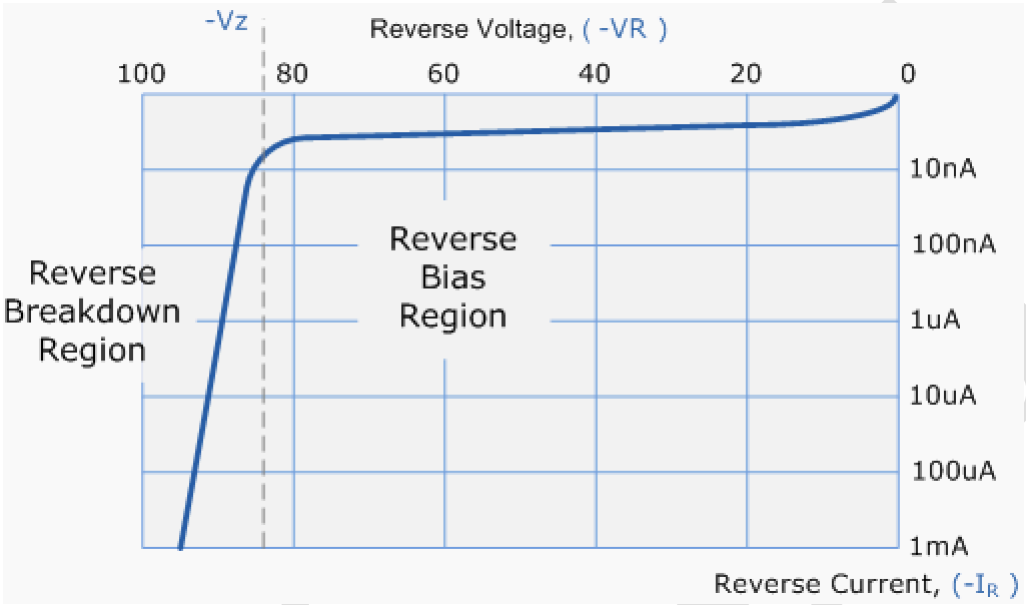


Fig 1.9b: Diode Reverse Characteristics

Sometimes this avalanche effect has practical applications in voltage stabilizing circuits where a series limiting resistor is used with the diode to limit this reverse breakdown current to a preset maximum value thereby producing a fixed voltage output across the diode. These types of diodes are commonly known as **Zener Diodes**

VI CHARACTERISTICS AND THEIR TEMPERATURE DEPENDENCE

Diode terminal characteristics equation for diode junction current:

$$I_D = I_o(e^{\frac{v}{\eta v_T}} - 1)$$

Where V_T = KT/q;

V_D_ diode terminal voltage, Volts

I_o _ temperature-dependent saturation current, µAT

_ absolute temperature of p-n junction, K

K _ Boltzmann's constant 1.38x 10 -

23J/K)q _ electron charge 1.6x10-19 C

η = empirical constant, 1 for Ge and 2 for Si

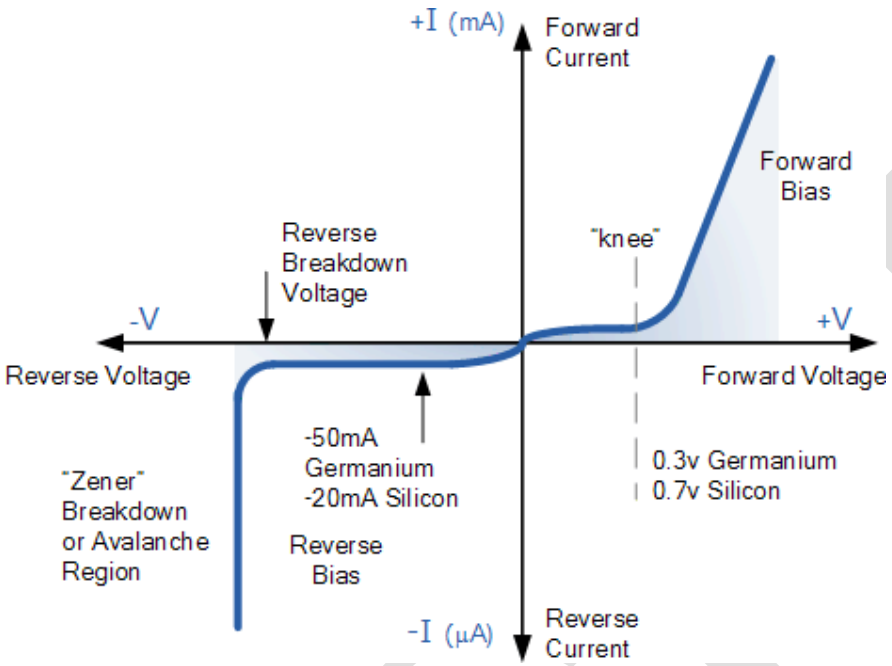


Fig 1.10: Diode Characteristics

Temperature Effects on Diode

Temperature can have a marked effect on the characteristics of a silicon semiconductor diodeas shown in Fig. 11 It has been found experimentally that the reverse saturation current Io will just about double in magnitude for every 10°C increase in temperature.

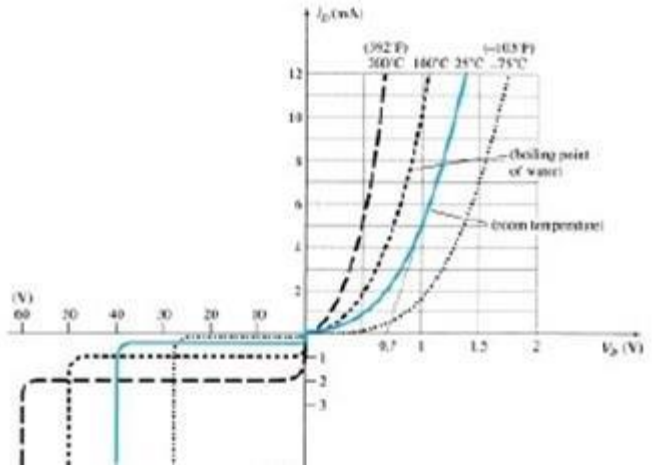


Fig 1.11 Variation in Diode Characteristics with temperature change

It is not uncommon for a germanium diode with an I_o in the order of 1 or 2 A at 25°C to have a leakage current of 100 A - 0.1 mA at a temperature of 100°C. Typical values of I_o for silicon are much lower thanthat of germanium for similar power and current levels. The result is that even at high temperatures the levels of I_o for silicon diodes do not reach the same high levels obtained. For germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium. The increasing levels of I_o with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.11. Simply increase the level of I_o in and notrise in diode current. Of course, the level of TK also will be increase, but the increasing level of I_o will overpower the smaller percent change in TK. As the temperature increases the forward characteristics are actually becoming more "ideal,"

IDEAL VERSUS PRACTICAL RESISTANCE LEVELS

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of VD and ID as shown in Fig. 1.12 and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

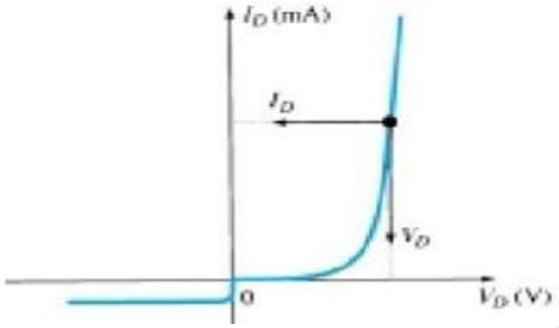


Fig 1.12 Determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

It is obvious from Eq. 1.3 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.13. With no applied varying signal, the point of operation would be the Q-point appearing on Fig. 1.13 determined by the applied dc levels. The designation Q-point is derived from the word quiescent, which means "still or unvarying." A straight-line drawn tangent to the curve through the Q-point as shown in Fig. 1.13 will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

Where Δ Signifies a finite change in the quantity

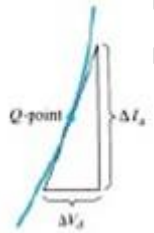


Fig 1.13: Determining the ac resistance of a diode at a particular operating point.

DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region. In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open- circuit state for the device. Since a silicon semiconductor, diode does not reach the conduction state until VD reaches 0.7 V with a forward bias (as shown in Fig. 1.14a), a battery V_T opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.14b. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established, the resistance of the diode will be the specified value of r_{av}.

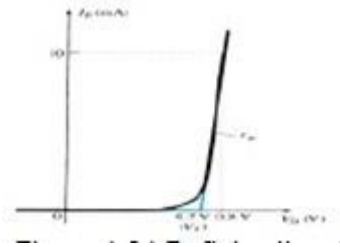


Fig: 1.14aDiode piecewise-linear model characteristics

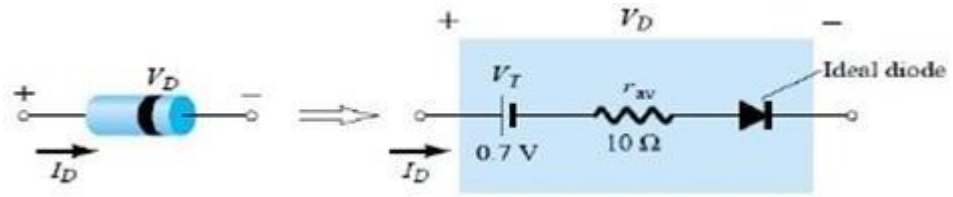


Fig: 1.14b Diode piecewise-linear model equivalent circuit

The approximate level of r_{av} can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if IF _ 10 mA (a forward conduction current for the diode) at VD _ 0.8 V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

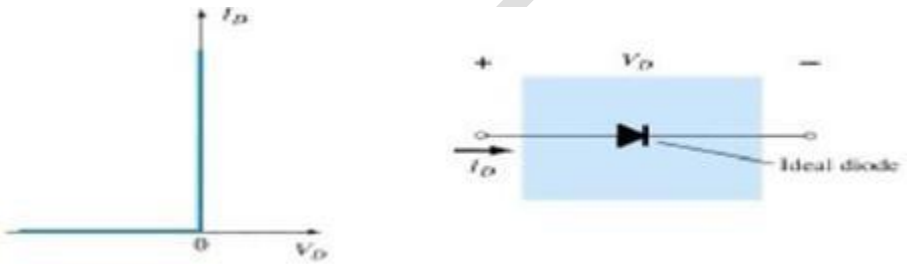


Fig 1.15 Ideal Diode and its characteristics

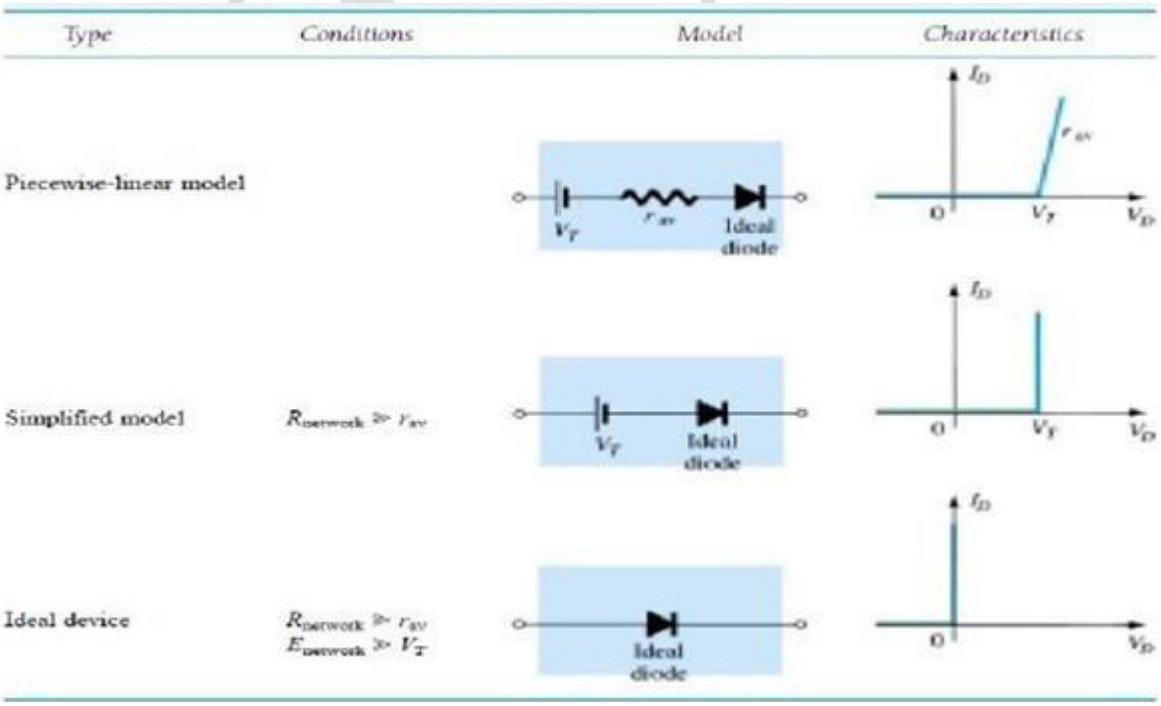


Fig 1.16: Diode equivalent circuits(models)

TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance XC=1/2πfC is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. XC will become sufficiently small due to the high value of f to introduce a low-reactance "shorting" path. In the p-n semiconductor diode, there are two capacitive effects to be considered. In the reverse-bias region we have the transition- or depletion region capacitance (CT), while in the forward-bias region we have the diffusion (CD) or storage capacitance. Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by C=€A/d, where € is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-, bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. Although the effect described above will also be present in the forward-bias region, it is over shadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

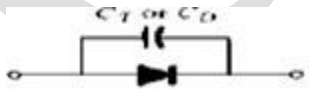


Fig 1.17: Including the effect of the transition or diffusion capacitance on the semiconductor diode

Diode capacitances: The diode exhibits two types of capacitances transition capacitance and diffusion capacitance.

- Transition capacitance: The capacitance which appears between positive ion layer in n-region and negative ion layer in p-region.
- Diffusion capacitance: This capacitance originates due to diffusion of charge carriers in the opposite regions.

The transition capacitance is very small as compared to the diffusion capacitance.

In reverse bias transition, the capacitance is the dominant and is given by:

$$C_T = \epsilon A/W$$

where C_T - transition capacitance

A - diode cross sectional area

W - depletion region width

In forward bias, the diffusion capacitance is the dominant and is given by:

$$C_D = dQ/dV = \tau^* dI/dV = \tau^* g = \tau/r \text{ (general)}$$

where C_D - diffusion capacitance

dQ - change in charge stored in depletion region

V - change in applied voltage

τ - time interval for change in voltage

g - diode conductance

r - diode resistance

The diffusion capacitance at low frequencies is given by the formula:

$$C_D = \tau^* g/2 \text{ (low frequency)}$$

The diffusion capacitance at high frequencies is inversely proportional to the frequency and is given by the formula:

$$C_D = g(\tau/2\omega)^{1/2}$$

Note: The variation of diffusion capacitance with applied voltage is used in the design of varactor.

BREAK DOWN MECHANISMS

When an ordinary **P-N junction diode** is reverse biased, normally only very small reverse saturation current flows. This current is due to movement of minority carriers. It is almost independent of the voltage applied. However, if the reverse bias is increased, a point is reached when the junction breaks down and the reverse current increases abruptly. This current could be large enough to destroy the junction. If the reverse current is limited by means of a suitable series resistor, the power dissipation at the junction will not be excessive, and the device may be operated continuously in its

breakdown region to its normal (reverse saturation) level. It is found that for a suitably designed diode, the breakdown voltage is very stable over a wide range of reverse currents. This quality gives the breakdown diode many useful applications as a voltage reference source.

The critical value of the voltage, at which the breakdown of a P-N junction diode occurs, is called the *breakdown voltage*. The breakdown voltage depends on the width of the depletion region, which, in turn, depends on the doping level. The junction offers almost zero resistance at the breakdown point.

There are two mechanisms by which breakdown can occur at a reverse biased P-N junction:

1. avalanche breakdown *and*
2. ***Zener breakdown.***

Avalanche breakdown

The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. The breakdown region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.

Zener breakdown

Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect. The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3×10^7 V/m.

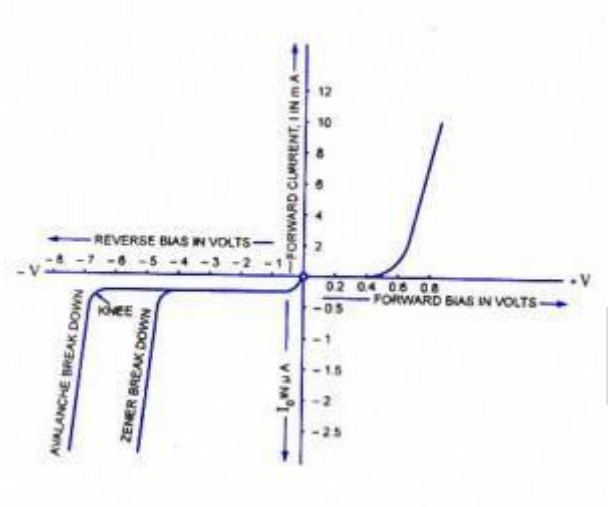


Fig 1.18: Diode characteristics with breakdown

Either of the two (Zener breakdown or avalanche breakdown) may occur independently, or both of these may occur simultaneously. Diode junctions that breakdown below 5 V are caused by Zener effect. Junctions that experience breakdown above 5 V are caused by avalanche effect. Junctions that breakdown around 5 V are usually caused by combination of two effects. The Zener breakdown occurs in heavily doped junctions (P-type semiconductor moderately doped and N-type heavily doped), which produce narrow depletion layers. The avalanche breakdown occurs in lightly doped junctions, which produce wide depletion layers. With the increase in junction temperature Zener breakdown voltage is reduced while the avalanche breakdown voltage increases. The Zener diodes have a negative temperature coefficient while avalanche diodes have a positive temperature coefficient. Diodes that have breakdown voltages around 5 V have zero temperature coefficient. The breakdown phenomenon is reversible and harmless so long as the safe operating temperature is maintained.

ZENER DIODES

The **Zener diode** is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage V_B is reached at which point a process called *Avalanche Breakdown* occurs in the semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.

The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achieved this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, V_B is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific *zener breakdown voltage*, (V_Z) for example, 4.3V or 7.5V. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

Zener Diode I-V Characteristics

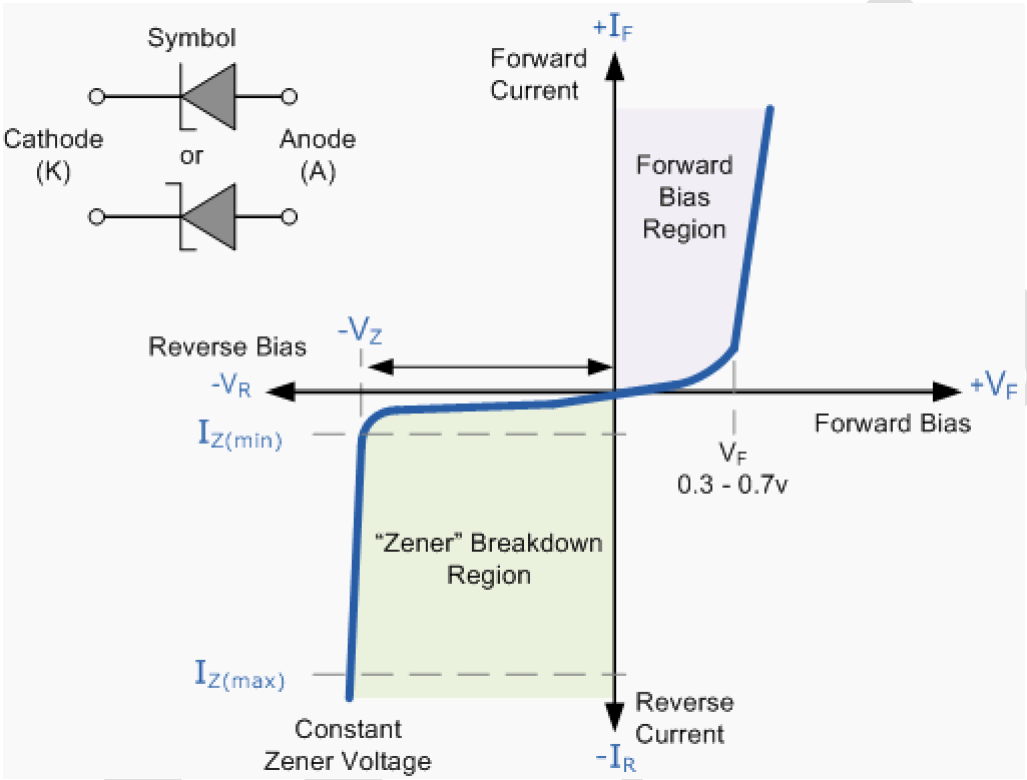


Fig 1.19 : Zener diode characteristics

The **Zener Diode** is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current $I_{Z(min)}$ and the maximum current rating $I_{Z(max)}$.

This ability to control itself can be used to great effect to regulate or stabilize a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator. The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will

Continue to regulate the voltage until the diodes current falls below the minimum $I_{Z(min)}$ value in the reverse breakdown region.

UNIT-II

DIODE APPLICATIONS

NON LINEAR WAVESHAPING

……

Diode clippers, Transistor clippers, clipping at two independent levels, Transfer characteristics of clippers, Emitter coupled clipper, Comparators, applications of voltage comparators, clamping operation, clamping circuits using diode with different inputs, Clamping circuit theorem, practical clamping circuits, effect of diode characteristics on clamping voltage, Transfer characteristics of clampers.

……

In the previous chapter we discussed about linear wave shaping. We saw how a change of wave shape was brought about when a non-sinusoidal signal is transmitted through a linear network like *RC* low pass and high pass circuit. In this chapter, we discuss some aspects of nonlinear wave shaping like clipping and clamping. The circuits for which the outputs are non-sinusoidal for sinusoidal inputs are called nonlinear wave shaping circuits, for example clipping circuits and clamping circuits.

Clipping means cutting and removing a part. A clipping circuit is a circuit which removes the undesired part of the waveform and transmits only the desired part of the signal which is above or below some particular reference level, i.e. it is used to select for transmission that part of an arbitrary waveform which lies above or below some particular reference. Clipping circuits are also called *voltage* (or current) *limiters, amplitude selectors* or *slicers.*

Nonlinear wave shaping circuits may be classified as clipping circuits and clamping circuits. Clipping circuits may be single level clippers or two level clippers.

Single level clippers may be series diode clippers with and without reference or shunt diode clippers with and without reference. Clipping circuits may use diodes or transistors.

Clamping circuits may be negative clampers (positive peak clampers) with and without reference or positive clampers (negative peak clampers) with and without reference.

CLIPPING CIRCUITS

In general, there are three basic configurations of clipping circuits.

A series combination of a diode, a resistor and a reference voltage.

A network consisting of many diodes, resistors and reference voltages.

Two emitter coupled transistors operating as a differential amplifier.

Diode Clippers

Figure 2.1(a) shows the v-i characteristic of a practical diode. Figures 2.1(b), (c), (d), and

show the *v-i* characteristics of an idealized diode approximated by a curve which is piece-wise linear and continuous. The break point occurs at *Vr*, where *Vr* = 0.2 V for Ge and Vr = 0.6 V for Si. Usually Vr is very small compared to the reference voltage VR and can be neglected.

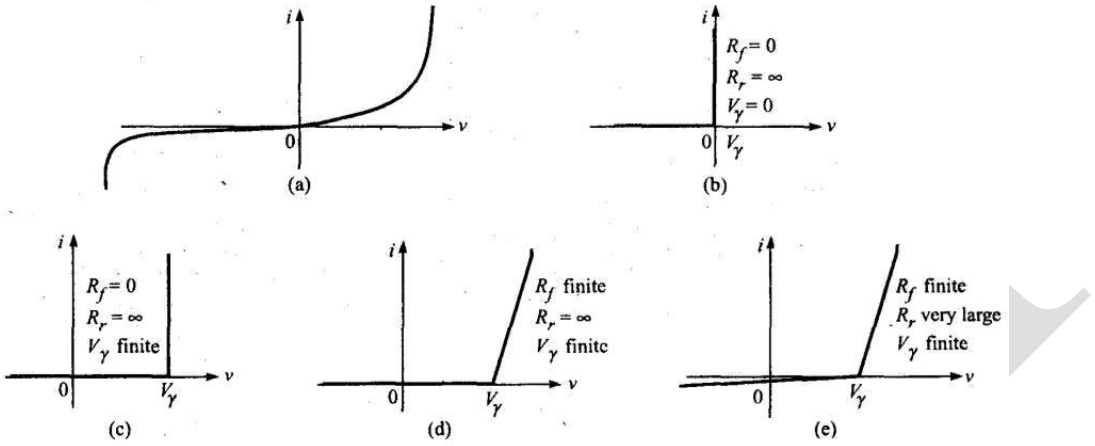


Figure 2.1 *v–i* characteristics of a diode.

Shunt Clippers

Clipping above reference level

Using the ideal diode characteristic of Figure 2.2(a), the clipping circuit shown in Figure 2.2(b), has the transmission characteristic shown in Figure 2.2(c). The transmission characteristic which is a plot of the output voltage *v0* as a function of the input voltage v, also exhibits piece-wise linear discontinuity. The break point occurs at the reference voltage VR. To the left of the break point i.e. for *vt* < *VR* the diode is reverse biased (OFF) and the equivalent circuit shown in Figure 2.2(d) results. In this region the signal v, may be transmitted directly to the output, since there is no load across the output to cause a drop across the series resistor /?. To the right of the break point i.e. for v(> VR the diode is forward biased (ON) and the equivalent circuit shown in Figure 2,2(e) results and increments in the inputs are totally attenuated and the output is fixed at VR. Figure 2.2(c) shows a sinusoidal input signal of amplitude large enough so that the signal makes excursions past the break point. The corresponding output exhibits a suppression of the positive peak of the signal. The output will appear as if the positive peak had been *clipped off* or *sliced off*

Clipping below reference level

If this clipping circuit of Figure 2.2(b), is modified by reversing the diode as shown in Figure 2.3(a), the corresponding piece-wise linear transfer characteristic and the output for a sinusoidal input will be as shown in Figure 2.3(b). In this circuit, the portion of the waveform

more positive than VR is transmitted without any attenuation but the portion of the waveform

less positive than VR is totally suppressed. For Vj < VR, the diode conducts and acts as a short

circuit and the equivalent circuit shown in Figure 2.3(c) results and the output is fixed at VR. For

v, > VR, the diode is reverse biased and acts as an open circuit and the equivalent circuit shown

in Figure 2.3(d) results and the output is the same as the input.

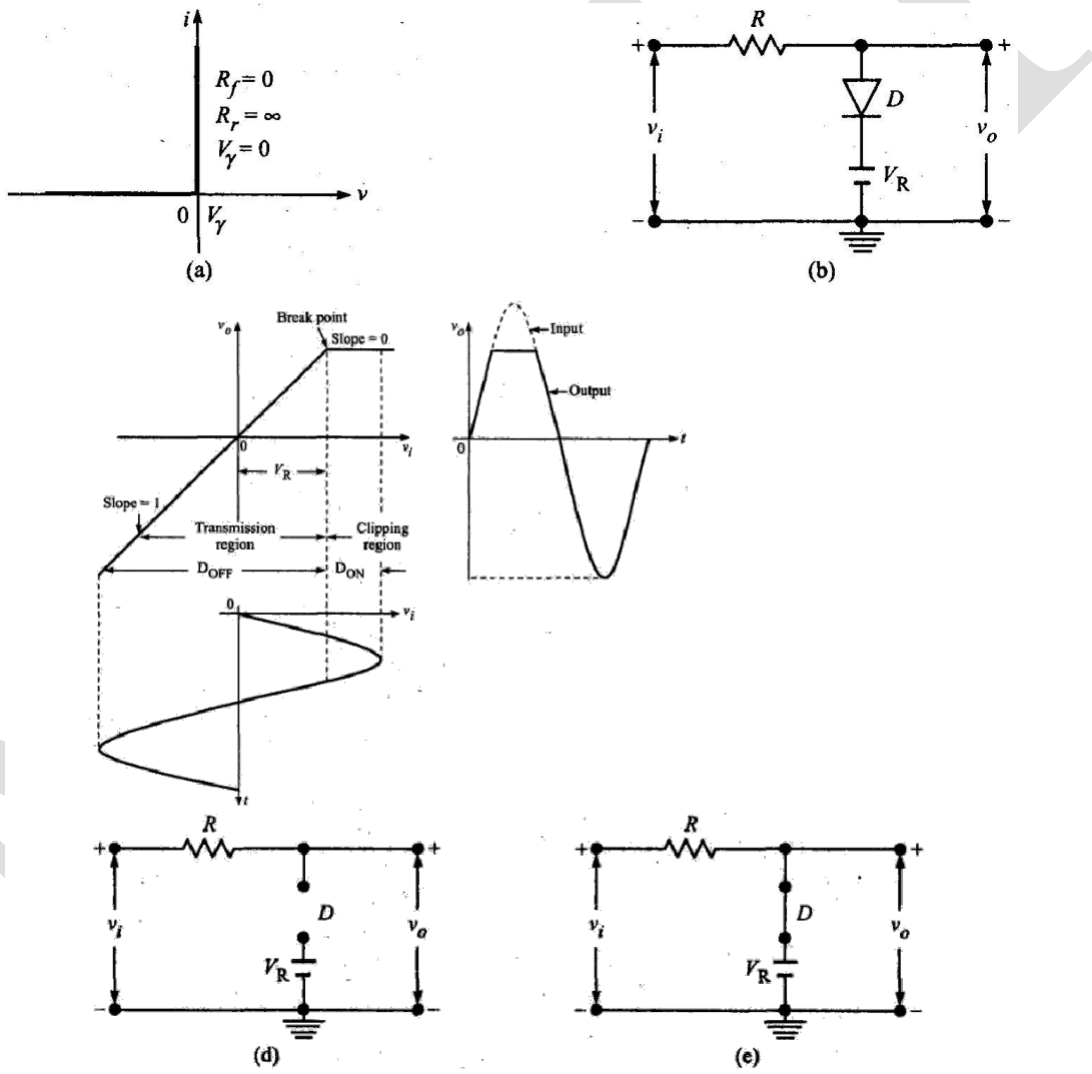


Figure 2.2 (a) *v-i* characteristic of an ideal diode, (b) diode clipping circuit, which removes that part of the waveform that is more positive than V_R, (c) the piece-wise linear transmission characteristic of the circuit, a sinusoidal input and the clipped output, (d) equivalent circuit for $v_(< V_R$, and (e) equivalent circuit for v, > V_R.

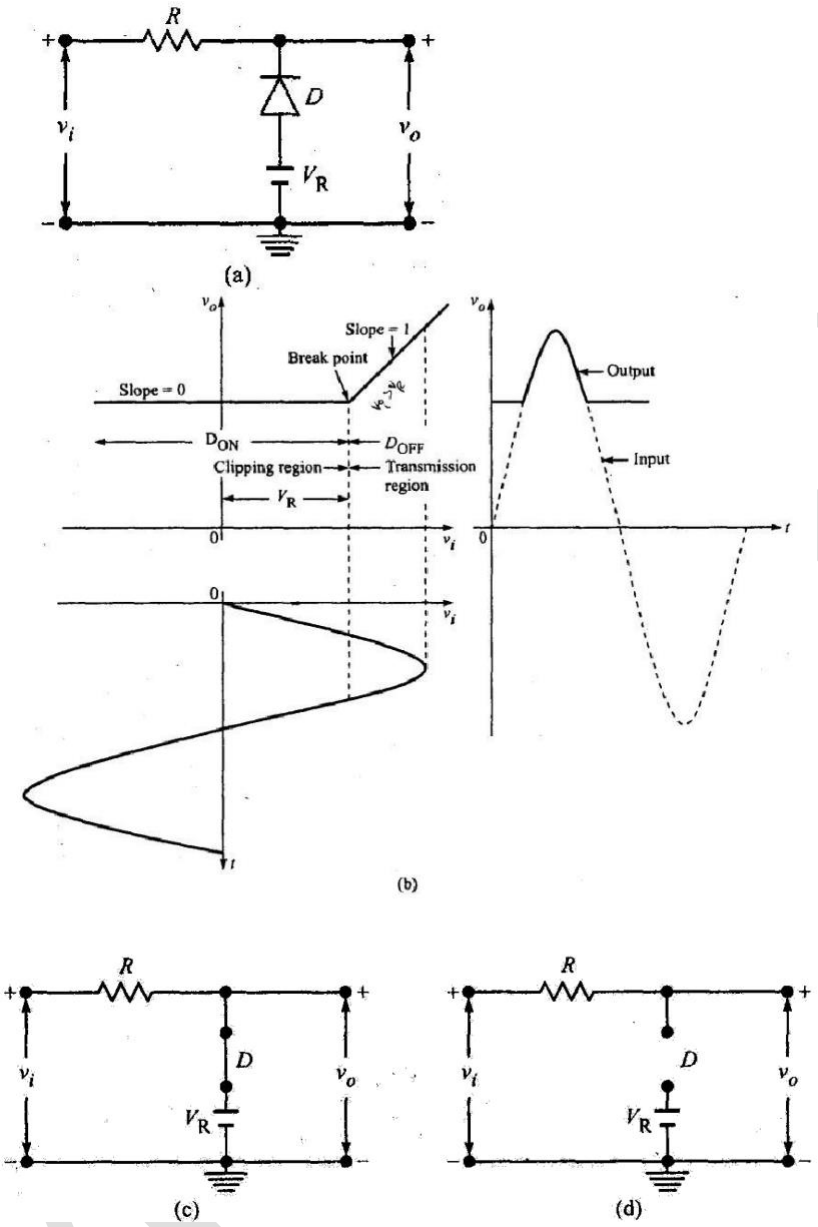


Figure 2.3 (a) A diode clipping circuit, which transmits that part of the sine wave that is more positive than VR, (b) the piece-wise linear transmission characteristic, a sinusoidal input and the clipped output, (c) equivalent circuit for v(< VR, and (d) equivalent circuit for v,- > VR.

In Figures 2.1(b) and 2.2(a), we assumed that *Rr* = °° and *Rf* = 0. If this condition does not apply, the transmission characteristic must be modified. The portions of those curves which are indicated as having unity slope must instead be considered as having a slope of *Rrl(Rr + R),* and those, having zero slope as having a slope of /?/(/?/ + /?). In the transmission region of a diode clipping circuit, it is required that *Rr » R,* i.e. *Rr = kR,* where *k* is a large number, and in the

attenuation region, it is required that $R \gg Rf$. From

these equations we can deduce that $R = J\,RrxR^{\wedge}$, i.e. the external resistance R is to be selected as the geometric mean of Rf and /?,. The ratio $RrIRf$ serves as a figure of merit for the diodes used in these applications. A zener diode may also be used in combination with a *p-n* junction diode to obtain single-ended clipping, i.e. one-level clipping.

Series Clippers

Clipping above the reference voltage *Vn*

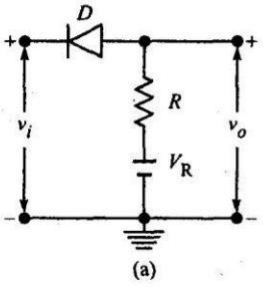
Figure 2.4(a) shows a series clipper circuit using a p-n junction diode. VR is the reference voltage source. The diode is assumed to be ideal (/?/ = 0, *Rr* = °°, Vy= 0) so that it acts as a short circuit when it is ON and as a open circuit when it is OFF. Since the diode is in the series path connecting the input and the output it is called a series clipper. The *v0* versus v, characteristic called the *transfer characteristic* is shown in Figure 2.4(b). The output for a sinusoidal input is shown in Figure 2.4(c).

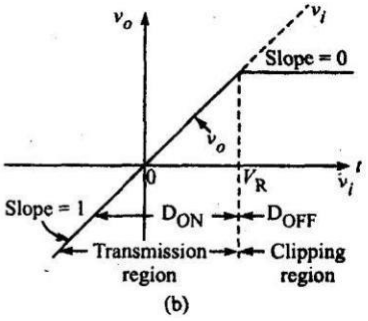
The circuit works as follows:

For v, < VR, the diode Dj is forward biased because its anode is at a higher potential than its cathode. It conducts and acts as a short circuit and the equivalent circuit shown in Figure

2.4(d) results. The difference voltage between the input v,- and the reference voltage VR i.e. (VR

– vi) is dropped across . Therefore *v0* = vi and the slope of the transfer characteristic for vi < *VR* is 1. Since the input signal is transmitted to the output without any change, this region is called the transmission region.





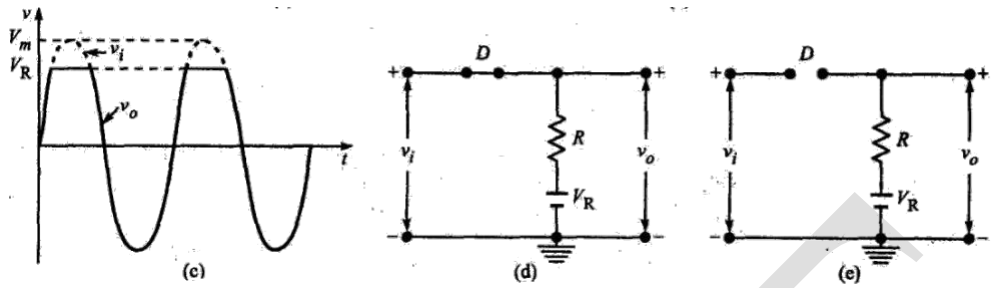
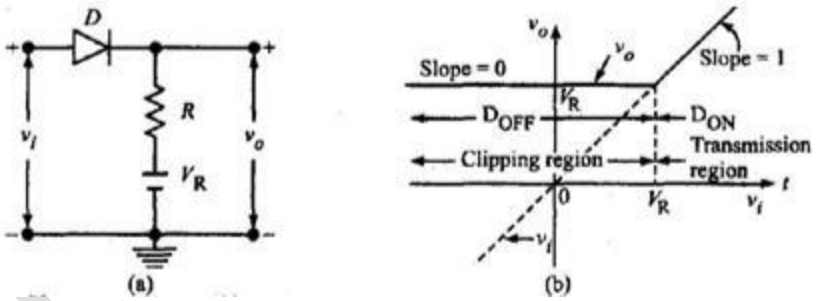


Figure 2.4 (a) Diode series clipper circuit diagram, (b) transfer characteristic, (c) output waveform for a sinusoidal input, (d) equivalent circuit for v; < VR, and (e) equivalent circuit for v(> *VR.*

For v, > VR, the diode is reverse biased because its cathode is at a higher potential than its anode, it does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.4(e) results. No current flows through *R* and so no voltage drop across it. So the output voltage *v0* = VR and the slope of the transfer characteristic is zero. Since the input signal above V R is clipped OFF for v, > VR, this region is called the *clipping region.* The equations V0=Vi for Vi < VR and V0= VR for Vi > VR are called the transfer characteristic equations.

Clipping below the reference voltage *VB*

Figure 2.5(a) shows a series clipper circuit using a p-n junction diode and a reference voltage source VR. The diode is assumed to be ideal *(Rf* = 0, *Rr* = °°, Vy = 0) so that it acts as a short circuit when it is ON and as a open circuit when it is OFF. Since the diode is in the series path connecting the input and the output it is called a series clipper. The transfer characteristic is shown in Figure 2.5(b). The output for a sinusoidal input is shown in Figure 2.5(c).



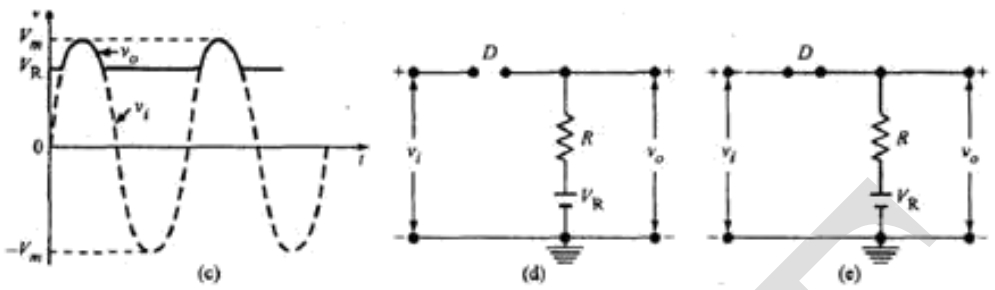


Figure 2.5 (a) Diode series clipper circuit diagram, (b). transfer characteristics, (c) output for a sinusoidal input, (d) equivalent circuit for vi- < VR, and (e) equivalent circuit for vi- > VR. The circuit works as follows:

For vi < VR, D is reversed biased because its anode is at a lower potential than its cathode.

The diode does not conduct and acts as an open circuit and the equivalent circuit shown in Figure 2.5(d) results. No current flows through *R* and hence no voltage drop across *R* and

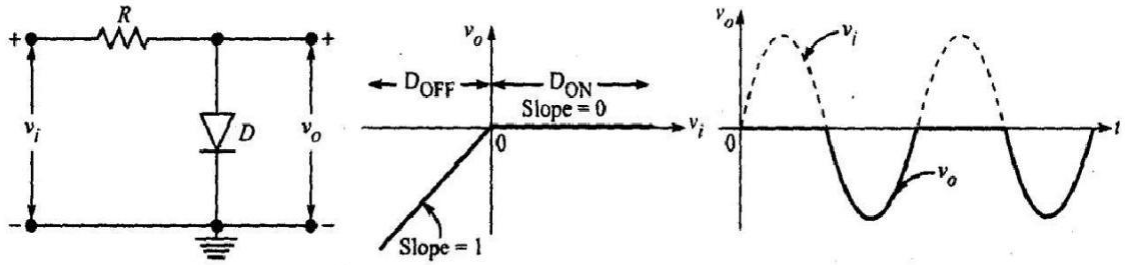
hence v_o = VR- So the slope of the transfer characteristic is zero for v, < VR. Since the input is clipped off for v, < VR, this region is called the clipping region.

For v, > VR, the diode is forward biased because its anode is at a higher potential than its cathode. The diode conducts and acts as a short circuit and the equivalent circuit shown in Figure 2.5(e) results. Current flows through /? and the difference voltage between the input and the output voltages v, - VR drops across /? and the output *v0* = vi. The slope of the transfer characteristic for v, > VR is unity. Since the input is transmitted to the output for v; > VR, this region is called the transmission region. The equations are called the transfer characteristic equations.

$v_o = V_R$ for $v_i < V_R$
$v_o = v_i$ for $v_i > V_R$

Some single-ended diode clipping circuits, their transfer characteristics and the output waveforms for sinusoidal inputs are shown below (Figure 2.6).

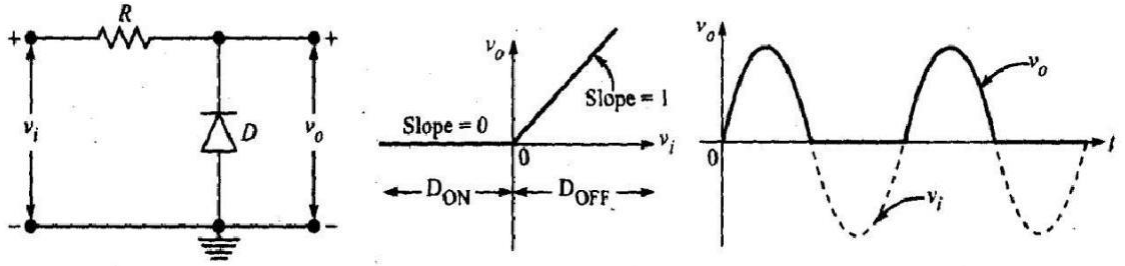
Some single-ended clipping circuits



For $v_i < 0$, D is OFF $\therefore v_o = v_i$

For $v_i > 0$, D is ON $\therefore v_o = 0$

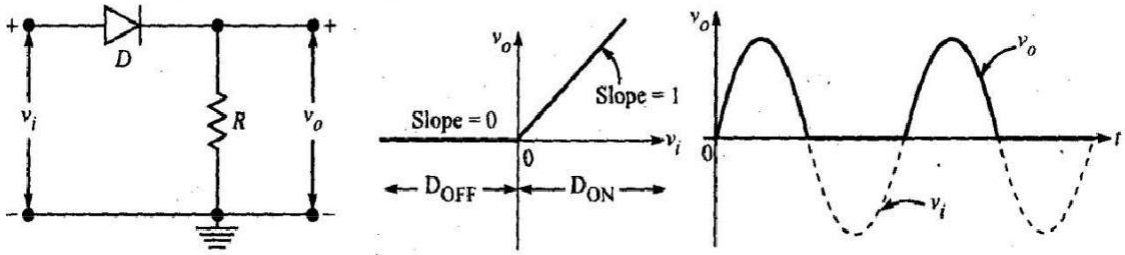
(a) Shunt clipper, positive peak clipping without reference



For $v_i < 0$, D is ON $\therefore v_o = 0$

For $v_i > 0$, D is OFF $\therefore v_o = v_i$

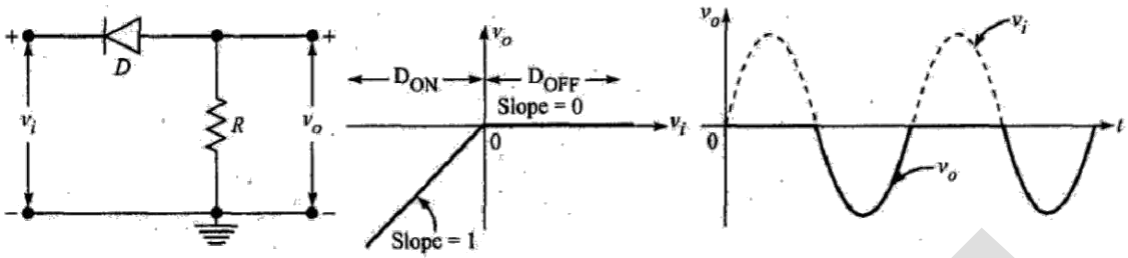
(b) Shunt clipper, negative peak clipping without reference



For $v_i < 0$, D is OFF $\therefore v_o = 0$

For $v_i > 0$, D is ON $\therefore v_o = v_i$

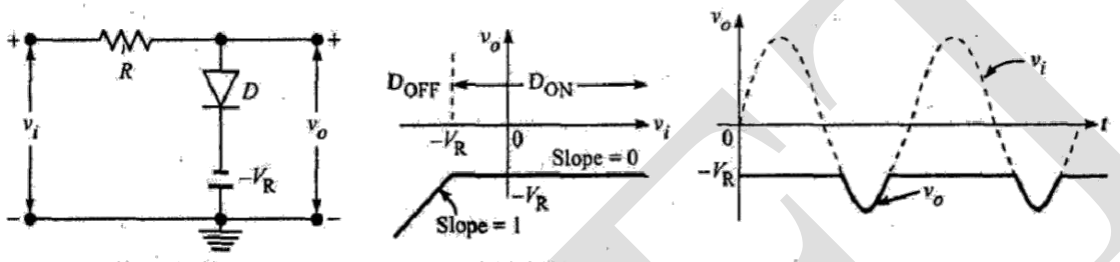
(c) Series clipper, negative peak clipping without reference



For $v_i < 0$, D is ON $\therefore v_o = v_i$

For $v_i > 0$, D is OFF $\therefore v_o = 0$

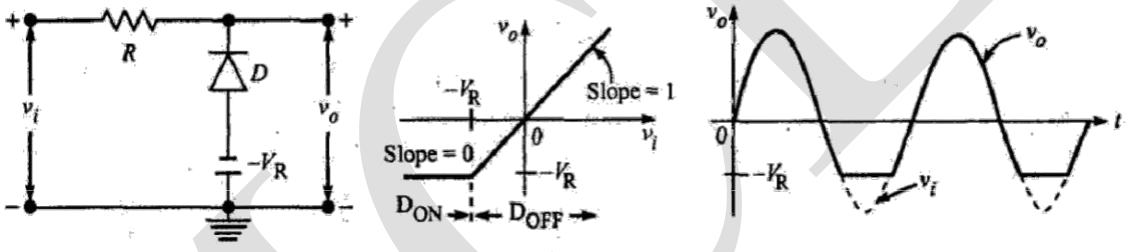
(d) Series clipper, positive peak clipping without reference



For $v_i < -V_R$, D is OFF $\therefore v_o = v_i$

For $v_i > -V_R$, D is ON $\therefore v_o = -V_R$

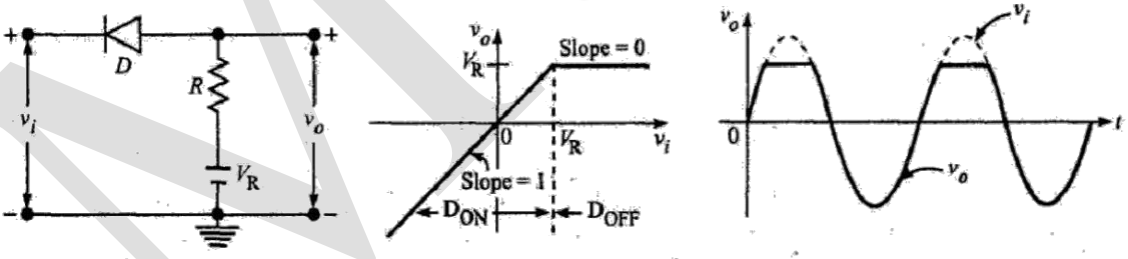
(e) Shunt clipper, negative base clipping above reference level



For $v_i < -V_R$, D is ON $\therefore v_o = -V_R$

For $v_i > -V_R$, D is OFF $\therefore v_o = v_i$

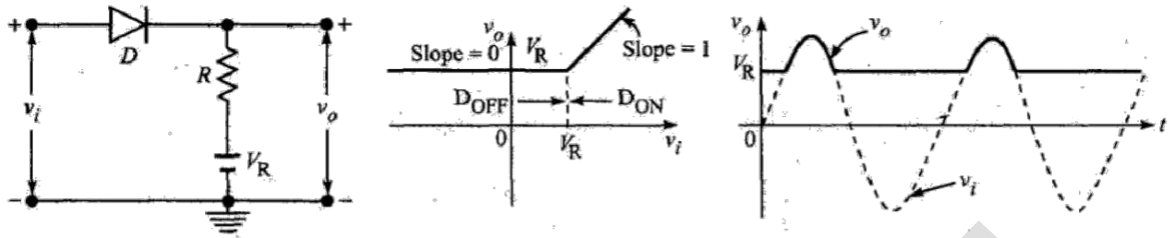
(f) Shunt clipper, negative base clipping below reference level



For $v_i < V_R$, D is ON $\therefore v_o = v_i$

For $v_i > V_R$, D is OFF $\therefore v_o = V_R$

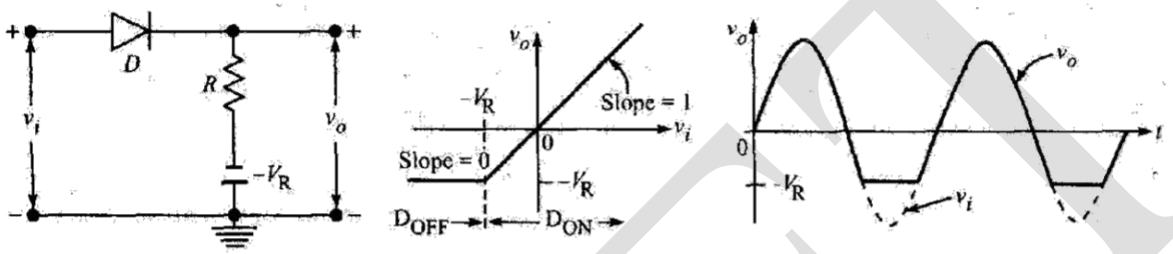
(g) Series clipper, positive base clipping above reference level



For $v_i < V_R$, D is OFF, $\therefore v_o = V_R$

For $v_i > V_R$, D is ON, $\therefore v_o = v_i$

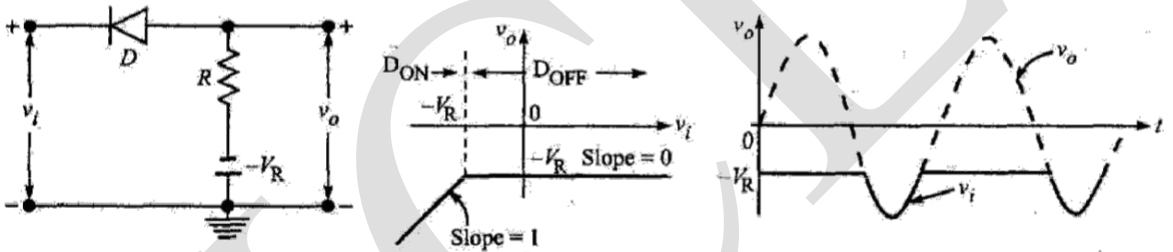
(h) Series clipper, positive base clipping before reference level



For $v_i < -V_R$, D is OFF, $\therefore v_o = -V_R$

For $v_i > -V_R$, D is ON, $\therefore v_o = v_i$

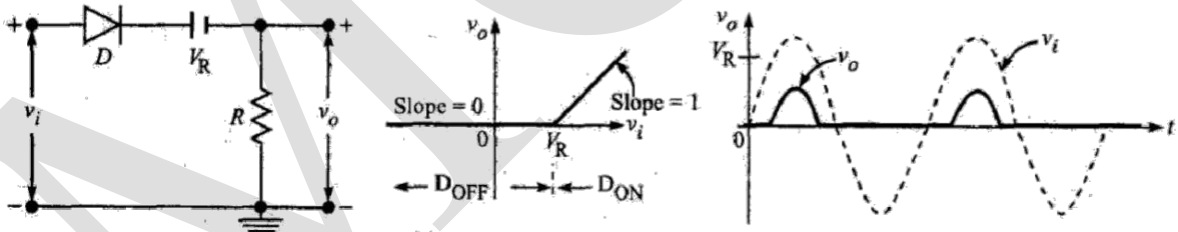
(i) Series clipper, negative base clipping above reference level



For $v_i < -V_R$, D is ON, $\therefore v_o = v_i$

For $v_i > -V_R$, D is OFF, $\therefore v_o = -V_R$

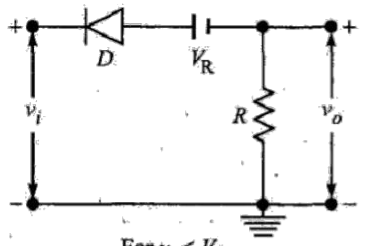
(j) Series clipper, negative base clipping above reference level



For $v_i < V_R$, D is OFF, $\therefore v_o = 0$

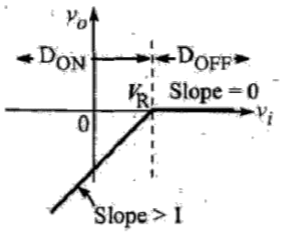
For $v_i > V_R$, D is ON, $\therefore v_o = v_i - V_R$

(k) Series clipper (Biased)



For $v_i < V_R$, $v_o = v_i - V_R$

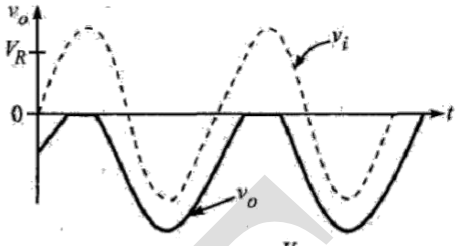
For $v_i > V_R$, $v_o = 0$

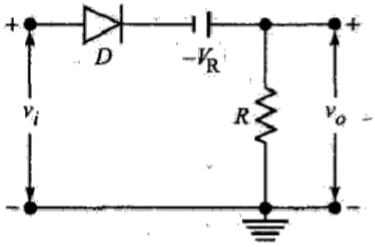


D is ON

D is OFF

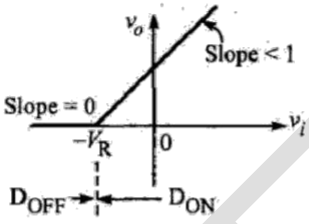
(l) Series clipper (Biased)





For $v_i < -V_R$, $v_o = 0$

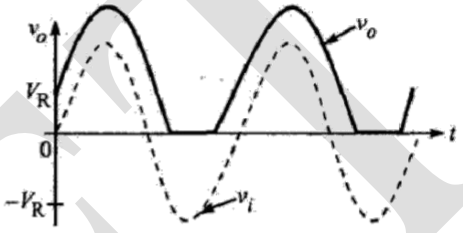
For $v_i > -V_R$, $v_o = v_i + V_R$

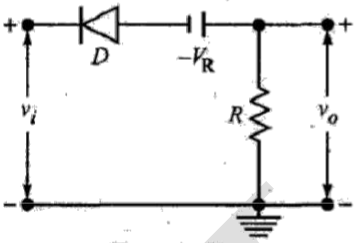


D is OFF

D is ON

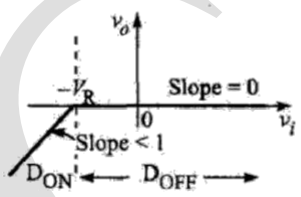
(m) Series clipper (Biased)





For $v_i < -V_R$, $v_o = v_i + V_R$

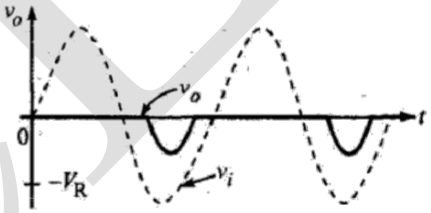
For $v_i > -V_R$, $v_o = 0$

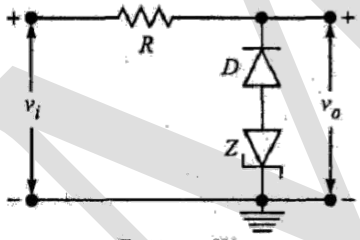


D is ON

D is OFF

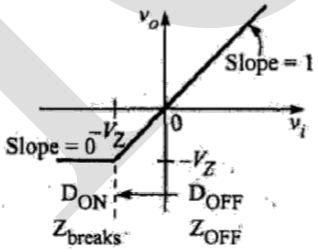
(n) Series clipper (Biased)





For $v_i < -V_Z$, $v_o = -V_Z$

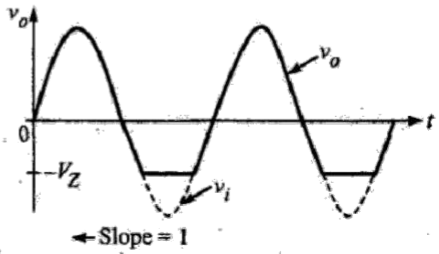
For $v_i > -V_Z$, $v_o = v_i$

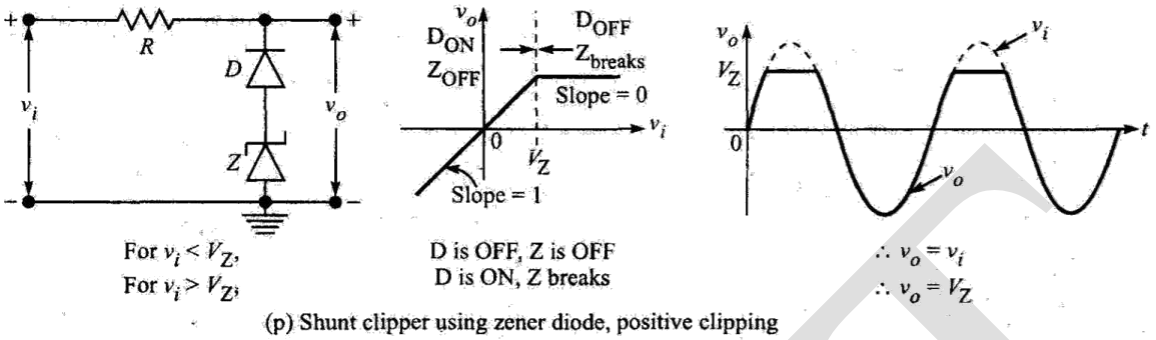


D is ON, Z breaks

D is OFF, Z is OFF

(o) Shunt clipper using zener diode, negative clipping





(p) Shunt clipper using zener diode, positive clipping

Figure 2.6 Examples of single-ended clipping circuits.

In the clipping circuits, the diode may appear as a series element or as a shunt element. The use of the diode as a series element has the disadvantage that when the diode is OFF and it is intended that there be no transmission, fast signals or high frequency waveforms may be transmitted to the output through the diode capacitance. The use of the diode as a shunt element has the disadvantage that when the diode is open and it is intended that there be transmission, the diode capacitance together with all other capacitances in shunt with the output terminals will round off the sharp edges of the input waveforms and attenuate, the high frequency signals.

Clipping at Two Independent Levels

parallel, a series, or a series-parallel arrangement may be used in double-ended limiting at two independent levels. A parallel arrangement is shown in Figure 2.7. Figure 2.8 shows the transfer characteristic and the output for a sinusoidal input. The input-output characteristic has two breakpoints, one at *v0* = v, = VR1 and the second at *v0* = v, = -VR2 and has the following characteristics.

Input v_i	*Output* v_o	*Diode status*
$v_i > V_{R1}$	$v_o = V_{R1}$	D_1 ON, D_2 OFF
$-V_{R2} < v_i < V_{R1}$	$v_o = v_i$	D_1 OFF, D_2 OFF
$v_i < -V_{R2}$	$v_o = -V_{R2}$	D_1 OFF, D_2 ON

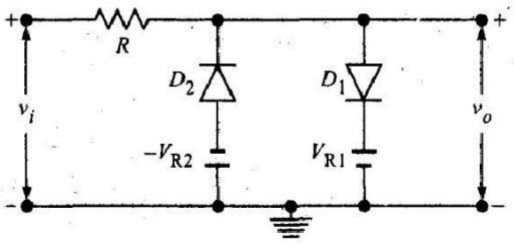


Figure 2.7 A diode clipper which limits at two independent levels.

DI is

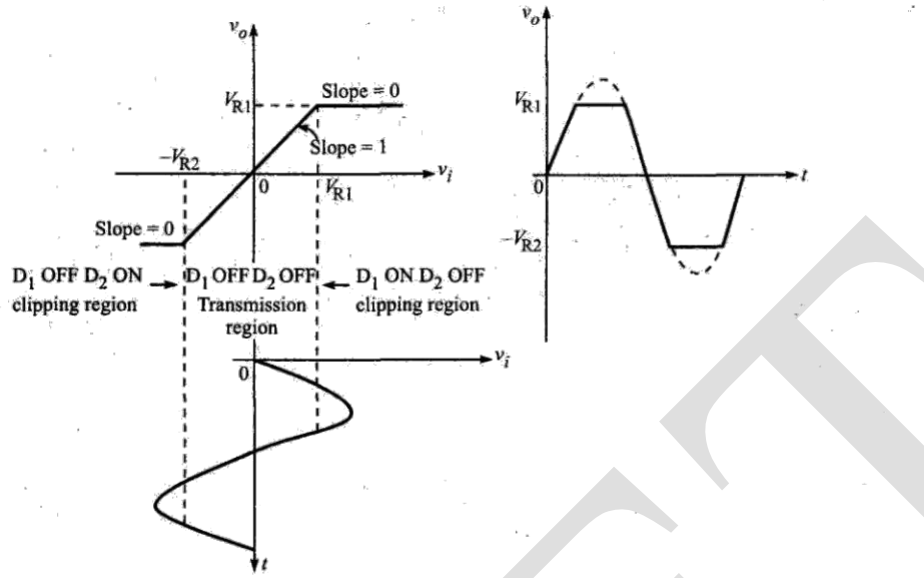


Figure 2.8 The piece-wise linear transfer curve, the input sinusoidal waveform and the corresponding output for the clipper of Figure 2.7.

The two level diode clipper shown in Figure 2.8 works as follows. For v, > VR1,

ON and D2 is OFF and the equivalent circuit shown in Figure 2.9(a) results. So the output *v0* = VR1 and the slope of the transfer characteristic is zero.

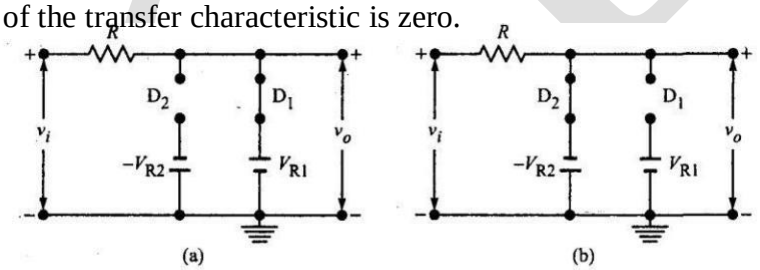


Figure 2.9 (a) Equivalent circuit for $v_i > V_{R1}$ and (b) equivalent circuit for $v_i < -V_{R2}$.

For v, < - VR2, DI is OFF and D2 is ON and the equivalent circuit shown in Figure 2.9(b) results. So the output v0 = - VR2 and the slope of the transfer characteristic is zero. For-VR2 < v, < VRI, D! is OFF and D2 is OFF and the equivalent circuit shown in Figure 2.10 results. So the output *v0* = v/ and the slope of the transfer characteristic is one.

The circuit of Figure 2.7 is called a slicer because the output contains a slice of the input between two reference levels VR! and VR2. Looking at the input and output waveforms, we observe that this circuit may be used to convert a sine wave into a square wave, if VDI = Vm. and if the amplitude of the input signal is very large compared with the difference in the

reference levels, the output will be a symmetrical square wave. Two zener diodes in series opposing may also be used to form a double-ended clipper.

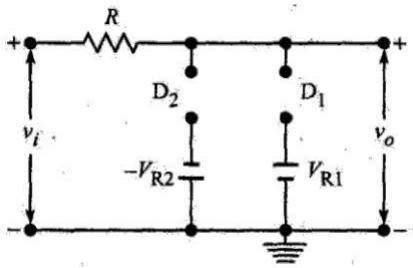
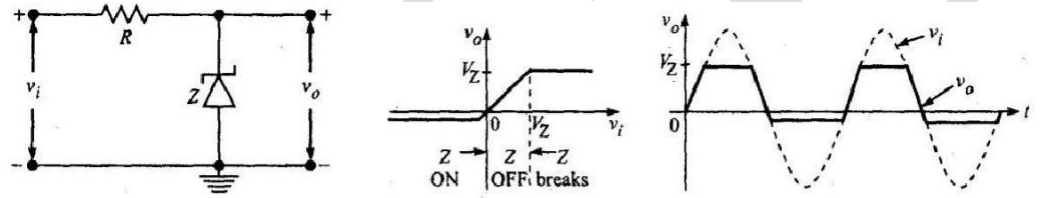


Figure 2.10 Equivalent circuit for $-V_{R2} < v_i < V_{R1}$.

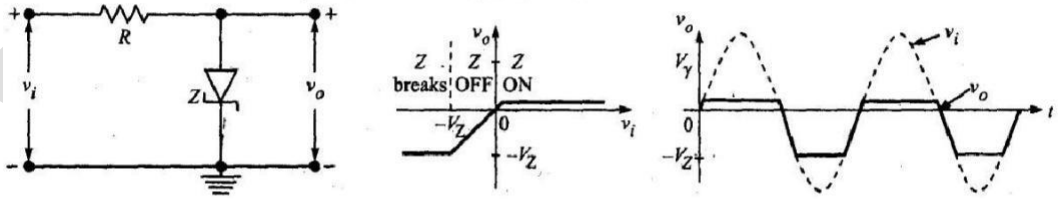
If the diodes have identical characteristics, then, a symmetrical limiter is obtained. Some double-ended clippers, their transfer characteristics and the outputs for sine wave inputs are shown in Figure 2.11.

Some double-ended clipping circuits



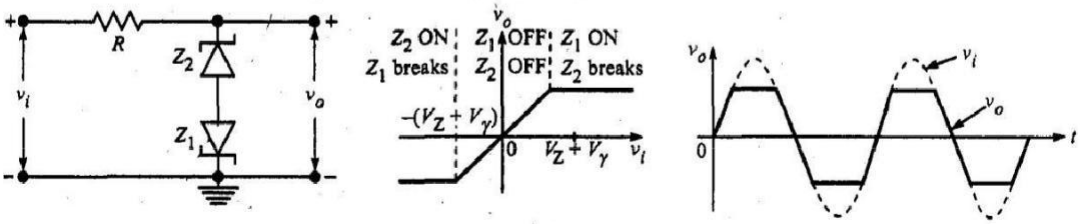
For $v_i < -V_\gamma$, Z is ON, $\therefore v_o = -V_\gamma$
For $-V_\gamma < v_i < V_Z$, Z is OFF, $\therefore v_o = v_i$
For $v_i > V_Z$, Z breaks, $\therefore v_o = V_Z$

(a) Two level clipping using a zener diode



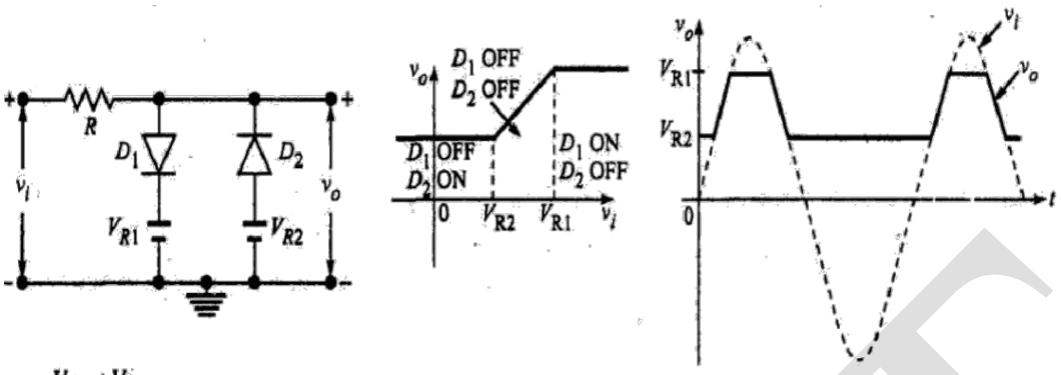
For $v_i < -V_Z$, Z breaks, $\therefore v_o = -V_Z$
For $-V_Z < v_i < V_\gamma$, Z is OFF, $\therefore v_o = v_i$
For $v_i > V_\gamma$, Z is ON, $\therefore v_o = V_\gamma$

(b) Two level clipping using one zener diode



For $v_i < -(V_Z + V_\gamma)$, Z_1 breaks, Z_2 is on, $\therefore v_o = -(V_Z + V_\gamma)$
For $-(V_Z + V_\gamma) < v_i < (V_Z + V_\gamma)$, Z_1 is OFF, Z_2 is OFF, $\therefore v_o = v_i$
For $v_i > (V_Z + V_\gamma)$, Z_1 is ON, Z_2 breaks, $\therefore v_o = V_Z + V_\gamma$

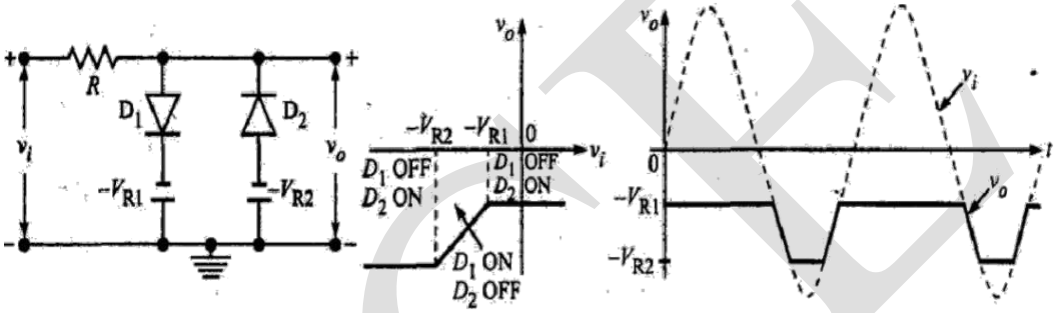
(c) Two level clipping using two zener diodes



$V_{R2} < V_{R1}$

For $v_i < V_{R2}$,	D_1 is OFF, D_2 is ON	$\therefore v_o = V_{R2}$
For $V_{R2} < v_i < V_{R1}$,	D_1 is OFF, D_2 is OFF	$\therefore v_o = v_i$
For $v_i > V_{R1}$,	D_1 is ON, D_2 is OFF	$\therefore v_o = V_{R1}$

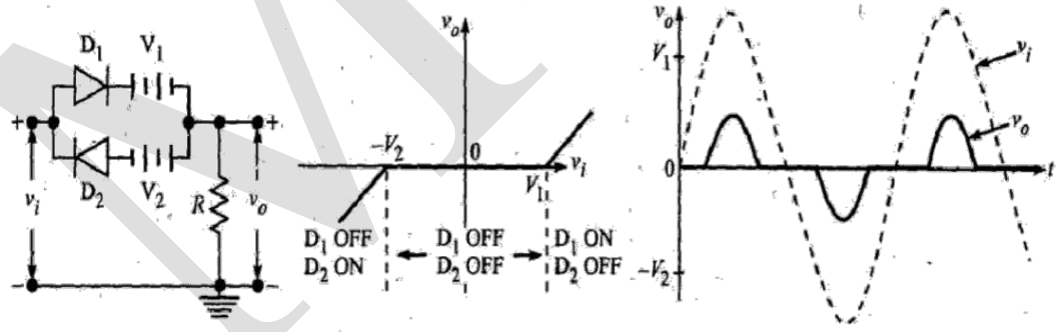
(d) Two level clipping using two diodes and two positive reference voltage sources.



$-V_{R2} < -V_{R1}$

For $v_i < -V_{R2}$,	D_1 is OFF, D_2 is ON	$\therefore v_o = -V_{R2}$
For $-V_{R2} < v_i < -V_{R1}$,	D_1 is OFF, D_2 is OFF	$\therefore v_o = v_i$
For $v_i > -V_{R1}$	D_1 is ON, D_2 is OFF	$\therefore v_o = -V_{R1}$

(e) Two level clipping using two diodes and two negative reference voltage sources.



For $v_i < -V_2$,	D_1 is OFF, D_2 is ON	$\therefore v_o = v_i + V_2$
For $-V_2 < v_i < V_1$,	D_1 is OFF, D_2 is OFF	$\therefore v_o = 0$
For $v_i > V_1$,	D_1 is ON, D_2 is OFF	$\therefore v_o = v_i - V_1$

(f) Double ended series biased clipper

Figure 2.11 Examples of double-ended clippers.

CLAMPING CIRCUITS

Clamping circuits are circuits, which are used to clamp or fix the extremity of a periodic waveform to some constant reference level *V.R.* Under steady-state conditions, these circuits restrain the extremity of the waveform from going beyond *VR.* Clamping circuits may be one-way clamps or two-way clamps. When only one diode is used and a voltage change in only one direction is restrained, the circuits are called one-way clamps. When two diodes are used and the voltage change in both the directions is restrained, the circuits are called two-way clamps.

The Clamping Operation

When a signal is transmitted through a capacitive coupling network *(RC* high-pass circuit), it looses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level. For this reason, the clamping circuit is often referred to as *dc restorer* or *dc reinserter.* In fact, it should be called a *dc inserter,* because the dc component introduced may be different from the dc component lost during transmission. The clamping circuit only changes the dc level of the input signal. It does not affect its shape

Classification of clamping circuits

Basically clamping circuits are of two types: (1) positive-voltage clamping circuits and

(2) negative-voltage clamping circuits.

In positive clamping, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level, i.e. the output waveform is positively clamped with reference to the reference level. In negative clamping, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference, i.e. the output waveform is negatively clamped with respect to the reference level. The capacitors are essential in clamping circuits. The difference between the clipping and clamping circuits is that while the clipper clipps off an unwanted portion of the input waveform, the clamper simply clamps the maximum positive or negative peak of the waveform to a desired level. There will be no distortion of waveform.

Negative Clamper

Figure 3.1 (a) shows the circuit diagram of a basic negative clamper. It is also termed a positive peak clamper since the circuit clamps the positive peak of a signal to zero level. Assume that the signal source has negligible output impedance and that the diode" is ideal, *Rf*= 0 n and Vy = 0 V in that, it exhibits an arbitrarily sharp break at 0 V, and that its input signal shown in Figure 2.71(b) is a sinusoid which begins at $t = 0$. Let the capacitor C be uncharged at $t = 0$.

During the first quarter cycle, the input signal rises from zero to the maximum value. The diode conducts during this time and since we have assumed an ideal diode, the voltage across it is zero. The capacitor *C* is charged through the series combination of the signal source and the diode and the voltage across C rises sinusoidally. At -the end of the first quarter cycle, the voltage across

the capacitor, $v_C = V_m$.When, after the first quarter cycle, the peak has been passed and the input

signal begins to fall, the voltage v_C across the capacitor is no longer able to follow the input, because

there is no path for the capacitor to discharge. Hence, the voltage across the capacitor remains

constant at $v_C = V_m$, and the charged capacitor acts as a voltage source of V volts and after the first

quarter cycle, the output is given by v_0 = v, - V_m. During the succeeding cycles, the positive extremity of the signal will be *clamped* or *restored* to zero and the output

for $v_i = 0$, $v_o = -V_m$.

for $v_i = V_m$, $v_o = 0$,

for $v_i = -V_m$, $v_o = -2V_m$.

waveform shown in Figure 2.7 l(c) results. Therefore

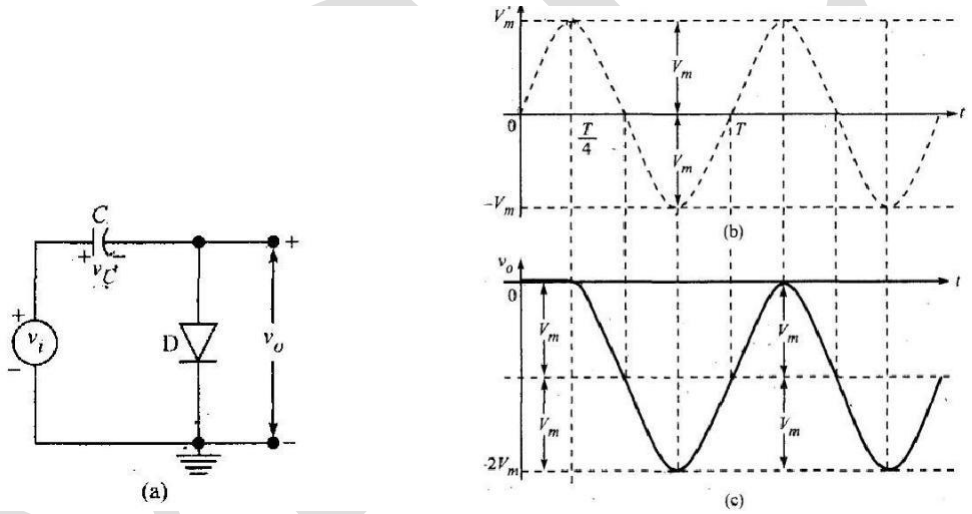


Figure 2.71 (a) A negative clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Suppose that after the steady-state condition has been reached, the amplitude of the input signal is increased, then the diode will again conduct for at most one quarter cycle and the dc voltage across the capacitor would rise to the new peak value, and the positive excursions of the signal would be again restored to zero.

Suppose the amplitude of the input signal is decreased after the steady-state condition has been reached. There is no path for the capacitor to discharge. To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across *C*, or equivalently to shunt a

resistor across D. In the latter case, the capacitor will discharge through the series combination of the resistor *R* across the diode and the resistance of the source, and in a few cycles the positive extremity would be again clamped at zero as shown in Figure 2.72(b). A circuit with such a resistor *'R* is shown in Figure 2.72(a).

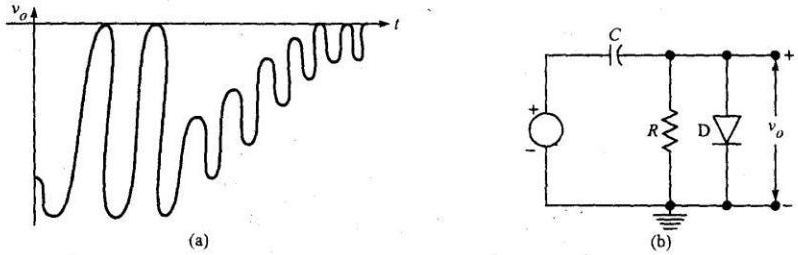


Figure 2.72 (a) Clamping circuit with a resistor *R* across the diode D and (b) output during transient period.

Positive Clamper

Figure 2.73(a) shows a positive clamper. This is also termed as negative peak clamper since this circuit clamps the negative peaks of a signal to zero level. The negative peak clamper, i.e. the positive clamper introduces a positive dc.

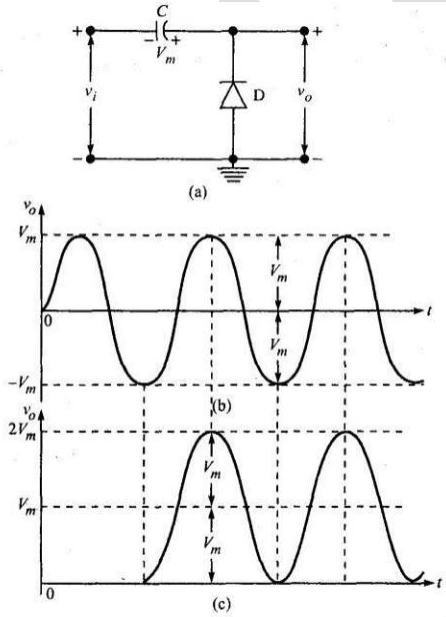


Figure 2.73 (a) A positive clamping circuit, (b) a sinusoidal input, and (c) a steady-state clamped output.

Let the input voltage be vi = *Vm* sin *(ot* as shown in Figure 2.73(b). When v, goes negative, the diode gets forward biased and conducts and in a few cycles the capacitor gets charged to *Vm* with the polarity shown in Figure 2.73(a). Under steady-state conditions, the capacitor acts as a constant voltage source and the output is $v_o = v_i - (-V_m) = v_i + V_m$.

Clamping Circuit Theorem

Under steady-state conditions, for any input waveform, the shape of the output waveform of a clamping circuit is fixed and also the area in the forward direction (when the diode conducts) and the area in the reverse direction (when the diode does not conduct) are related.

The clamping circuit theorem states that, for any input waveform under steady-state conditions, the ratio of the area Af under the output voltage curve in the forward direction

to that in the reverse direction Ar is equal to the ratio R//R-

This theorem applies quite generally independent of the input waveform and the magnitude of the source resistance. The proof is as follows:

Consider the clamping circuit of Figure 2.79, the equivalent circuits in Figures 2.80(a) and 2.80(b), and the input and output waveforms of Figures 2.82(a) and 2.82(b) respectively.

In the interval $0 < t < T$, the input is at its upper level, the diode is ON, and the equivalent circuit of Figure 2.80(a) results. If v/(f) is the output waveform in the forward direction, then the

capacitor charging current is $i_f(t) = \frac{v_f(t)}{R_f}$ Therefore, -the charge gained by the capacitor during

$$Q_g = \int_0^{T_1} i_f(t)dt = \frac{1}{R_f}\int_0^{T_1} v_f(t)dt = \frac{A_f}{R_f}$$

the forward interval is

In the interval TJ $< t <$ *T{ + T2*, the input is at its lower level, the diode is OFF, and the equivalent circuit of Figure 2.80(b) results. If *vr(t)* is the output voltage in the reverse direction,

then the current which discharges the capacitor is $i_r(t) = \frac{v_r(t)}{R}$

Therefore, the charge lost by the capacitor during the reverse interval is

$$Q_l = \int_{T_1}^{T_1+T_2} i_r(t)dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)dt = \frac{A_r}{R}$$

Under steady-state conditions, the net charge acquired by the capacitor over one cycle must be equal to zero. Therefore, the charge gained in the interval $0 < t < T\}$, will be equal to the charge lost in the interval $T1 < t < T1 + T2$, i.e. Qg = Ql

$$\frac{A_f}{R_f} = \frac{A_r}{R} \quad \text{i.e.} \quad \frac{A_f}{A_r} = \frac{R_f}{R}$$

RECTIFIERS & FILTERS

INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c.voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier,

iii) Filter and iv) Voltage regulator circuits.

These elements constitute d.c. regulated power supply shown in the fig 1 below.

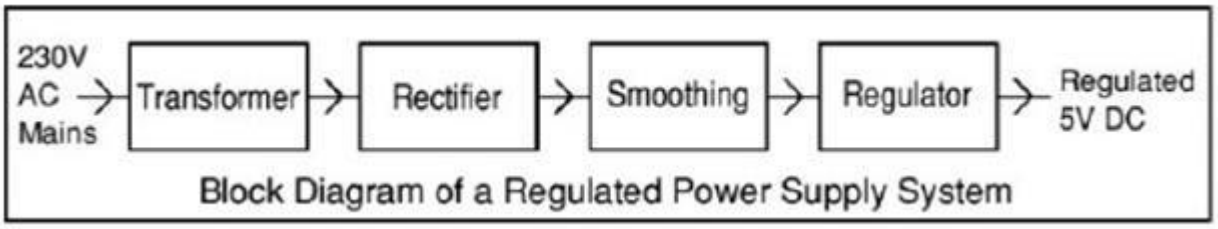


Fig 2.1: Block Diagram of regulated D.C Power Supply

- ✓ Transformer – steps down 230V AC mains to low voltage AC.
- ✓ Rectifier – converts AC to DC, but the DC output is varying.
- ✓ Smoothing – smooth the DC from varying greatly to a small ripple.
- ✓ Regulator – eliminates ripple by setting DC output to a fixed voltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

RECTIFIER

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a non-zero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating

d.c. voltage (Unidirectional).

Characteristics of a Rectifier Circuit:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a non-zero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c..Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base.

It is expressed mathematically as

i) Average value/dc value/mean value= $\frac{Area\ over\ one\ period}{Total\ time\ period}$

$$V_{dc} = \frac{1}{T}\int_0^T Vd(wt)$$

ii) Effective (or) R.M.S current:

The effective (or) R.M.S. current squared ofa periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

iii) Peak factor:

It is the ratio of peak value to Rms value

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

iv) Form factor:

It is the ratio of Rms value to average value

$$\text{Form factor} = \frac{Rms value}{average value}$$

v) Ripple Factor (Γ) :

It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

vi) Efficiency (η :

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuitconverts a.c. power into d.c. power.

$$\eta = \frac{o/p\ power}{i/p\ power}$$

vii) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroyingthe junction.

viii) Transformer Utilization Factor (UTF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{p_{ac(rated)}}$$

ix) % Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\%\,\mathrm{Re}\,gulation = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

For an ideal power supply, % Regulation is zero.

CLASSIFICATION OF RECTIFIERS

Using one or more diodes in the circuit, following rectifier circuits can be designed.

1) Half - Wave Rectifier

2) Full – Wave Rectifier

3) Bridge Rectifier

HALF-WAVE RECTIFIER:

A Half – wave rectifier as shown in **fig 1.2** is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

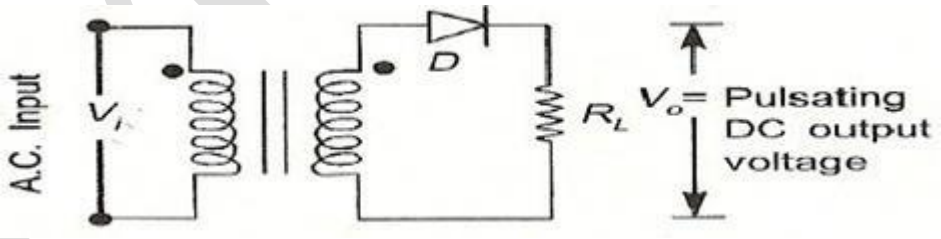


Fig 1.2: Basic structure of Half-Wave Rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

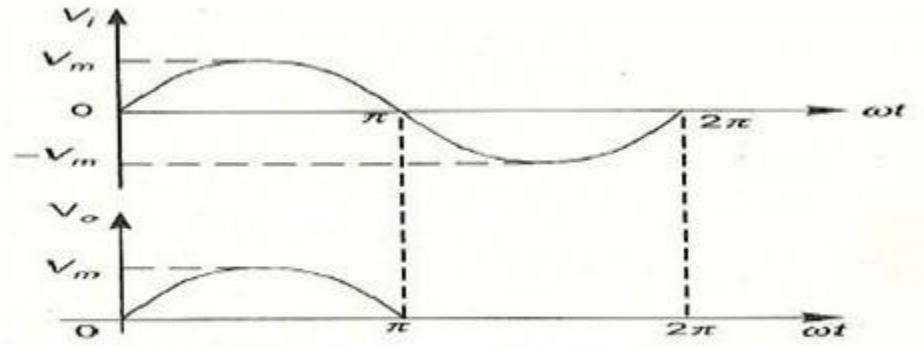


fig 3 Input and output waveforms of a Half wave rectifier

$V=V_m \sin(wt)$

The input to the rectifier circuit, Where V_m is the peak value of secondary a.c. voltage.

Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across RL. The waveform of the diode current (or) load current is shown in **fig 3**.

For the negative half-cycle of input, the diode D is reverse biased and hence it does not Conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half- cycle nopower is delivered to the load.

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage
5. Rectifier Efficiency (η)
6. Ripple factor (γ)

7. Peak Factor
8. % Regulation
9. Transformer Utilization Factor (TUF)
10. form factor
11. o/p frequency

Let a sinusoidal voltage Vi be applied to the input of the rectifier.

Then $V=V_m \sin(wt)$ Where V_m is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance Rf in the forward direction i.e., in the ON state and Rr (=∞) in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance RL is given by $V=V_m \sin(wt)$

i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T}\int_0^T Vd(wt)$$

$$V_{dc} = \frac{1}{T}\int_0^{2\Pi} V(\alpha)d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_{\Pi}^{2\Pi} V(\alpha)d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_0 V_m \sin(wt)$$

$$V_{dc} = \frac{V_m}{\Pi}$$

ii).AVERAGE CURRENT:

$$I_{dc} = \frac{I_m}{\Pi}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m \, sim(wt))^2 \, d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{I_m}{\Pi}}$$

V) PEAK FACTOR

$$\textbf{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\textbf{Peak Factor} = \frac{V_m}{(V_m / 2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rmsvalue}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m / 2)}{V_m / \Pi}$$

Form Factor =1.57

vii) Ripple Factor: $\Gamma = \frac{V_{ac}}{V_{dc}}$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{ac}}$$

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$\Gamma = 1.21$$

viii) Efficiency (η):

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{p_{ac}}{P_{dc}} * 100$$

$$\eta = 40.8$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is defined as

$$TUF = \frac{p_{dc}}{P_{ac(rated)}}$$

$$TUF = 0.286.$$

The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized.If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver

1000 X 0.287 = 287 watts to resistance load.

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half-wave rectifier, PIV is Vm.

DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

FULL WAVE RECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full waverectifier is shown in the **fig 4** below

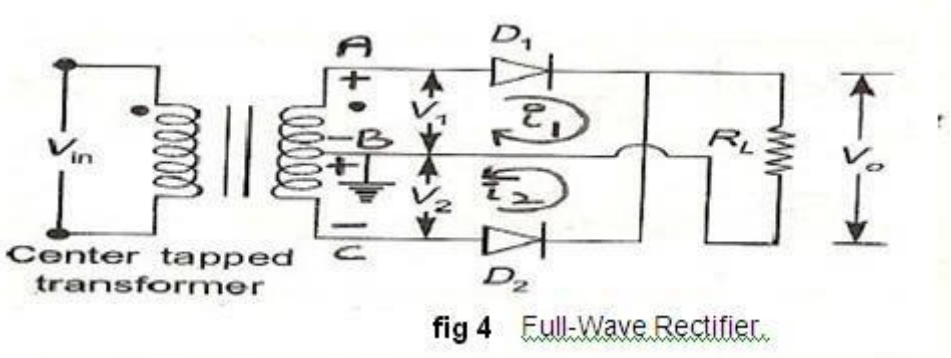


fig 4 Full-Wave Rectifier.

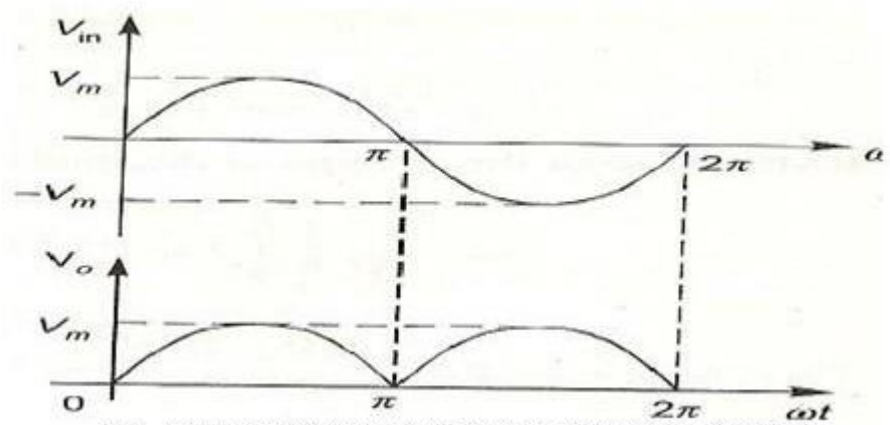


Fig. 5 input and output waveforms of Fullwave rectifier

Fig. 5 shows the input and output wave forms of the ckt.

During positive half of the input signal, anode of diode D1 becomes positive and at the same time the anode of diode D2 becomes negative. Hence D1 conducts and D2 does not conduct. The load current flows through D1 and the voltage drop across RL will be equal to the input voltage.

During the negative half cycle of the input, the anode of D1 becomes negative and the anode of D2 becomes positive. Hence, D1 does not conduct and D2 conducts. The load current flows through D2 and the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

i) AVERAGEVOLTAGE

$$V_{dc} = I_{dc}.R_L = \frac{2I_m}{\pi}.R_L \quad \text{We know } I_m = \frac{V_m}{R_S + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2.V_m.R_L}{\pi(R_S + R_f + R_L)}$$

$$If\ (R_s + R_f) << R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637V_m.$$

ii) _AVERAGE CURRENT

$$\frac{1}{2\pi}\int_0^{2\pi} id\theta = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\theta d\theta$$

$$I_{dc} = \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right]$$

$$= \frac{I_m}{2\pi}[(-2)(-2)]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637\, I_m.$$

$$\boxed{I_{dc} = 0.637 I_m.}$$

$$\therefore I_{DC}\ FWR = 2\ I_{DC}\ HWR.$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))^2\, d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{2I_m}{\Pi}}$$

V) PEAK FACTOR

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m / 2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rms\ value}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m / \sqrt{2})}{2V_m / \Pi}$$

Form Factor =1.11

vii) Ripple Factor:

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR,

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2 \times 1.414}\right)^2 - 1} = 0.483$$

viii) Efficiency (η):

$$\eta = \frac{o / ppower}{i / ppower} * 100$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

For FWR, $P_{dc} = I_{dc}^2 . R_L = \left(\frac{2}{\pi} . I_m\right)^2 . R_L$

$P_{ac} = I^2_{rms} (R_f + R_S + R_L)$

$$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_S + R_L)$$

$$\eta = \frac{\frac{I^2_m 4}{\pi^2} . R_L}{\frac{I^2 m^2}{2} . (R_f + R_s + R_L)}$$

$$If\ (R_f + R_S) << R_L$$

$$\eta = \frac{4}{\pi^2} . \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

a) $\text{TUF (Secondary)} = \dfrac{P_{dc}\ delivered\ to\ load}{AC\ power\ rating\ of\ transformer\ secondary}$

b) Since both the windings are used $\text{TUF}_{FWR} = 2\ \text{TUF}_{HWR}$

$= 2 \times 0.287 = 0.574$

c) TUF primary = Rated efficiency $= \frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$

d) Average $= \frac{0.812 + 0.574}{2} = 0.693$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half- wave rectifier, PIV is 2Vm

xi) % Regulation

$$\text{Voltage regulation} = \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_S)}$$

.

Advantages

1) Ripple factor = 0.482 (against 1.21 for HWR)

2) Rectification efficiency is 0.812 (against 0.405 for HWR)

3) Better TUF (secondary) is 0.574 (0.287 for HWR)

4) No core saturation problem

Disadvantages:

1) Requires center tapped transformer.

BRIDGE RECTIFIER.

Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the **Full Wave Bridge Rectifier**. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

The Diode Bridge Rectifier

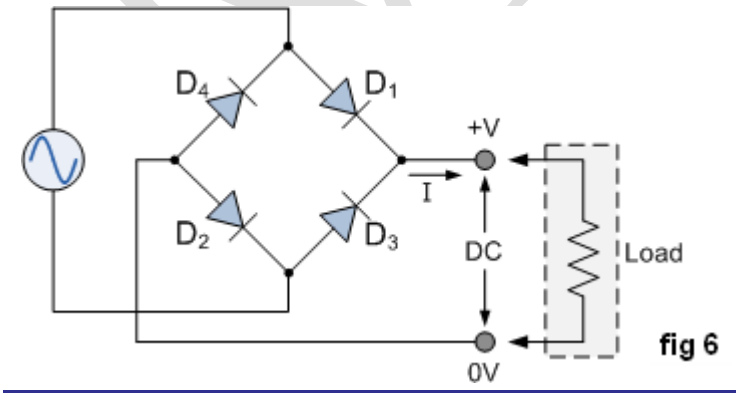


fig 6

The four diodes labelled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below (fig 7).

The Positive Half-cycle

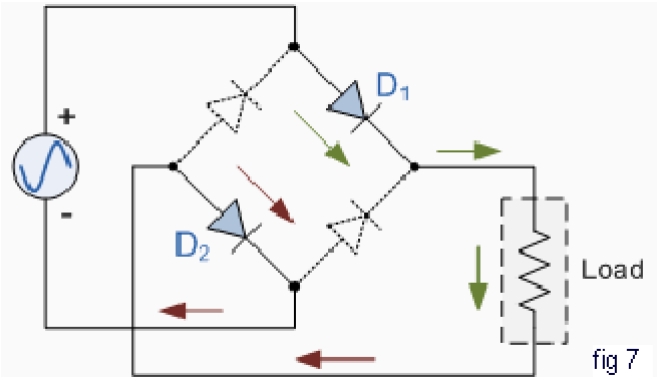


fig 7

The Negative Half-cycle

During the negative half cycle of the supply, diodes D3 and D4 conduct in series (fig 8), but diodes D1 and D2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.

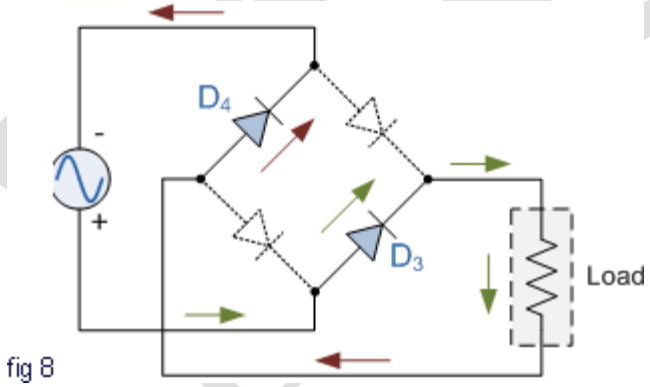


fig 8

As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC

voltage across the load is $0.637V_{max}$. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops (2x 0.7 = 1.4V) less than the input V_{MAX} amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply)

Therefore, the following expressions are same as that of full wave rectifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no.load) V_{DC} $\frac{2V_m}{\pi}$

d) Ripple factor $\gamma = 0.482$

e) Rectification efficiency = $\eta = 0.812$

f) DC output voltage full load.

= $V_{DCFL} = \frac{2V_m}{\pi} - I_{dc}(R_S + 2R_f)$; i.e., less by one diode loss.

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

Comparison:

Sl. No.	Parameter	HWR	FWR	BR
1	No. of diodes	1	2	4
2	PIV of diodes	V_m	2 V_m	V_m
3	Secondary voltage (rms)	V	V-0-V	V
4	DC output voltage at no load	$\frac{V_m}{\pi}$ =0.318 V_m	$\frac{2V_m}{\pi}$ =0.636 V_m	$\frac{2V_m}{\pi}$ =0.636 V_m
5	Ripple factor γ	1.21	0.482	0.482
6	Ripple frequency	f	2f	2f
7	Rectification efficiency η	0.406	0.812	0.812
8	TUF	0.287	0.693	0.812

FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimizethe undesirable ac i.e., ripple leaving only the dc component to appear at the output.

Some important filters are:

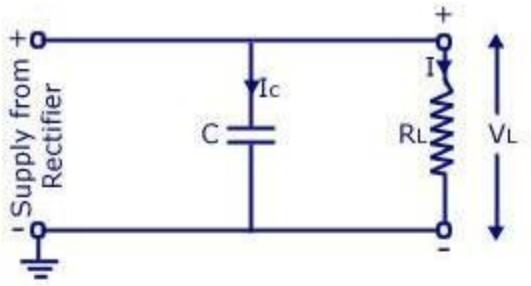
1. Inductor filter
2. Capacitor filter
3. LC or L section filter
4. CLC or Π-type filter

CAPACITOR FILTER

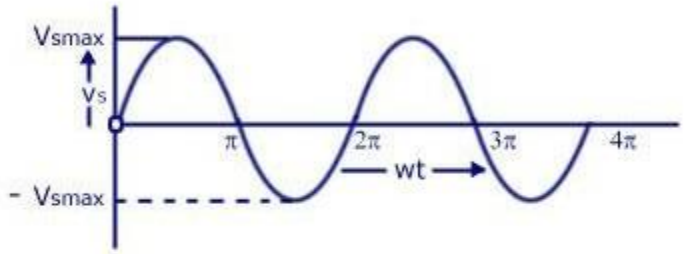
This is the most simple form of the **filter circuit** and in this arrangement a high value capacitor C is placed directly across the output terminals, as shown in figure. During the conduction period it gets charged and stores up energy to it during non-conduction period. Through this process, the time duration during which Ft is to be noted here that the capacitor C gets charged to the peak because there is no resistance (except the negligible forward resistance of diode) in the charging path. But the discharging time is quite large (roughly 100 times more than the charging time depending upon the value of RL) because it discharges through load resistance RL.

The function of the capacitor filter may be viewed in terms of impedances. The large value capacitor C offers a low impedance shunt path to the ac components or ripples but offers high impedance to thedc component. Thus ripples get bypassed through capacitor C and only dc component flows through the load resistance RL

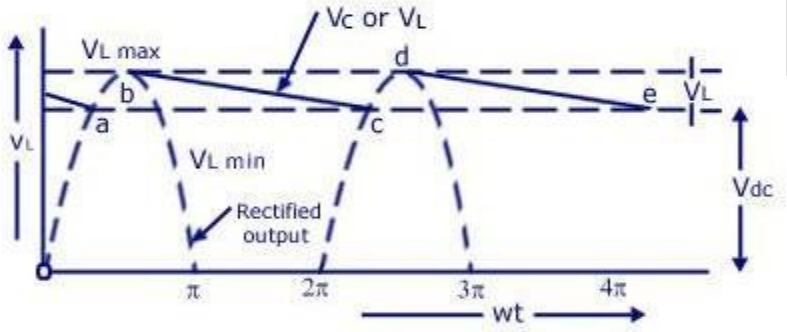
> Capacitor filter is very popular because of its low cost, small size, light weight and good characteristics.



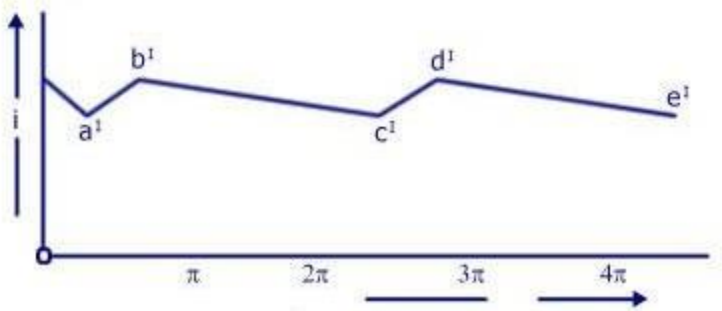
Circuit Diagram



Input voltage Waveform to Rectifier



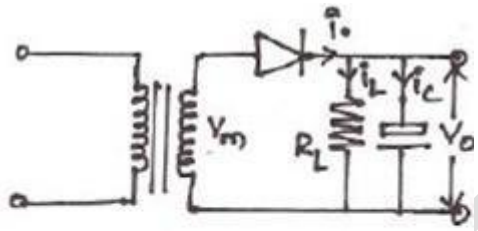
Rectified and filtered Output Voltage Waveform



Load Current Waveform
Half-wave Rectifier With Shunt Capacitor Filter

www.CircuitsToday.com

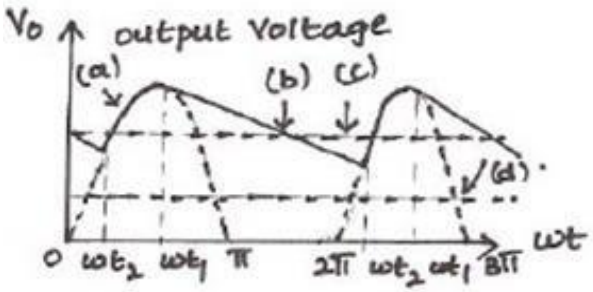
CAPACITOR FILTER WITH HWR



Cut In angle – wt_2

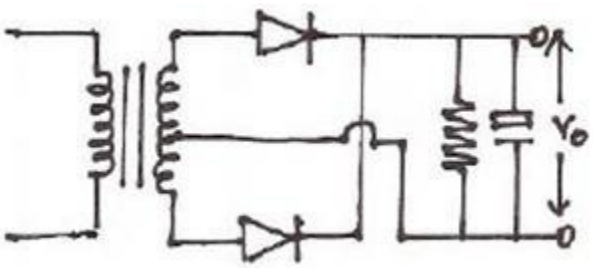
Cut out angle = Wt_1

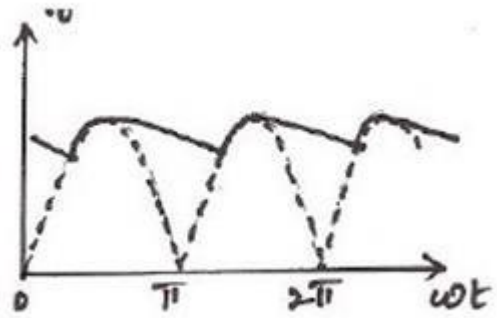
$Wt_1 = \pi - \tan^{-1} WCR_L$



(a) Capacitor charging through diode ($Wt_2 - Wt_1$)
(b) Capacitor discharging through R_L (Wt_1 to Wt_2)
(c) Average (DC) voltage with fitter
(d) Average (DC) voltage without fitter.

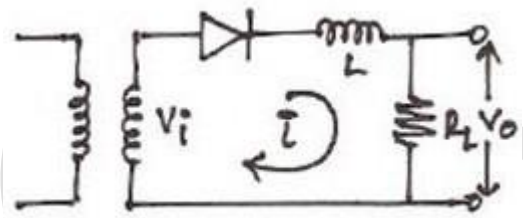
CAPACITOR FILTER WITH FWR

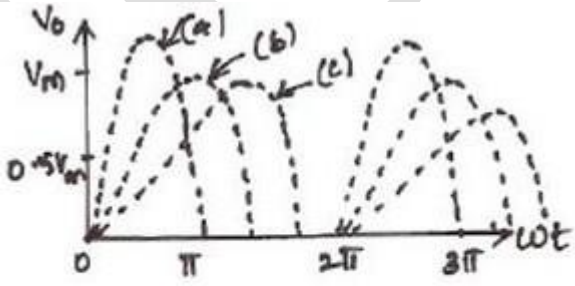




$$\text{Ripple factor } r = \frac{1}{4\sqrt{3}fCR_L}$$

Ripple freq $_{FWR}$ = 2 ripple freq $_{HWR}$.





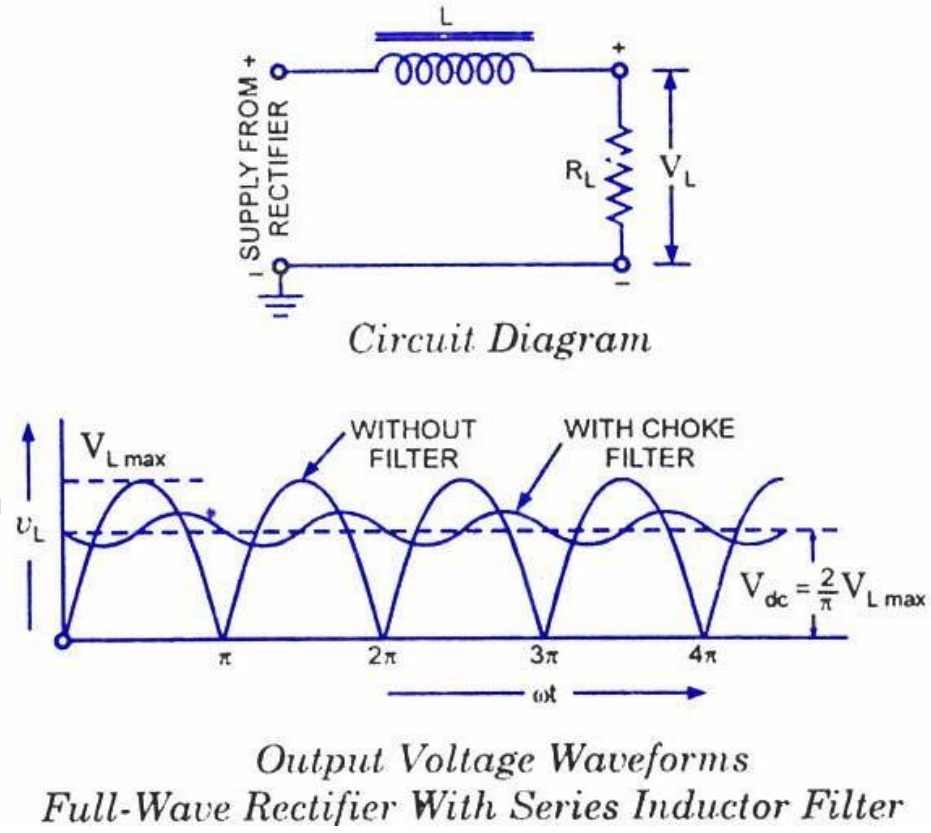
(a) $\frac{W_L}{R_L} = 0$ (b) $\frac{W_L}{R_L} = 1$ (c) $\frac{W_L}{R_L} = 5$.

The worthnoting points about shunt capacitor filter are:

1. For a fixed-value filter capacitance larger the load resistance RL larger will be the discharge time constant CRL and therefore, lower the ripples and more the output voltage. On the other hand lower the load resistance (or more the load current), lower will be the output voltage.

2. Similarly smaller the filter capacitor, the less charge it can hold and more it will discharge. Thus the peak-to-peak value of the ripple will increase, and the average dc level will decrease. Larger the filter capacitor, the more charge it can hold and the less it will discharge. Hence the peak-to-peak value of the ripple will be less, and the average dc level will increase. But, the maximum value of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be handled by a diode is limited by the figure quoted by the manufacturer. Thus the maximum value of the capacitance, that can be used in the shunt filter capacitor is limited.

Series Inductor Filter.



Circuit Diagram

Output Voltage Waveforms

Full-Wave Rectifier With Series Inductor Filter

In this arrangement a high value inductor or choke L is connected in series with the rectifier element and the load, as illustrated in figure. The filtering action of an inductor filter depends upon its property of opposing any change in the current flowing through it. When the output current of the rectifier

increases above a certain value, energy is stored in it in the form of magnetic field and this energy is given up when the output current falls below the average value. Thus by placing a choke coil in series with the rectifier output and load, any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor L.

The function of the inductor filter may be viewed in terms of impedances. The choke offers high impedance to the ac components but offers almost zero resistance to the desired dc components. Thus ripples are removed to a large extent. Nature of the output voltage without filter and with choke filter is shown in figure.

For dc (zero frequency), the choke resistance R_c in series with the load resistance R_L forms a voltage divider and dc voltage across the load is given as

where V_{dc} is dc voltage output from a full-wave rectifier. Usually choke coil resistance Rc, is much small than R_L and, therefore, almost entire of the dc voltage is available across the load resistance R_L.

Since the reactance of inductor increases with the increase in frequency, better filtering of the higher harmonic components takes place, so effect of third and higher harmonic voltages can be neglected.

As obvious from equation , if choke coil resistance R_c is negligible in comparison to load resistance R_L, then the entire dc component of rectifier output is available across 2 R_L and is equal to — $V_{L\ max}$. The ac voltage partly drops across X_L and partly over R_L.

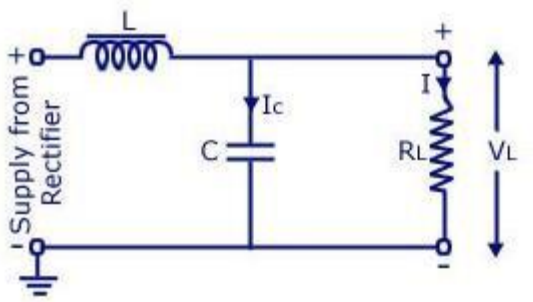
L-SECTION FILTER:

A simple series inductor reduces both the peakand effective values of the output current and output voltage. On the other hand a simple **shunt capacitor filter** reduces the ripple voltage but increases the diode current. The diode may get damaged due to large current and at the same time it causes greater heating of supply transformer resulting in reduced efficiency.

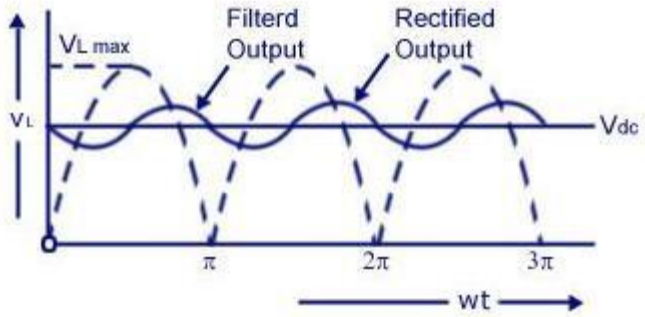
In an inductor filter, ripple factor increases with the increase in load resistance RL while in a capacitor filter it varies inversely with load resistance RL.

From economical point of view also, neither series inductor nor shunt capacitor type filters are suitable.

Practical **filter-circuits** are derived by combining the voltage stabilizing action of shunt capacitor with the current smoothing action of series choke coil. By using combination of inductor and capacitor ripple factor can be lowered, diode current can be restricted and simultaneously ripple factor can be made almost independent of load resistance (or load current). Two types of most commonly used combinations are choke-input or L-section filter-and capacitor-input or Pi-Filter.



Circuit Digram

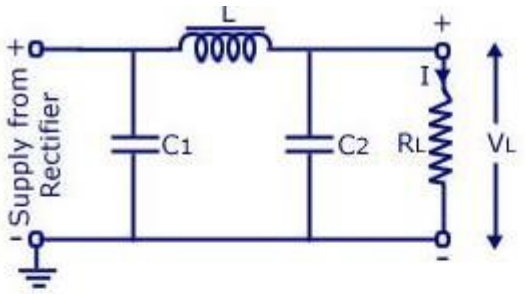


Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With Choke-Input Filter

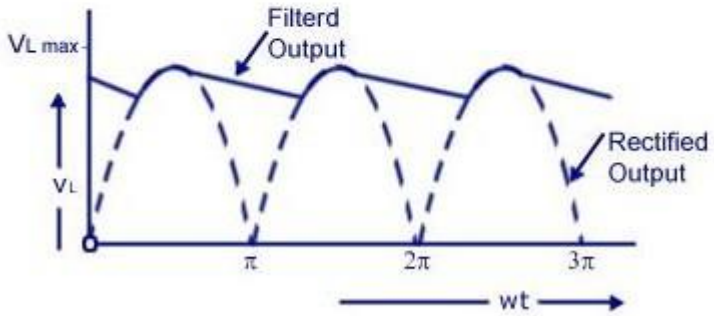
Choke-input filter is explained below:

Choke-input filter consists of a choke L connected in series with the rectifier and a capacitor C connected across the load . This is also sometimes called the L-section filter because in this arrangement inductor and capacitor are connected, as an inverted L. ln figure only one filter section is shown. But several identical sections are often employed to improve the smoothing action. (The choke L on the input side of the filter readily allows dc to pass but opposes the flow of ac components because its dc resistance is negligibly small but ac impedance is large. Any fluctuation that remains in the current even after passing through the choke are largely by-passed around the load by the shunt capacitor because Xc is much smaller than RL. Ripples can be reduced effectively by making XL greater than Xc at ripple frequency. However, a small ripple still remains in the filtered output and this is considered negligible if it than l%. The rectified and filtered output voltage waveforms from a full-wave re with choke-input filter are shown in figure.

Π-SECTION FILTER:



Circuit Digram



Rectified and Filtered Output Voltage Waveform
Full-wave Rectifier With capacitor Input Filter

Capacitor-Input or Pi-Filter.

Such a filter consists of a shunt capacitor C1 at the input followed by an L-section filter formed by series inductor L and shunt capacitor C_2. This is also called the *n-filter* because the shape of the circuit diagram for this filter appears like Greek letter *n (pi)*. Since the rectifier feeds directly into the capacitor so it is also called *capacitor input filter.*

As the rectified output is fed directly into a capacitor C1. Such a filter can be used with a half-wave rectifier (series inductor and L-section filters cannot be used with half-wave rectifiers). Usually electrolytic capacitors are used even though their capacitances are large but they occupy minimum space. Usually both capacitors C1 and C_2 are enclosed in one metal container. The metal container serves as, the common ground for the two capacitors.

A capacitor-input or *pi-* filter is characterized by a high voltage output at low current drains. Such a filter is used, if, for a given transformer, higher voltage than that can be obtained from an L-section filter is required and if low ripple than that can be obtained from a shunt capacitor filter or L-section filter is desired. In this filter, the input capacitor C1 is selected to offer very low reactance to the ripple frequency. Hence major part of filtering is accomplished by the input capacitor *C1*. Most of the remaining ripple is removed by the L-section filter consisting of a choke L and capacitor C_2.)

The action of this filter can *best* be understood by considering the action of L-section filter, formed by L and C_2, upon the triangular output voltage wave from the input capacitor C_1 The charging and discharging action of input capacitor C1 has already been discussed. The output voltage is roughly the same as across input capacitor C1 less the dc voltage drop in inductor. The ripples contained in this output are reduced further by L-section filter. The output voltage of pi-filter falls off rapidly with the increase in load-current and, therefore, the voltage regulation with this filter is very poor.

SALIENT FEATURES OF L-SECTION AND PI-FILTERS.

1. In pi-filter the dc output voltage is much larger than that can be had from an L-section filter with the same input voltage.

2.In pi-filter ripples are less in comparison to those in shunt capacitor or L-section filter. So smaller valued choke is required in a pi-filter in comparison to that required in L-section filter.

3.In pi-filter, the capacitor is to be charged to the peak value hence the rms current in supply transformer is larger as compared in case of L-section filter.

4.Voltage regulation in case of pi-filter is very poor, as already mentioned. So n-filters are suitable for fixed loads whereas L-section filters can work satisfactorily with varying loads provided a minimum current is maintained.

5.In case of a pi-filter PIV is larger than that in case of an L-section filter.

COMPARISON OF FILTERS

1) A capacitor filter provides Vm volts at less load current. But regulation is poor.

2) An Inductor filter gives high ripple voltage for low load currents. It is used

forhigh load currents

3) L – Section filter gives a ripple factor independent of load current. Voltage

Regulation can be improved by use of bleeder resistance

4) Multiple L – Section filter or π filters give much less ripple than the single L

–Section Filter.

SPECIAL PURPOSE SEMI-CONDUCTOR DEVICES

PRINCIPLE OF OPERATION OF SCR

A **silicon-controlled rectifier** (or **semiconductor-controlled rectifier**) is a four-layer solid state device that controls current. The name "silicon controlled rectifier" or **SCR** is General Electric's trade name for a type of thyristor. The SCR was developed by a team of power engineers led by Gordon Hall and commercialized by Frank W. "Bill" Gutzwiller in 1957.symbol of SCR is given below:

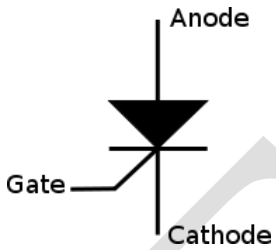


Fig 1.22: symbol of SCR

Construction of SCR

An SCR consists of four layers of alternating P and N type semiconductor materials. Silicon is used as the intrinsic semiconductor, to which the proper dopants are added. The junctions are either diffused or alloyed. The planar construction is used for low power SCRs (and all the junctions are diffused). The mesa type construction is used for high power SCRs. In this case, junction J2 is obtained by the diffusion method and then the outer two layers are alloyed to it, since the PNPN pellet is required to handle large currents. It is properly braced with tungsten or molybdenum plates to provide greater mechanical strength. One of these plates is hard soldered to a copper stud, which is threaded for attachment of heat sink. The doping of PNPN will depend on the application of SCR, since its characteristics are similar to those of the thyratron. Today, the term thyristor applies to the larger family of multilayer devices that exhibit bistable state-change behaviour, that is, switching either ON orOFF.

The operation of a SCR and other thyristors can be understood in terms of a pair of tightly coupled bipolar junction transistors, arranged to cause the self-latching action.The following figures are construction of SCR,its two transistor model and symbol respectively

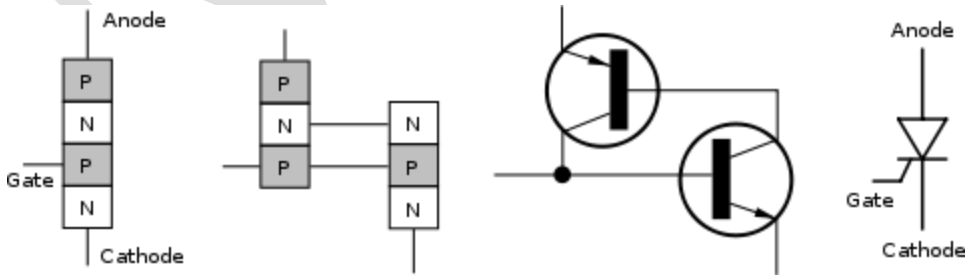


Fig 1.23: Construction, Two transistor model of SCR and symbol of SCR

SCR Working Principle

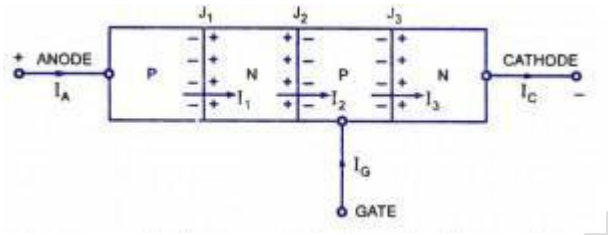


Fig 1.24: Current flow and voltage bias in an SCR

The **SCR** is a four-layer, three-junction and a three-terminal device and is shown in fig.1.24. The end P-region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. Ideally it remains off (voltage blocking state), or appears to have an infinite impedance until both the anode and gate terminals have suitable positive voltages with respect to the cathode terminal. The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero impedance in conduction state. For switching off or reverting to the blocking state, there must be no gate signal and the anode current must be reduced to zero. Current can flow only in one direction.

In absence of external bias voltages, the majority carrier in each layer diffuses until there is a built-in voltage that retards further diffusion. Some majority carriers have enough energy to cross the barrier caused by the retarding electric field at each junction. These carriers then become minority carriers and can recombine with majority carriers. Minority carriers in each layer can be accelerated across each junction by the fixed field, but because of absence of external circuit in this case the sum of majority and minority carrier currents must be zero.

A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which include the following terms:

The current I_x is due to

- Majority carriers (holes) crossing junction J_1
- Minority carriers crossing junction J_1
- Holes injected at junction J_2 diffusing through the N-region and crossing junction J_1 and
- Minority carriers from junction J_2 diffusing through the N-region and crossing junction J_1.

V I characteristics of SCR:

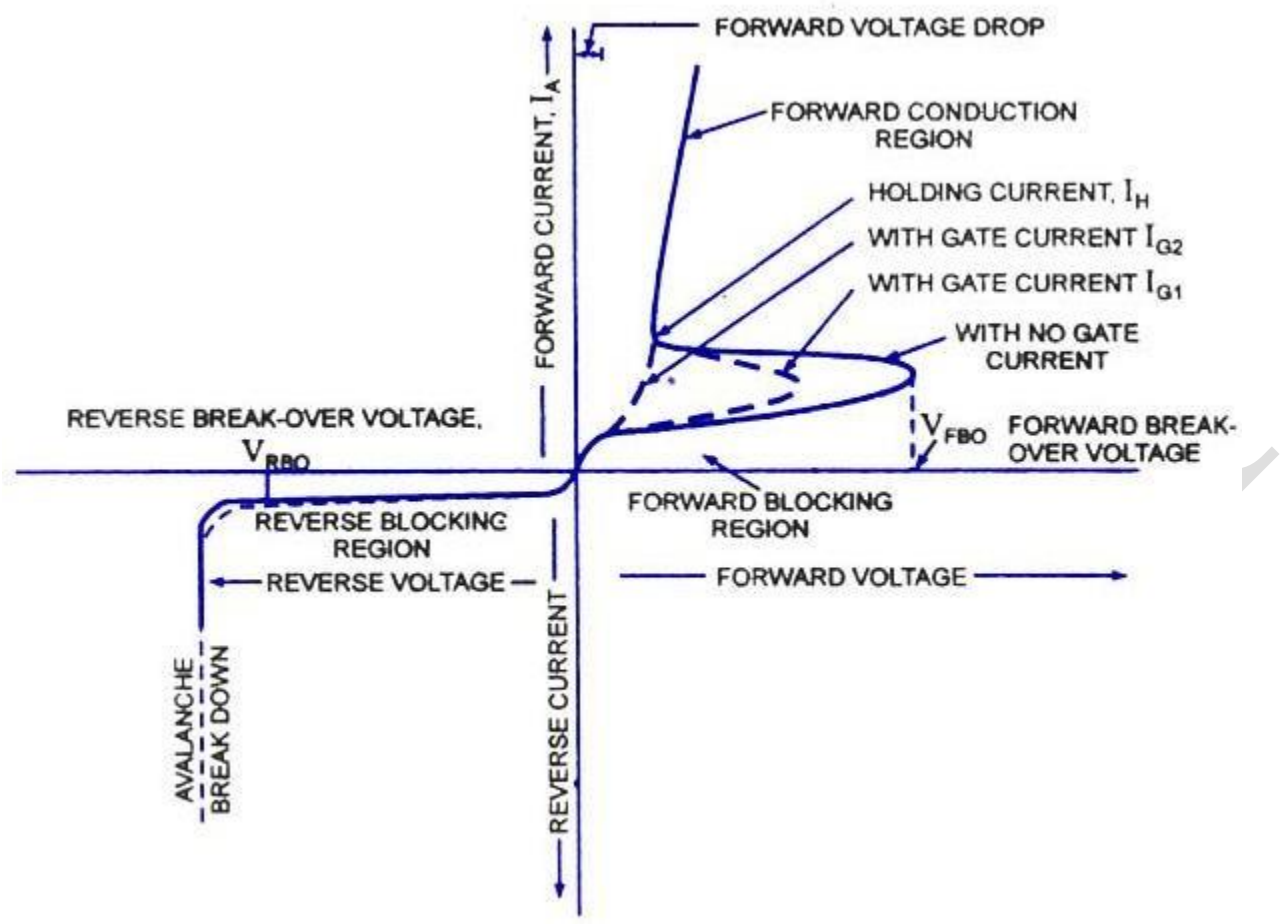


Fig 1.25: V-I characteristics of SCR

As already mentioned, the **SCR** is a four-layer device with three terminals, namely, the anode, the cathode and the gate. When the anode is made positive with respect to the cathode, junctions J_1 and $J_3$are forward biased and junction J_2 is reverse-biased and only the leakage current will flow through the device. The SCR is then said to be in the forward blocking state or in the forward mode or off state. But when the cathode is made positive with respect to the anode, junctions J_1 and J_3 are reverse-biased, a small reverse leakage current will flow through the SCR and the SGR is said to be in the reverse blocking state or in reverse mode.

When the anode is positive with respect to cathode i.e. when the SCR is in forward mode, the SCR does not conduct unless the forward voltage exceeds certain value, called the forward breakover voltage, V_{FB0}. In non-conducting state, the current through the SCR is the leakage current which is very small and is negligible. If a positive gate current is supplied, the SCR can become conducting at a voltage much lesser than forward break-over voltage. The larger the gate current, lower the break-over voltage. With sufficiently large gate current, the SCR behaves identical to PN rectifier. Once the SCR is switched on, the forward voltage drop across it is suddenly reduced to very small value, say about 1 volt. In the conducting or on-state, the current through the SCR is limited by the external impedance.

When the anode is negative with respect to cathode, that is when the SCR is in reverse mode or in blocking state no current flows through the SCR except very small leakage current of the order of few micro-amperes. But if the reverse voltage is increased beyond a certain value, called the reverse break-over voltage, V_{RB0} avalanche break down takes place. Forward break-over voltage V_{FB0} is usually higher than reverse breakover voltage, V_{RBO}.

From the foregoing discussion, it can be seen that the SCR has two stable and reversible operating states. The change over from off-state to on-state, called turn-on, can be achieved by increasing the forward voltage beyond V_{FB0}. A more convenient and useful method of turn-on the device employs the gate drive. If the forward voltage is less than the forward break-over voltage, V_{FB0}, it can be turned-on by applying a positive voltage between the gate and the cathode. This method is called the gate control. Another very important feature of the gate is that once the SCR is triggered to on-state the gate loses its control.

The switching action of gate takes place only when

(i) SCR is forward biased i.e. anode is positive with respect to cathode, and

(ii) Suitable positive voltage is applied between the gate and the cathode.

Once the SCR has been switched on, it has no control on the amount of current flowing through it. The current through the SCR is entirely controlled by the external impedance connected in the circuit and the applied voltage. There is, however, a very small, about 1 V, potential drop across the SCR. The forward current through the SCR can be reduced by reducing the applied voltage or by increasing the circuit impedance. There is, however, a minimum forward current that must be maintained to keep the SCR in conducting state. This is called the holding current rating of SCR. If the current through the SCR is reduced below the level of holding current, the device returns to off-state or blocking state.

The SCR can be switched off by reducing the forward current below the level of holding current which may be done either by reducing the applied voltage or by increasing the circuit impedance.

Note : The gate can only trigger or switch-on the SCR, it cannot switch off.

Alternatively the SCR can be switched off by applying negative voltage to the anode (reverse mode), the SCR naturally will be switched off.

Here one point is worth mentioning, the SCR takes certain time to switch off. The time, called the turn-off time, must be allowed before forward voltage may be applied again otherwise the device will switch-on with forward voltage without any gate pulse. The turn-off time is about 15 micro-seconds, which is immaterial when dealing with power frequency, but this becomes important in the inverter circuits, which are to operate at high frequency.

Merits of SCR

1. Very small amount of gate drive is required.
2. SCRs with high voltage and current ratings are available.3.On state losses of SCR are less.

Demerits of SCR

1.Gate has no control,once SCR is turned on.
2.External circuits are required for turning it off.
3.Operationg frequencies are low.
4.Additional protection circuits are required.

Application of SCRs

SCRs are mainly used in devices where the control of high power, possibly coupled with high voltage, is demanded. Their operation makes them suitable for use in medium to high-voltage AC power control applications, such as lamp dimming, regulators and motor control.

SCRs and similar devices are used for rectification of high power AC in high-voltage direct current power transmission

PRINCIPLE OF OPERATION AND CHARACTERISTICS OF TUNNEL DIODE

A **tunnel diode** or **Esaki diode** is a type of semiconductor diode which is capable of very fast operation, well into the microwave frequency region, by using quantum mechanical effects.

It was invented in August 1957 by Leo Esaki when he was with Tokyo Tsushin Kogyo, now known as Sony. In 1973 he received the Nobel Prize in Physics, jointly with Brian Josephson, for discovering the electron tunneling effect used in these diodes. Robert Noyce independently came up with the idea of a tunnel diode while working for William Shockley, but was discouraged from pursuing it.

Fig 1.19: Tunnel diode schematic symbol

These diodes have a heavily doped p–n junction only some 10 nm (100 Å) wide. The heavy doping results in a broken bandgap, where conduction band electron states on the n-side are more or less aligned with valence band hole states on the p-side. Tunnel diodes were manufactured by Sony for the first time in 1957 followed by General Electric and other companies from about 1960, and are still made in

low volume today. Tunnel diodes are usually made from germanium, but can also be made in gallium arsenide and silicon materials. They can be used as oscillators, amplifiers, frequency converters and detectors.Tunnelling Phenomenon:

In a conventional semiconductor diode, conduction takes place while the p–n junction is forward biased and blocks current flow when the junction is reverse biased. This occurs up to a point known as the "reverse breakdown voltage" when conduction begins (often accompanied by destruction of the device). In the tunnel diode, the dopant concentration in the p and n layers are increased to the point where the **reverse breakdown voltage** becomes **zero** and the diode conducts in the reverse direction. However, when forward-biased, an odd effect occurs called "quantum mechanical tunnelling" which gives rise to a region where an *increase* in forward voltage is accompanied by a *decrease* in forward current. This negative resistance region can be exploited in a solid state version of the dynatron oscillator which normally uses a tetrode thermionic valve (or tube).

Forward bias operation

Under normal forward bias operation, as voltage begins to increase, electrons at first tunnel through the very narrow p–n junction barrier because filled electron states in the conduction band on the n-

side become aligned with empty valence band hole states on the p-side of the p-n junction. As voltage increases further these states become more misaligned and the current drops – this is called *negative resistance* because current decreases with increasing voltage. As voltage increases yet further, the diode begins to operate as a normal diode, where electrons travel by conduction across the p–n junction, and no longer by tunneling through the p–n junction barrier. Thus the most importantoperating region for a tunnel diode is the negative resistance region.

Reverse bias operation

When used in the reverse direction they are called **back diodes** and can act as fast rectifiers with zero offset voltage and extreme linearity for power signals (they have an accurate square law characteristic in the reverse direction).

Under reverse bias filled states on the p-side become increasingly aligned with empty states on the n-side and electrons now tunnel through the pn junction barrier in reverse direction – this is the Zener effect that also occurs in zener diodes.

Technical comparisons

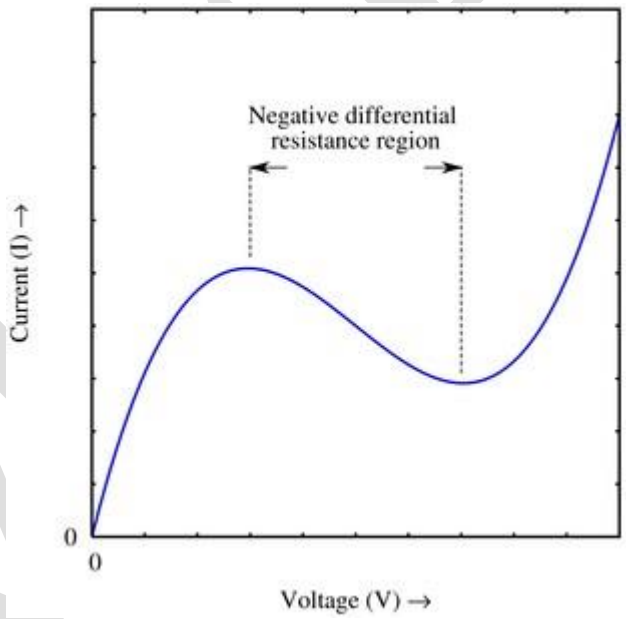


Fig 1.20a: current-voltage characteristic of tunnel diode

A rough approximation of the VI curve for a tunnel diode, showing the negative differential resistance region. The Japanese physicist Leo Esaki invented the tunnel diode in 1958.It consists of a p-n junction with highly doped regions. Because of the thinness of the junction, the electrons can pass through the potential barrier of the dam layer at a suitable polarization, reaching the energy states on the other sides of the junction. The current-voltage characteristic of the diode is represented in Figure 1.20a. In this sketch *i p* and *Up* are the peak, and *iv* and *Uv* are the valley values for the current and voltage

respectively. The form of this dependence can be qualitatively explained by considering the tunneling processes that take place in a thin p-n junction.

Energy band structure of tunnel diode:

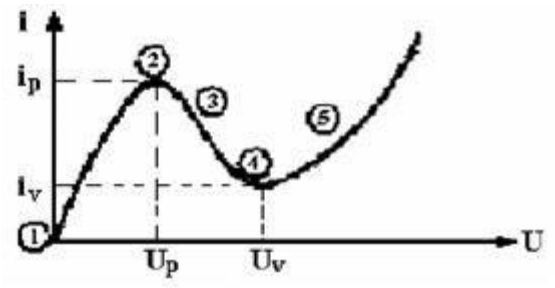


Figure 1.

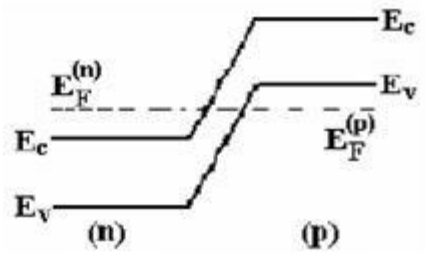
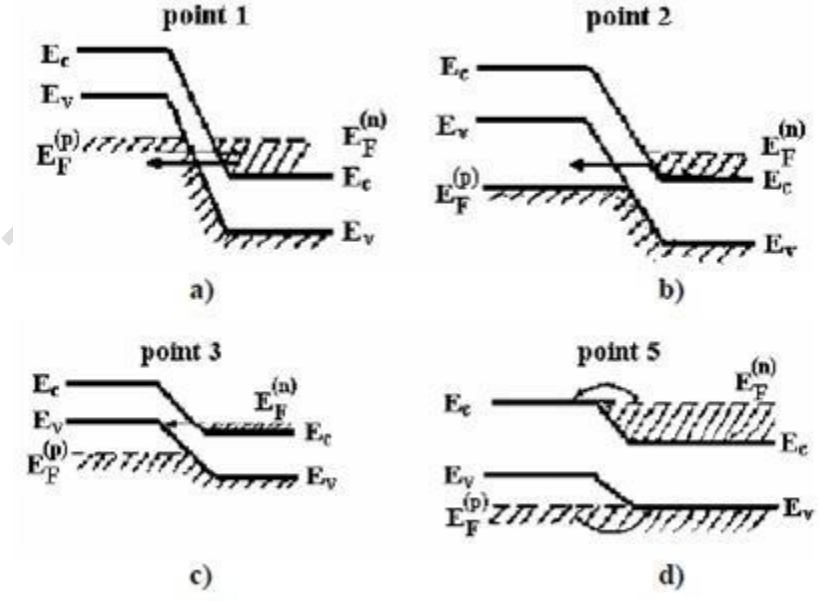


Fig 1.20b Energy band structure of tunnel diode

For the degenerated semiconductors, the energy band diagram at thermal equilibrium is presented in Figure 1.20b.

In Figure 1.20c the tunneling processes in different points of the current voltage characteristic for the tunnel diode are presented.



Advantages of tunnel diodes:

- Environmental immunity i.e. peak point is not a function of temperature.
- Low cost.
- Low noise.
- Low power consumption.
- High speed i.e. tunneling takes place very fast at the speed of light in the order of nanoseconds
- Simplicity i.e. a tunnel diode can be used along with a d.c supply and a few passive elements to obtain various application circuits.

Applications for tunnel diodes:

- local oscillators for UHF television tuners
- Trigger circuits in oscilloscopes
- High speed counter circuits and very fast-rise time pulse generator circuits
- The tunnel diode can also be used as low-noise microwave amplifier.

PHOTO DIODE

The photo diode is a semiconductor p-n junction device whose region of operation is limited to the reverse biased region.The figure below shows the symbol of photodiode

Fig 1.26:Symbol of photodiode.

Principle of operation:

A photodiode is a type of photo detector capable of converting light into either current or voltage, depending upon the mode of operation. The common, traditional solar cell used to generate electric solar power is a large area photodiode. A photodiode is designed to operate in reverse bias. The deletion region width is large. Under normal conditions it carries small reverse current due to minority charge carriers. When light is incident through glass window on the p-n junction, photons in the light bombard the p-n junction and some energy s imparted to the valence electrons. So valence electrons

break covalent bonds and become free electrons. Thus more electron-hole pairs are generated. Thus total number of minority charge carriers increases and hence reverse current increases.This is the basic principle of operation of photo diode.

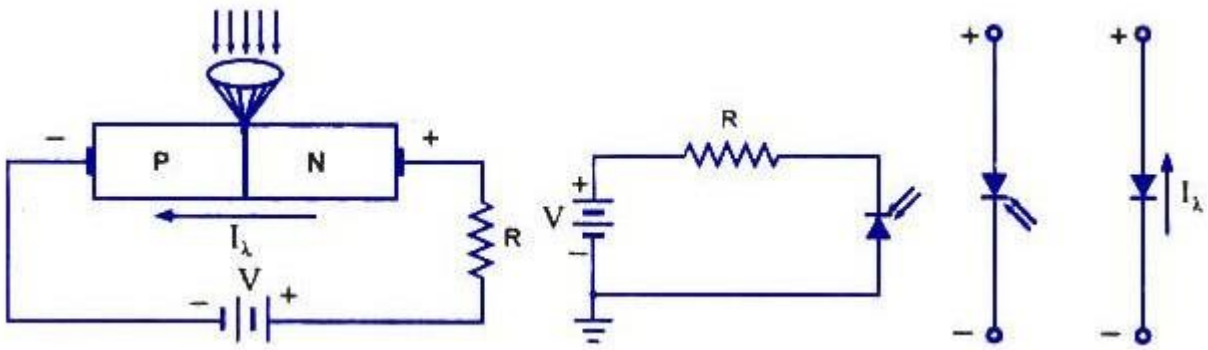


Fig 1.27: Basic Biasing Arrangement and construction of photodiode and symbols

Characteristics of photodiode:

When the P-N junction is reverse-biased, a reverse saturation current flows due to thermally generated holes and electrons being swept across the junction as the minority carriers. With the increase in temperature of the junction more and more hole-electron pairs are created and so the reverse saturation current I_0 increases. The same effect can be had by illuminating the junction. When light en- ergy bombards a P-N junction, it dislodges valence electrons. The more light striking the junction the larger the reverse current in a diode. It is due to generation of more and more charge carriers with the increase in level of illumination. This is clearly shown in ‘ figure for different intensity levels. The dark current is the current that exists when no light is incident. It is to be noted here that current becomes zero only with a positive applied bias equals to V_Q. The almost equal spacing between the curves forthe same increment in luminous flux reveals that the reverse saturation current I_0 increases linearly with the luminous flux as shown in figure. Increase in reverse voltage does not increase the reverse current significantly, because all available charge carriers are already being swept across the junction. For reducing the reverse saturation current I_0 to zero, it is necessary to forward bias the junction by an amount equal to barrier potential. Thus the photodiode can be used as a photoconductive device.

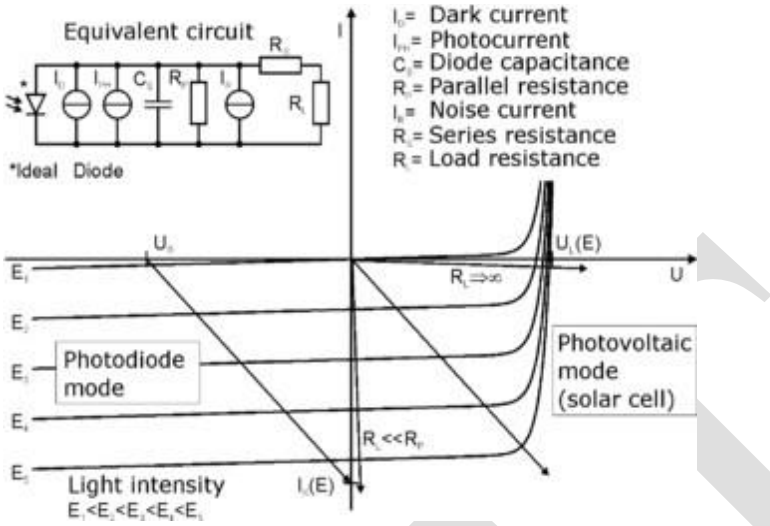


Fig 1.28: characteristics of photodiode

On removal of reverse bias applied across the photodiode, minority charge carriers continue to be swept across the junction while the diode is illuminated. This has the effect of increasing the concentration of holes in the P-side and that of electrons in the N-side But the barrier potential is negative on the P-side and positive on the N-side, and was created by holes flowing from P to N-side and electrons from N to P-side during fabrication of junction. Thus the flow of minority carriers tendsto reduce the barrier potential.

When an external circuit is connected across the diode terminals, the minority carrier; return to the original side via the external circuit. The electrons which crossed the junction from P to N-side nowflow out through the N-terminal and into the P-terminal This means that the device is behaving as a voltage cell with the N-side being the negative terminal and the P-side the positive terminal. Thus, the photodiode is & photovoltaic device as well as photoconductive device.

Advantages:

The advantages of photodiode are:
1.It can be used as variable resistance
device.2.Highly sensitive to the light.
3.The speed of operation is very high.

Disadvantages:

1.Temperature dependent dark
current.2.poor temperature stability.
3.Current needs amplification for driving other circuits.

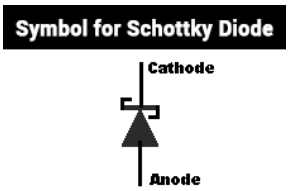
Applications:

1.Alarm system.
2.counting system.

Schottky Diode

The schottky diode is a type of metal – semiconductor junction diode, which is also known as hot-carrier diode, low voltage diode or schottky barrier diode. The schottky diode is formed by the junction of a semiconductor with a metal. Schottky diode offers fast switching action and has a low forward voltage drop. As we are aware that in a PN junction diode, p-type and n-type are joined together to form a PN junction. Whereas, in a Schottky diode metals like platinum or aluminum are used instead of P type semiconductors.

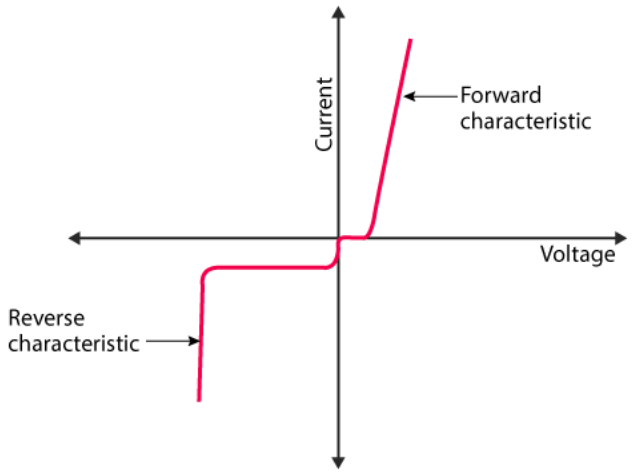
The symbol for the Schottky barrier diode is based around the basic diode circuit symbol. The circuit symbol of the Schottky diode is shown in the figure.



Schottky Diode Symbol

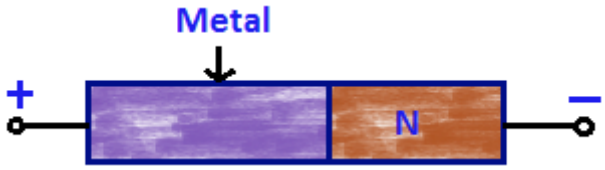
V-I Characteristics of Schottky Diode

The V-I characteristics of Schottky diodes are very much similar to the PN junction diode. Current is the dependent variable while voltage is the independent variable in the Schottky diode. The forward voltage drop of the Schottky diode is low between 0.2 to 0.3 volts.



Working of a Schottky Diode

- The operation relies on the principle that the electrons in different materials have different potential energy.
- N-type semiconductors have higher potential energy than electrons of metals.

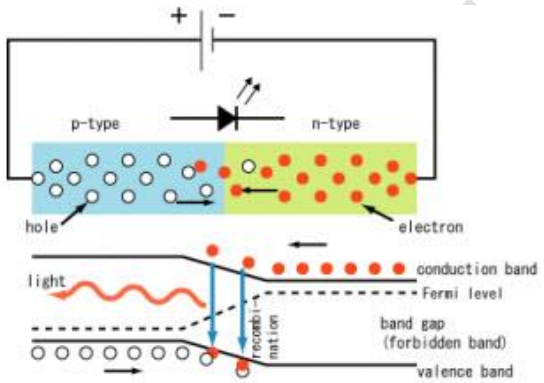


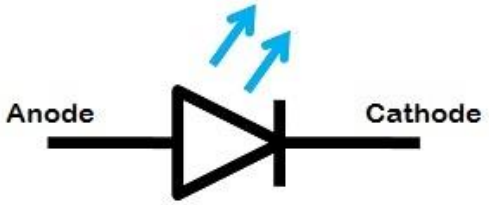
- When these two are brought into contact, there is a flow of electrons in both directions across the metal-semiconductor interface.
- A voltage is applied to the Schottky so that the metal is positive when compared to the semiconductor.
- The voltage opposes the built-in potential and makes the current flow easy.

Construction and working of LED

A light-emitting diode (LED) is a semiconductor device that emits light when an electric current flows through it. When current passes through an LED, the electrons recombine with holes emitting light in the process. LEDs allow the current to flow in the forward direction and block the current in the reverse direction.

LED symbol is similar to a diode symbol except for two small arrows that specify the emission of light, thus it is called LED (light-emitting diode). The LED includes two terminals namely anode (+) and the cathode (-). The LED symbol is shown below.





LED Symbol

The construction of LED is very simple because it is designed through the deposition of three semiconductor material layers over a substrate. These three layers are arranged one by one where the top region is a P-type region, the middle region is active and finally, the bottom region is N-type. The three regions of semiconductor material can be observed in the construction. In the construction, the P-type region includes the holes; the N-type region includes elections whereas the active region includes both holes and electrons.

When the voltage is not applied to the LED, then there is no flow of electrons and holes so they are stable. Once the voltage is applied then the LED will forward biased, so the electrons in the N-region and holes from P-region will move to the active region. This region is also known as the depletion region. Because the charge carriers like holes include a positive charge whereas electrons have a negative charge so the light can be generated through the recombination of polarity charges.

Working Principle of LED

The working principle of the Light-emitting diode is based on the quantum theory. The quantum theory says that when the electron comes down from the higher energy level to the lower energy level then, the energy emits from the photon. The photon energy is equal to the energy gap between these two energy levels. If the PN-junction diode is in the forward biased, then the current flows through the diode.

The flow of current in the semiconductors is caused by the flow of holes in the opposite direction of current and the flow of electrons in the direction of the current. Hence there will be recombination due to the flow of these charge carriers.

The recombination indicates that the electrons in the conduction band jump down to the valence band. When the electrons jump from one band to another band the electrons will emit the electromagnetic energy in the form of photons and the photon energy is equal to the forbidden energy gap.

UNIT III

BIPOLAR JUNCTION TRANSISTOR

INTRODUCTION

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. The BJT is analogues to vacuum triode and is comparatively smaller in size. It is used as amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

CONSTRUCTION OF BJT AND ITS SYMBOLS

The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

- 1. Active Region - the transistor operates as an amplifier and $I_c = \beta . I_b$
- 2. Saturation - the transistor is "fully-ON" operating as a switch and $I_c = I_{(saturation)}$
- 3. Cut-off - the transistor is "fully-OFF" operating as a switch and $I_c = 0$

Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type(fig 1).

Bipolar Transistor Construction

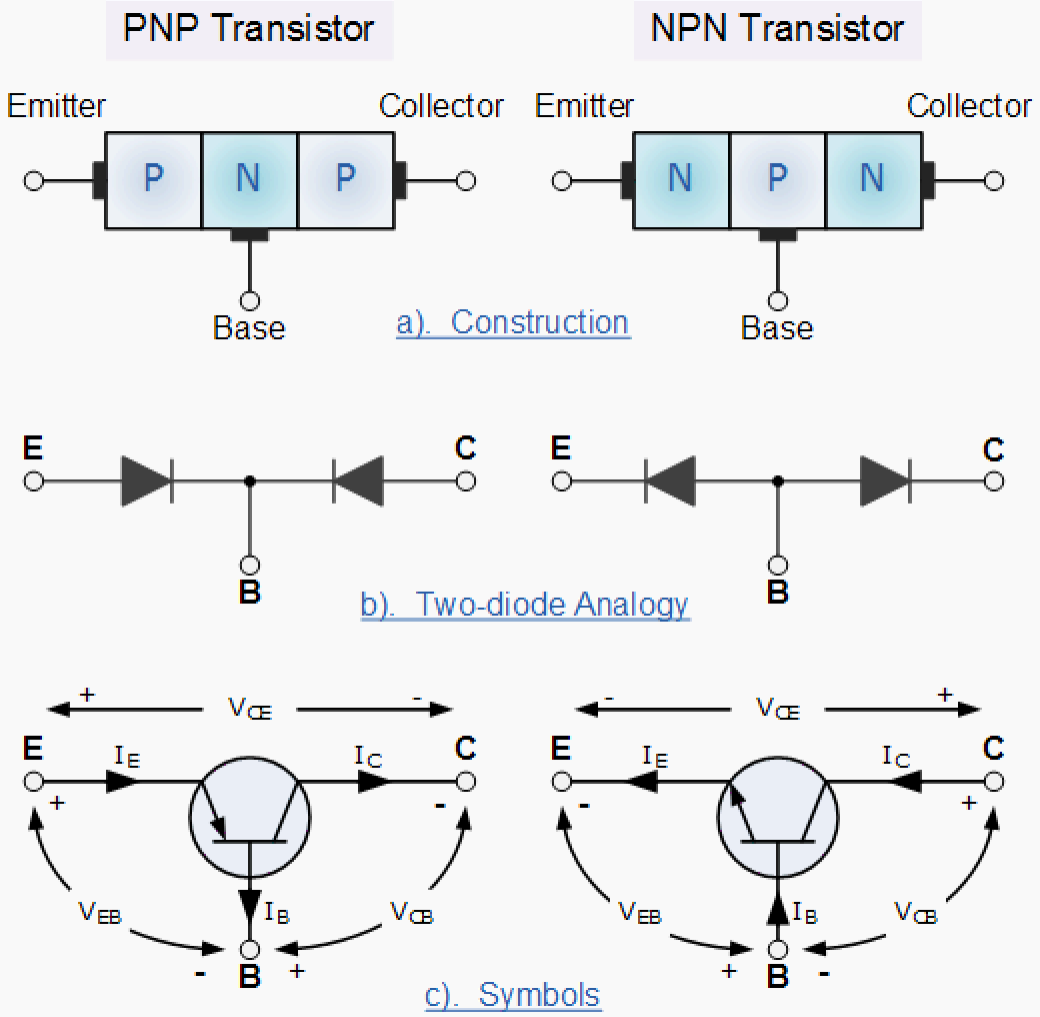


Fig 3.1 Bipolar Junction Transistor Symbol

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

TRANSISTOR CURRENT COMPONENTS:

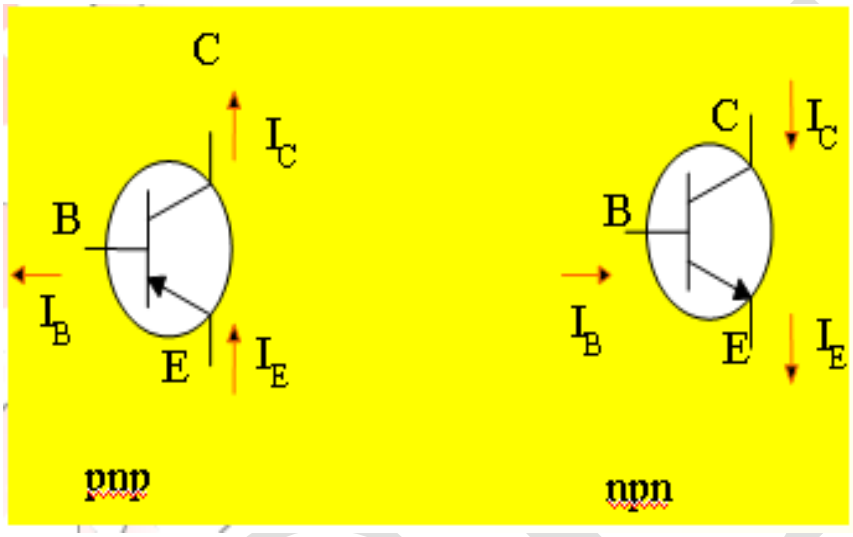


Fig 3.2 Bipolar Junction Transistor Current Components

The above fig 3.2 shows the various current components, which flow across the forward biased emitter junction and reverse- biased collector junction. The emitter current I_E consists of hole current I_{PE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into emitter).The ratio of hole to electron currents, I_{pE} / I_{nE} , crossing the emitter junction is proportional to the ratio of the conductivity of the p material to that of the n material. In a transistor, the doping of that of the emitter is made much larger than the doping of the base. This feature ensures (in p-n-p transistor) that the emitter current consists an almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter do not contribute carriers, which can reach the collector.

Not all the holes crossing the emitter junction J_E reach the the collector junction J_C

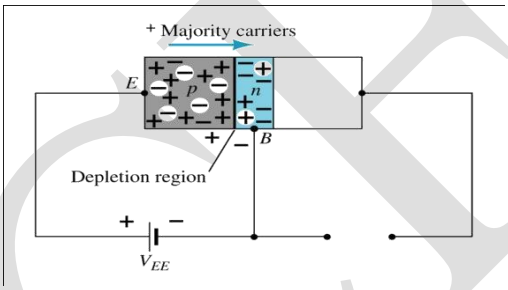
Because some of them combine with the electrons in n-type base. If I_{pC} is hole current at junction J_C there must be a bulk recombination current (I_{PE}- I_{pC}) leaving the base.

Actually, electrons enter the base region through the base lead to supply those charges, which have been lost by recombination with the holes injected in to the base across J_E. If the emitter were open circuited so that $I_E=0$ then I_{pC} would be zero. Under these circumstances, the base and collector current I_C would equal the reverse saturation current I_{CO}. If $I_E \neq 0$ then

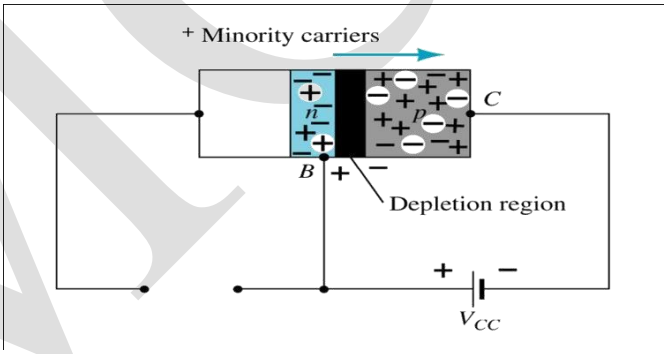
$I_C = I_{CO} - I_{pC}$

For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in opposite direction. Assumed referenced direction for I_{CO} i.e. from right to left, then for a p-n-p transistor, I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive.The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same if the roles played by the electron and hole are interchanged.

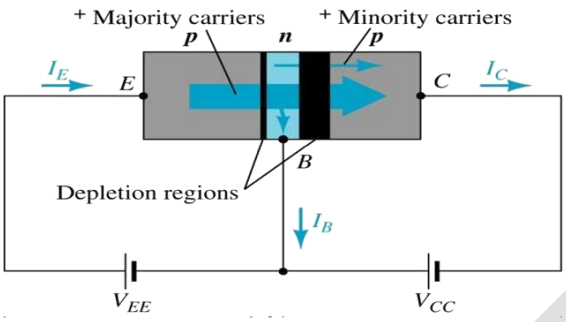
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



3.3a Forward-biased junction of a pnp transistor



3.3b Reverse-biased junction of a pnp transistor



c Both biasing potentials have been applied to a pnp transistor and resulting majority and minority carrier flows indicated.

Majority carriers (+) will diffuse across the forward-biased p-n junction into the n-type material.

A very small number of carriers (+) will through n-type material to the base terminal. Resulting IB istypically in order of microamperes.

The large number of majority carriers will diffuse across the reverse-biased junction into the p-type material connected to the collector terminal

Applying KCL to the transistor :

$$I_E = I_C + I_B$$

The comprises of two components – the majority and minority carriers

$$I_C = I_{Cmajority} + I_{COminority}$$

I_{CO} – I_C current with emitter terminal open and is called leakage current

Various parameters which relate the current components is given below

Emitter efficiency:

$$\gamma = \frac{currentofinjectedcarriersatJ_E}{totalemittercurrent}$$

$$\gamma = \frac{I_{PE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\beta^* = \frac{injectedca\ rriercurrentreachingJ_C}{injectedca\ rrierncurrentatJ_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut-off)to I_E the large signal current gain of a common base transistor.

$$\alpha = \frac{-(I_C - I_{CO})}{I_E}$$

Since $I_{C\ and}$ I_E have opposite signs, then α, as defined, is always positive. Typically numerical values ofα lies in the range of 0.90 to 0.995

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \quad \alpha = \beta * \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio α^* is unity. α^* is the ratio of total current crossing J_C to hole arriving at the junction.

Bipolar Transistor Configurations

As the **Bipolar Transistor** is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

- 1. Common Base Configuration - has Voltage Gain but no Current Gain.
- 2 Common Emitter Configuration - has both Current and Voltage Gain.
- 3. Common Collector Configuration - has Current Gain but no Voltage Gain.

COMMON-BASE CONFIGURATION

Common-base terminology is derived from the fact that the : base is common to both input and outputof t configuration. base is usually the terminal closest to or at ground potential. Majority carriers can cross the reverse-biased junction because the injected majority carriers will appear as minority carriersin the n-type material. All current directions will refer to conventional (hole) flow and the arrows in all electronic symbols have a direction defined by this convention.

Note that the applied biasing (voltage sources) are such as to establish current in the directionindicated for each branch.

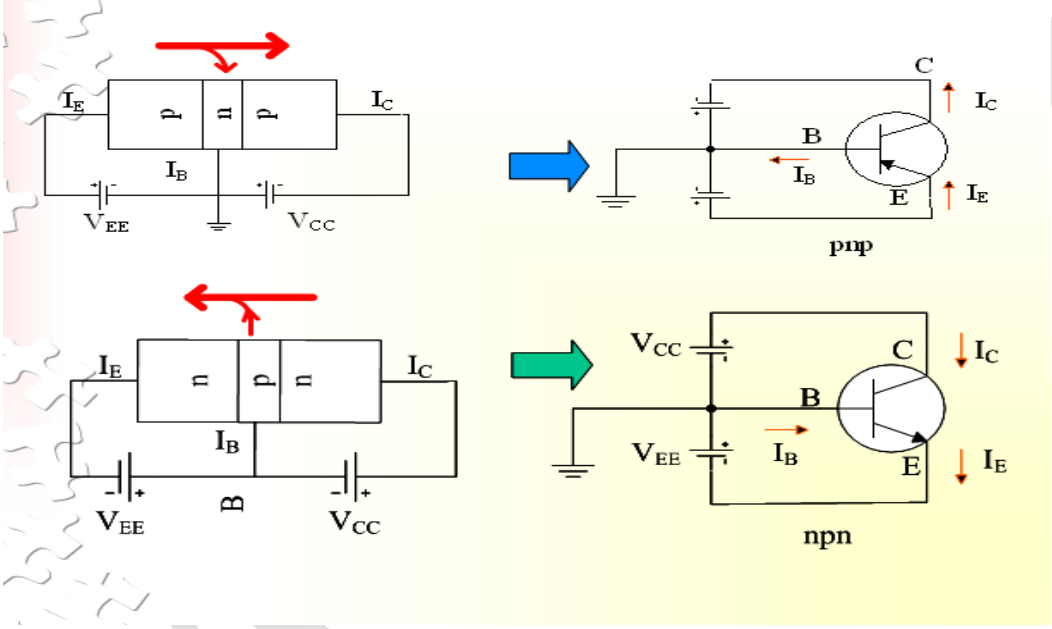


Fig 3.4 CB Configuration

To describe the behavior of common-base amplifiers requires two set of characteristics:

1. Input or driving point characteristics.
2. Output or collector characteristics

The output characteristics has 3 basic regions:

- Active region –defined by the biasing arrangements
- Cutoff region – region where the collector current is 0A

- Saturation region- region of the characteristics to the left of V_{CB} = 0V

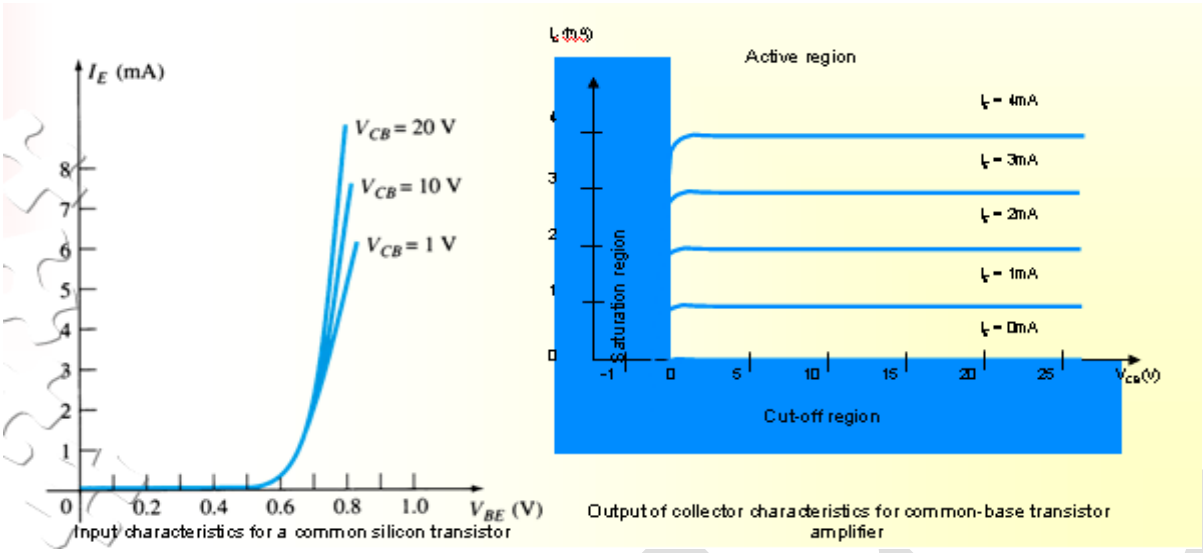


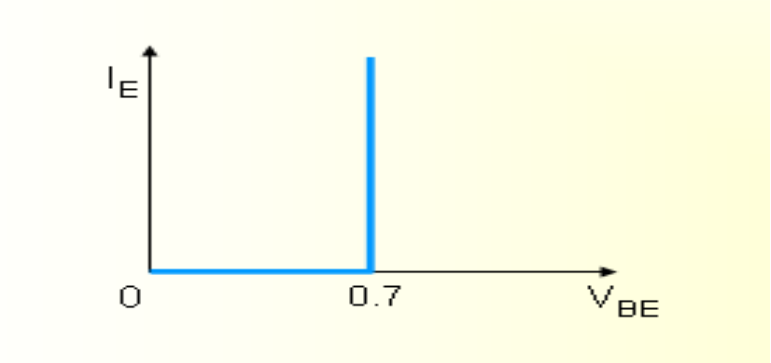
Fig 3.5 CB Input-Output Characteristics

Active region	Saturation region	Cut-off region
•IE increased, Ic increased •BE junction forward bias and CB junction reverse bias •Refer to the graf, Ic ≈ IE •Ic not depends on VCB •Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in VCB will cause big different to Ic • The allocation for this region is to the left of VCB= 0 V.	• Region below the line of IE=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

The curves (output characteristics) clearly indicate that a first approximation to the relationship between IE and IC in the active region is given by

$I_C \approx IE$

Once a transistor is in the 'on' state, the base-emitter voltage will be assumed to beV_{BE} = 0.7V



In the dc mode the level of I_C and I_E due to the majority carriers are related by a quantity called alpha

$\alpha = \alpha_{dc}$

$I_C = \alpha I_E + I_{CBO}$

It can then be summarize to $I_C = \alpha I_E$ (ignore I_{CBO} due to small value)

For ac situations where the point of operation moves on the characteristics curve, an ac alpha definedby

α_{ac}

Alpha a common base current gain factor that shows the efficiency by calculating the current percent from current flow from emitter to collector. The value of α is typical from 0.9 ~ 0.998.

Biasing: Proper biasing CB configuration in active region by approximation $I_C \approx I_E$ ($I_B \approx 0$ uA)

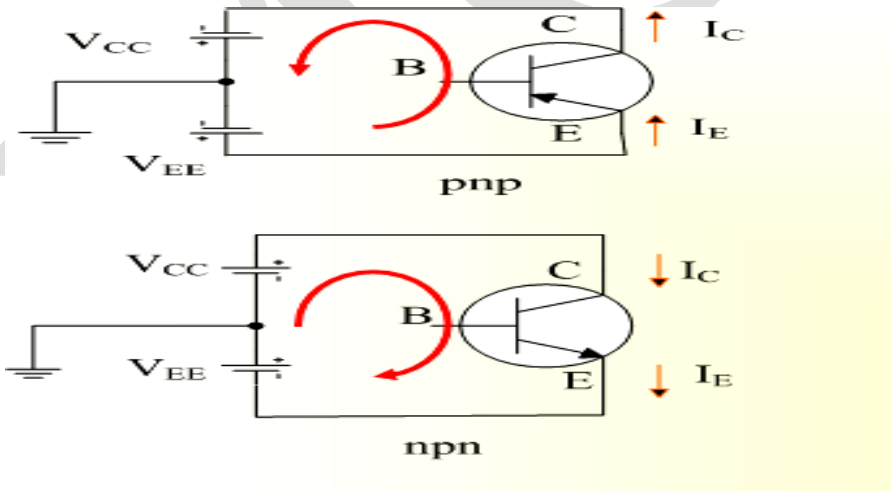


Fig 3.6 CE Configuration

TRANSISTOR AS AN AMPLIFIER

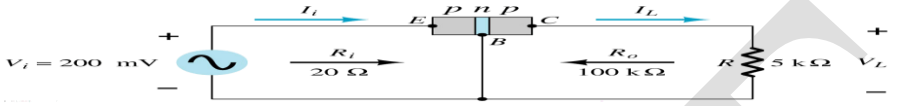


Fig 3.7 Basic Transistor Amplifier Circuit

Common-Emitter Configuration

It is called common-emitter configuration since : emitter is common or reference to both input and output terminals.emitter is usually the terminal closest to or at ground potential.

Almost amplifier design is using connection of CE due to the high gain for current and voltage.

Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region

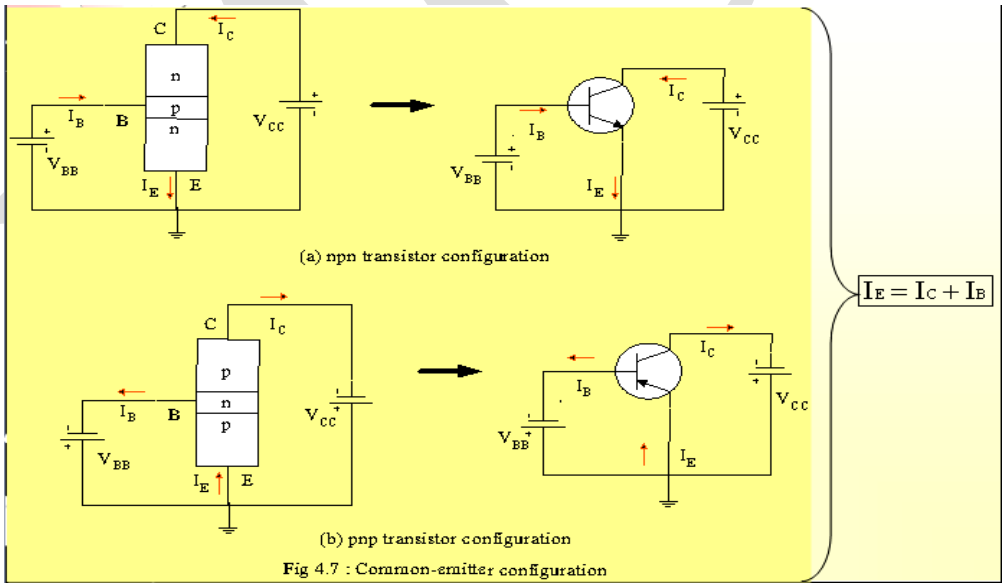


Fig 3.8 CE Configuration

I_B is microamperes compared to miliamperes of I_C.

I_B will flow when V_{BE} > 0.7V for silicon and 0.3V for

germaniumBefore this value I_B is very small and no I_B.

Base-emitter junction is forward bias Increasing V_{CE} will reduce I_B for different values.

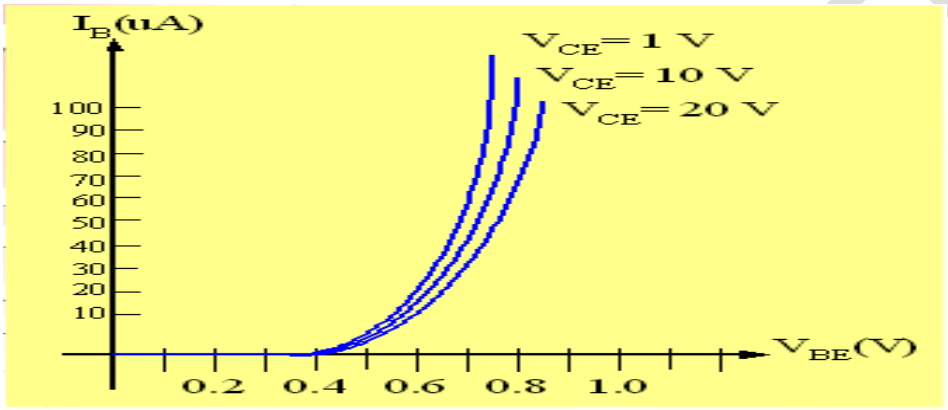


Fig 3.9a Input characteristics for common-emitter npn transistor

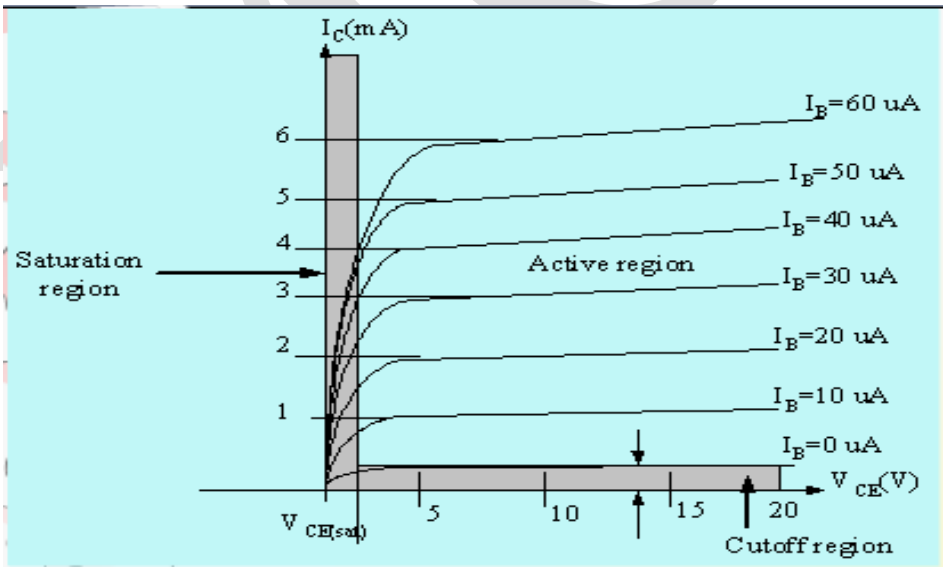


Fig 3.9b Output characteristics for common-emitter npn transistor

For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing

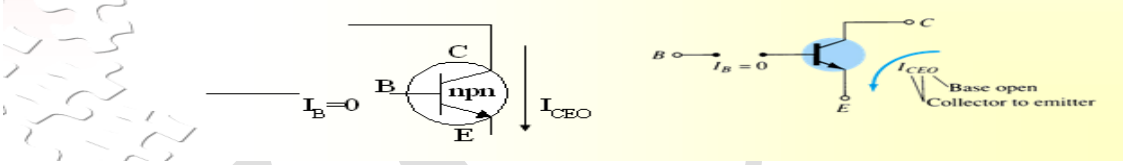
of $V_{CE}V_{CE} > V_{CESAT}$ I_C not totally depends on V_{CE} → constant I_C

I_B(uA) is very small compare to I_C (mA). Small increase in I_B cause big increase

in I_CI_B=0 A → I_{CEO} occur.

Noticing the value when I_C=0A. There is still some value of current flows.

Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below I_B=0μA is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • I_B=0, I_C not zero, during this condition $I_C=I_{CEO}$ where is this current flow when B-E is reverse bias.

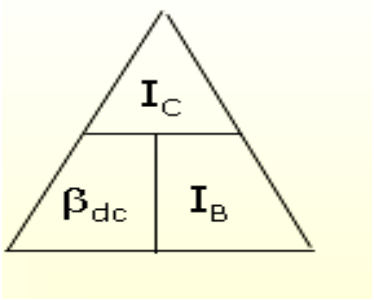


Beta (β) or amplification factor

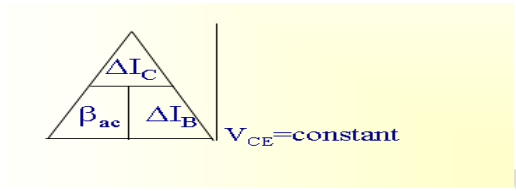
The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (βdc) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation:

$$30 < \beta dc < 300 \rightarrow 2N3904$$

On data sheet, β_{dc}=*hfe* with *h* is derived from ac hybrid equivalent cct. FE are derived from forward-current amplification and common-emitter configuration respectively.



For ac conditions, an ac beta has been defined as the changes of collector current (I_C) compared to the changes of base current (I_B) where I_C and I_B are determined at operating point. On data sheet, β_{ac}=*hfe* It can defined by the following equation:



From output characteristics of commonemitter configuration, find β_{ac} and β_{dc} with an

Operating point at I_B=25 μA and V_{CE} =7.5V

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{ce}\ =\ \text{constant}}$$

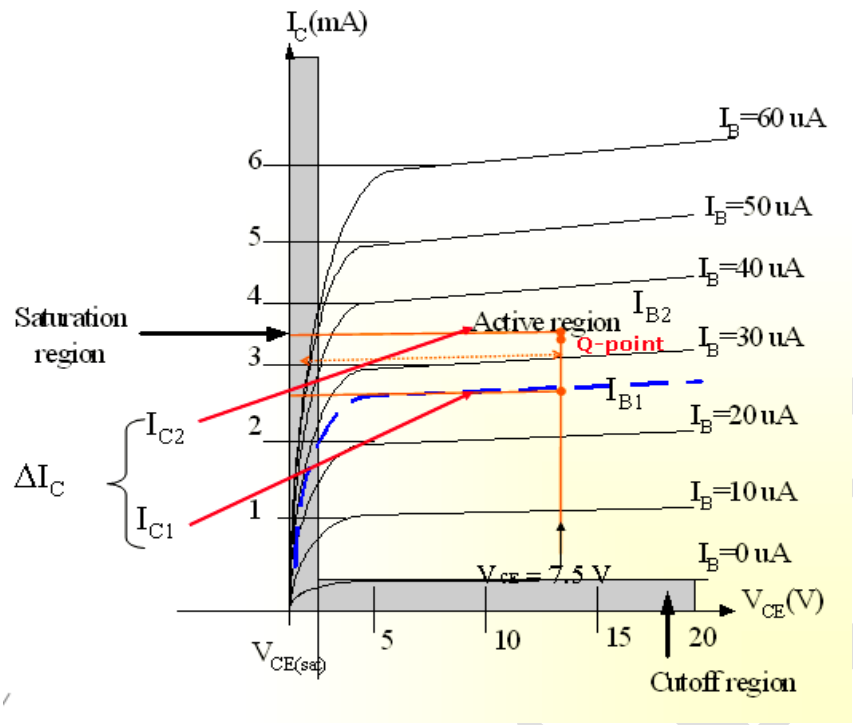
$$= \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{3.2\,m - 2.2\,m}{30\,\mu - 20\,\mu}$$

$$= \frac{1\,m}{10\,\mu} = 100$$

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$= \frac{2.7\,m}{25\,\mu}$$

$$= 108$$



Relationship analysis between α and β

CASE 1

$I_E = I_C + I_B$ (1)

subtitute equ. $I_C = \beta I_B$ into (1) we get

$$\underline{\underline{I_E = (\beta + 1) I_B}}$$

CASE 2

known : $\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$ (2)

known : $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$ (3)

subtitute (2) and (3) into (1) we get,

$$\underline{\underline{\alpha = \frac{\beta}{\beta + 1}}} \quad \text{and} \quad \underline{\underline{\beta = \frac{\alpha}{1 - \alpha}}}$$

COMMON – COLLECTOR CONFIGURATION

Also called emitter-follower (EF). It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point.The output voltageis obtained at emitter terminal. The input characteristic of common-collector configuration is

similar with common-emitter. configuration.Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.

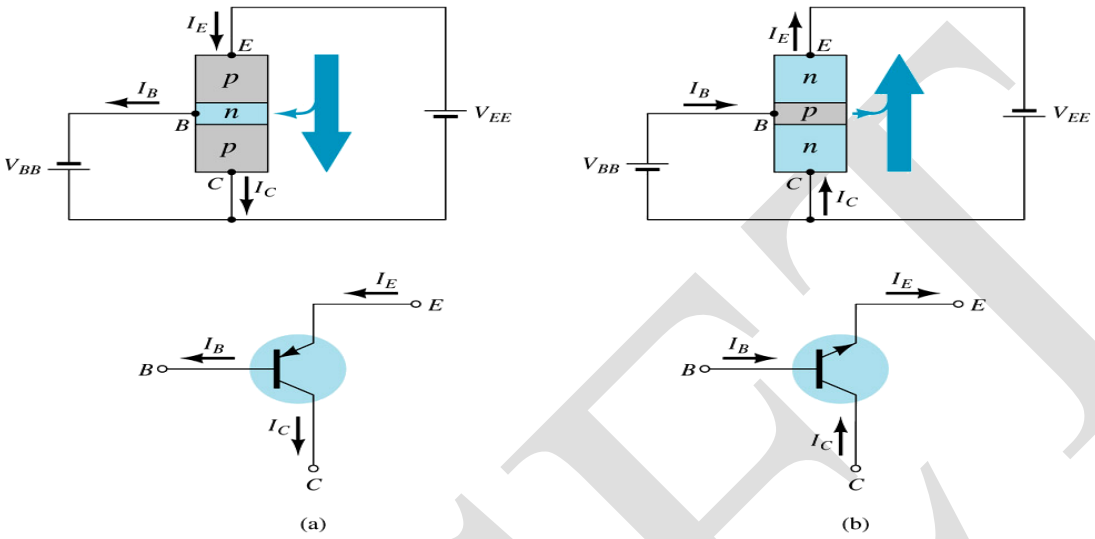


Fig 3.10 CC Configuration

For the common-collector configuration, the output characteristics are a plot of I_E vs V_{CE} for a range of values of I_B

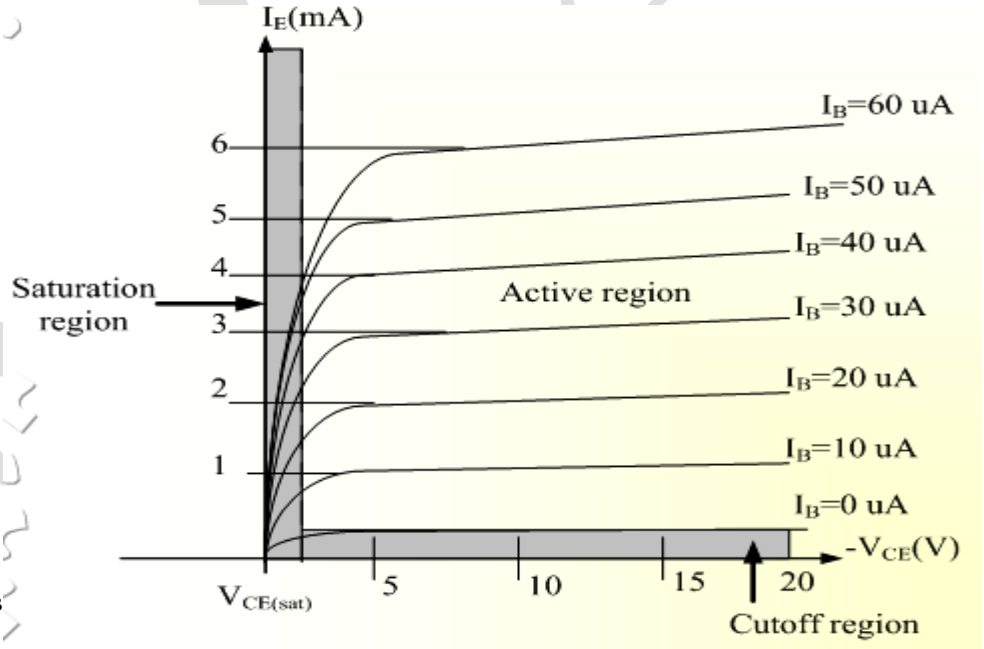


Fig 3.11 Output Characteristics of CC Configuration for npn Transistor

Limits of opearation

Many BJT transistor used as an amplifier. Thus it is important to notice the limits of operations.At least 3 maximum values is mentioned in data sheet.

There are:

a) Maximum power dissipation at collector: P_{Cmax} or P_D

b) Maximum collector-emitter voltage: V_{CEmax} sometimes named as $V_{BR(CEO)}$) or V_{CEO}.

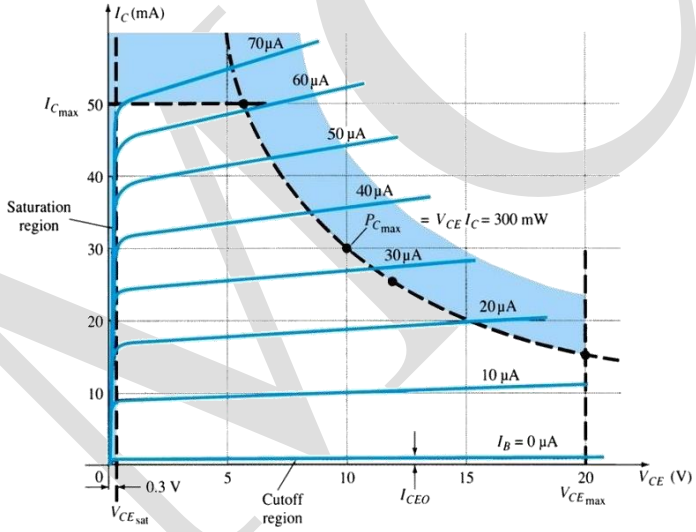
c) Maximum collector current: ICmax

There are few rules that need to be followed for BJT transistor used as an amplifier. The rules are: transistor need to be operate in active region!

$I_C < I_{Cmax}$

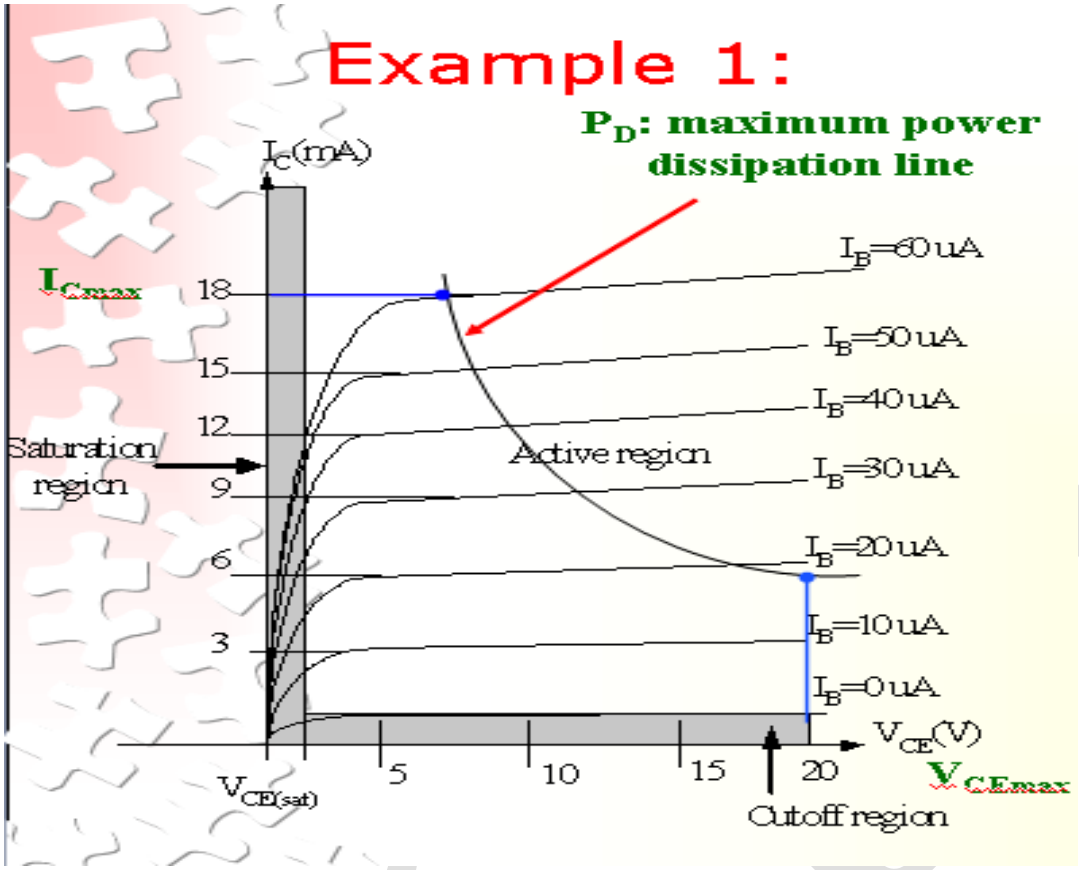
$P_C <$

P_{Cmax}



Note: V_{CE} is at maximum and I_C is at minimum (I_{CMAX}=I_{CEO}) in the cutoff region. I_C is at maximum and V_{CE} is at minimum (V_{CE} max = V_{cesat} = V_{CEO}) in the saturation region. The transistor

operates in the active region between saturation and cutoff.



Refer to the fig. Example; A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

Step1:

The maximum collector power dissipation,

P_D=I_{CMAX} x V_{CEmax}= 18m x 20 = 360 mW

Step 2:

At any point on the characteristics the product of and must be equal to 360 mW.Ex.

1. If choose I_{Cmax}= 5 mA, substitute into the (1), we get

$V_{CEmax}I_{Cmax}$= 360 mW

V_{CEmax}(5 m)=360/5=7.2

V

Ex.2. If choose V_{CEmax}=18 V, substitute into (1), we

get$V_{CEmax}I_{Cmax}$= 360 mW

(10) I_{CMAX}=360m/18=<u>20 mA</u>

Derating P_{Dmax}

P_{DMAX} is usually specified at 25°C.

The higher temperature goes, the less is P_{DMAX}

Example;A derating factor of 2mW/°C indicates the power dissipation is reduced 2mW each degree centigrade increase of temperature.

BJT HYBRID MODEL

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in **fig. 1**.

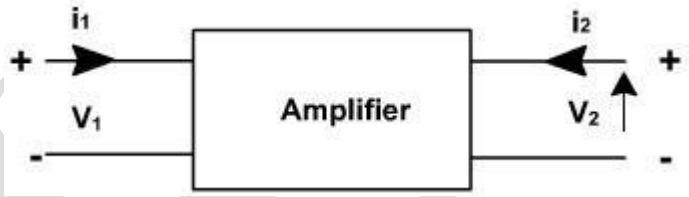


Fig. 1

A two-port network is represented by four external variables: voltage V_1 and current I_1 at the input port, and voltage V_2 and current I_2 at the output port, so that the two-port network can be treated as a black box modeled by the relationships between the four variables,V_1,V_2, I_1,I_2 . Out of four variables two can be selected as are independent variables and two are dependent variables.The dependent variables can be expressed interns of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z-parameters)
2. Admittance parameters (y-parameters)
3. Hybrid parameters (h-parameters)

z-parameters

A two-port network can be described by z-parameters as

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0}$$

Input impedance with output port open circuited

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

Output impedance with input port open circuited

Y-parameters

A two-port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}$$

Input admittance with output port short circuited

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}$$

Reverse transfer admittance with input port short circuited

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}$$

Forward transfer admittance with output port short circuited

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

Output admittance with input port short circuited

Hybrid parameters (h-parameters)

If the input current I1 and output voltage V2 are taken as independent variables, the dependent variables V1 and I2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where h_{11}, h_{12}, h_{21}, h_{22} are called as hybrid parameters.

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$$

Input impedance with o/p port short circuited

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

output impedence with i/p port open circuited

THE HYBRID MODEL FOR TWO PORT

NETWORK:

Based on the definition of hybrid parameters the mathematical model for two pert networks known ash-parameter model can be developed. The hybrid equations can be written as:

$$V_1 = h_i I_1 + h_r V_2$$

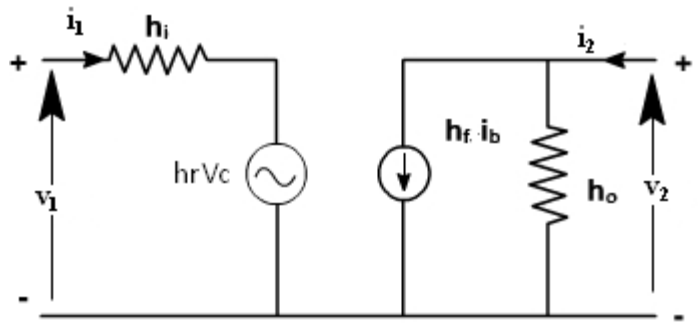
$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended
by the **IEEE Standards**:

***i*=11= input** ***o* = 22 = output**

***f* =21 = forward transfer *r* = 12 = reverse transfer)**

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff'svoltage and current laws for input and output ports.



If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} ,h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in fig. 2.

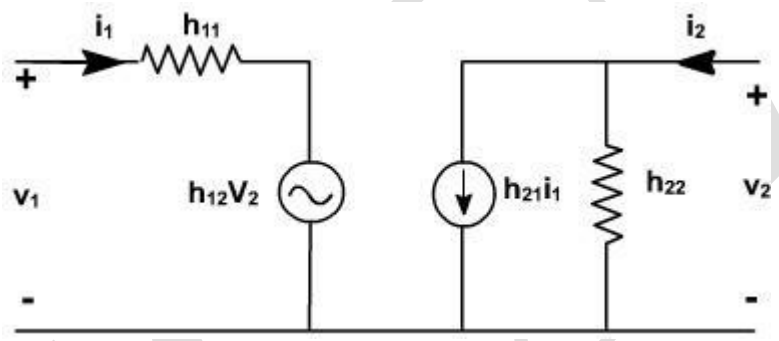


Fig. 2

TRANSISTOR HYBRID MODEL:

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in fig. 3. The variables, i_B, i_C ,v_C, and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B, I_C as dependent variables.

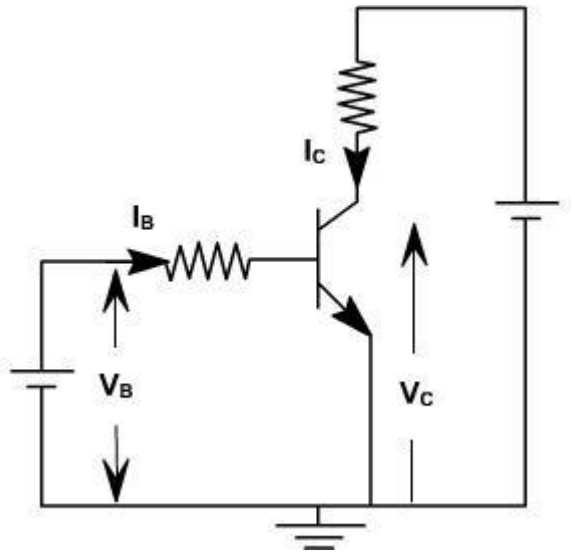


Fig. 3

$V_B = f1\ (i_B$

$,v_C\ )I_C = f2$

$(i_B\ ,v_C)$.

Using Taylor 's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} \Delta v_C$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B, Δv_C, Δi_B, Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as v_B, i_C, i_B ,v_C

$$\therefore v_b = h_{ie}\, i_B + h_{re}\, v_C$$
$$i_C = h_{fe}\, i_B + h_{oe}\, v_b$$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_c} = \left.\frac{\partial v_B}{\partial i_B}\right|_{v_c}; \qquad h_{re} = \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_c} = \left.\frac{\partial i_C}{\partial i_B}\right|_{v_c}; \qquad h_{oe} = \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

The model for CE configuration is shown in fig. 4.

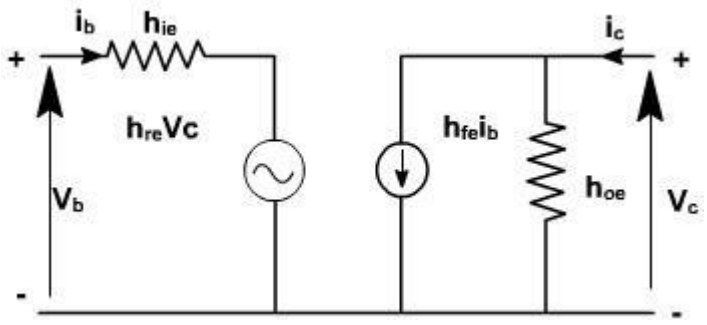


Fig. 4

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. Fig. 5, shows the output characteristics of CE amplifier.

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

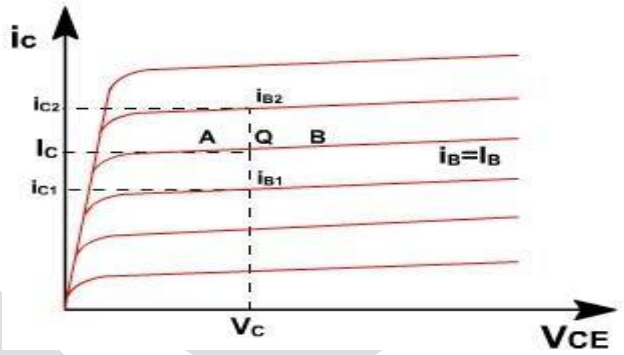


Fig. 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{i_B}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic atthe operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left.\frac{\Delta V_B}{\Delta i_B}\right|_{V_C}$$

h_{ie} is the slope of the appropriate input on fig. 6, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left.\frac{\Delta V_B}{\Delta V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

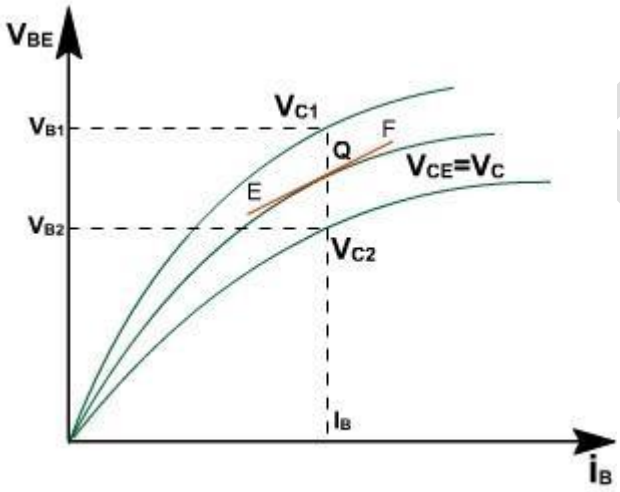


Fig. 6

A vertical line on the input characteristic represents constant base current. The parameter hre can be obtained from the ratio (V_{B2}– V_{B1}) and (V_{C2}– V_{C1}) for at Q.

Typical CE h-parametersof transistor 2N1573 are given below:

h_{ie} = 1000 ohm.
h_{re} = 2.5 * 10 –4
h_{fe} = 50
h_{oe} = 25 A / V

ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in **fig. 1** and to bias the transistor properly.

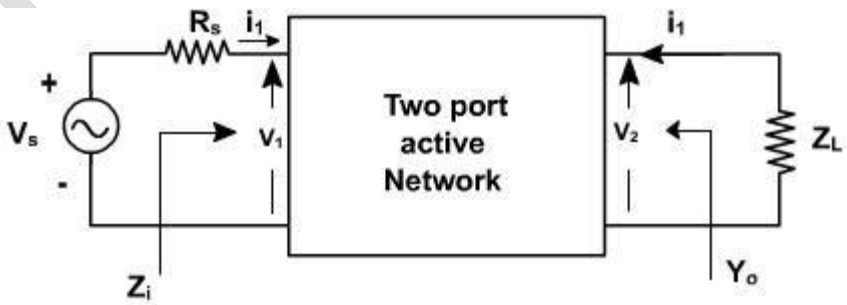
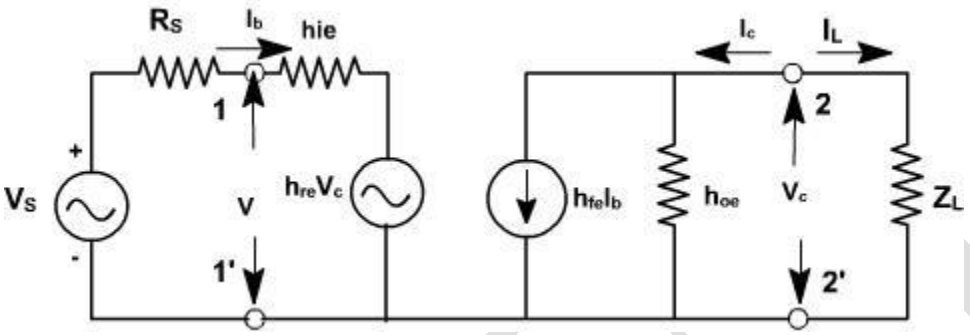


Fig. 1

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedence h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in fig. 2. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedence, voltage gain, and output impedence.



Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

Input impedence:

The impedence looking into the amplifier input terminals (1,1') is the input impedance Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = -\frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance:

$$Y_O = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe}\frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $\quad R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0.$

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_O = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V \cdot \frac{Z_i}{Z_i + R_s}$$

It is defined as $$= \frac{A_i Z_L}{Z_i + R_s}$$

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_S in parallel with a resistance R_S as shown in fig. 3.

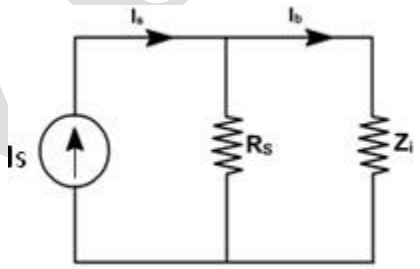


Fig. 3

In this case, overall current gain A_{IS} is defined as

$$A_{I_s} = \frac{I_L}{I_s}$$

$$= -\frac{I_c}{I_s}$$

$$= -\frac{I_c}{I_b} * \frac{I_b}{I_s} \qquad \left(I_b = \frac{I_s * R_s}{R_s + Z_i}\right)$$

$$= A_I * \frac{R_s}{R_s + Z_i}$$

If $R_s \to \infty$, $A_{Is} \to A_I$

h-parameters

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example fig. 4 hrc in terms of CE parameter can be obtained as follows.

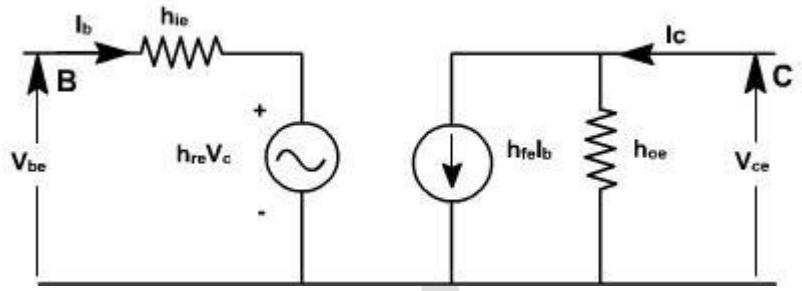


Fig. 4

For CE transistor configuaration

Vbe = hie Ib + hre Vce

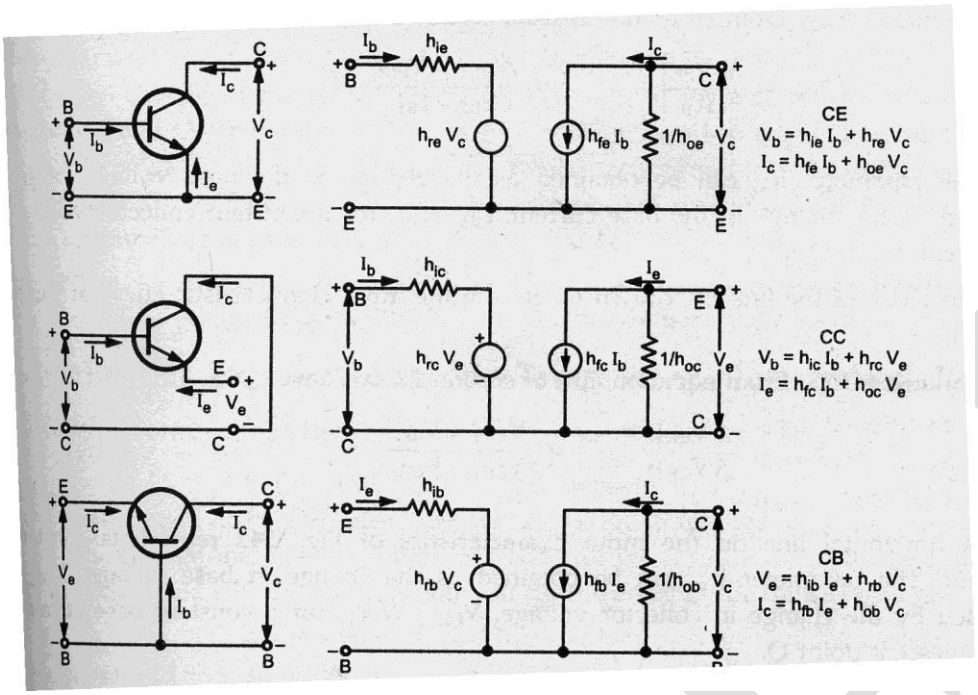
Ic = h fe Ib + hoe Vce

The circuit can be redrawn like CC transistor configuration as shown in fig. 5.

Vbc = hie Ib + hrc Vec

Ic = hfe Ib + hoe Vec

hybrid model for transistor in three different configurations



Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100 Ω	1100 Ω	22 Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	25 μA/V	25 μA/V	0.49 μA/V

Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

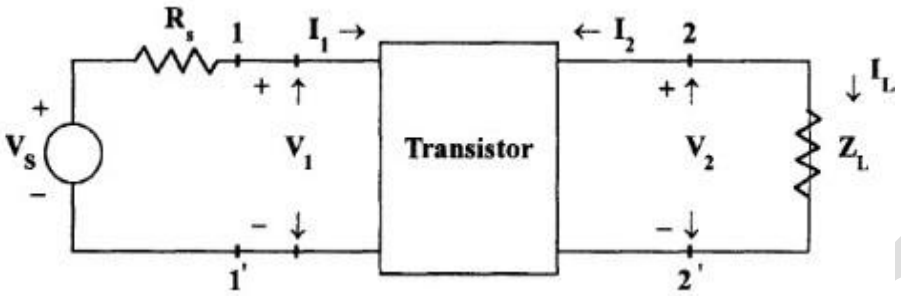


Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range.The input is sinusoidal and I_1,V_1,I_2 and V_2 are phase quantities

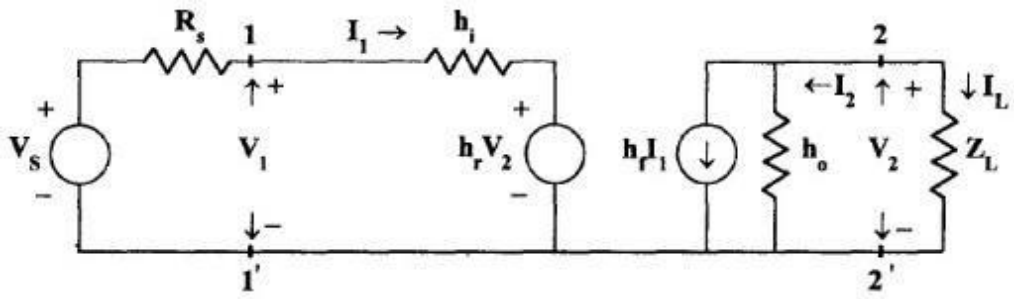


Fig. 1.5 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current,i.e,

$$A_i = I_L / I_1 = -I_2 / I_1$$

From the circuit of Fig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -$

$I_2 Z_L$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$I_2 + I_2 Z_L h_o = h_f I_1$

$I_2(1+ Z_L h_o) = h_f$

I_1

$A_i = -I_2 / I_1 = - h_f / (1+ Z_L h_o)$

Therefore,

$A_i = - h_f / (1+ Z_L h_o)$

Input Impedence (Z_i)

In the circuit of Fig , R_S is the signal source resistance .The impedence seen when looking into the amplifier terminals (1,1') is the amplifier input impedence Z_i,

$Z_i = V_1 / I_1$

From the input circuit of Fig $V_1 = h_i I_1 +$

$h_r V_2 Z_i = (h_i I_1 + h_r V_2) / I_1$

$= h_i + h_r V_2 /$

I_1Substituting

$V_2 = -I_2 Z_L = A_1 I_1 Z_L$

$Z_i = h_i + h_r A_1 I_1 Z_L / I_1$

$= h_i + h_r A_1 Z_L$

Substituting for

A_i

$Z_i = h_i - h_f h_r Z_L / (1+ h_o Z_L)$

$= h_i - h_f h_r Z_L / Z_L(1/Z_L+ h_o)$

Taking the Load admittance as $Y_L = 1/$

$Z_L Z_i = h_i - h_f h_r / (Y_L + h_o)$

Voltage Gain or Voltage Gain Amplification Factor(A_v)

The ratio of output voltage V_2 to input voltage V_1 give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_i Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_S to zero, Z_L to infinity and by driving the output terminals from a generator V_2. If the current V_2 is I_2 then $Y_o = I_2/V_2$ with $V_S=0$ and $R_L= \infty$.

From the circuit of fig

$$I_2 = h_f I_1 +$$

$h_o V_2$ Dividing by V_2,

$$I_2 / V_2 = h_f I_1/V_2 + h_o$$

With $V_2 = 0$, by KVL in input circuit,

$$R_S I_1 + h_i I_1 + h_r V_2 =$$

$$0 (R_S + h_i) I_1 + h_r V_2 =$$

$$0$$

Hence, $I_2 / V_2 = -h_r / (R_S + h_i)$

$$= h_f (-h_r/(R_S +$$

$h_i) + h_o Y_o = h_o - h_f h_r/(R_S + h_i)$

The output admittance is a function of source resistance. If the source impedence is resistive then Y_o is real.

Voltage Amplification Factor(A_{vs}) taking into account the resistance (R_s) of the

source

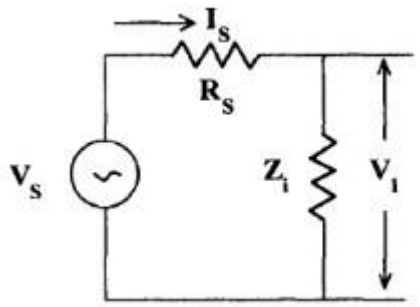


Fig. 5.6 Thevenin's Equivalent Input

CircuitThis overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_S = V_2V_1 / V_1V_S = A_v V_1 / V_S$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$V_1 = V_S Z_i / (Z_i + R_S)$

$V_1 / V_S = Z_i / (Z_i + R_S)$

Then, $A_{vs} = A_v Z_i / (Z_i +$

$R_S)$Substituting $A_v = A_iZ_L / Z_i$

$$A_{vs} = A_iZ_L / (Z_i + R_S)$$

$$A_{vs} = A_iZ_L R_S / (Z_i + R_S) R_S$$

$$A_{vs} = A_{is}Z_L / R_S$$

Current Amplification (A_{is}) taking into account the sourse Resistance(R_S)

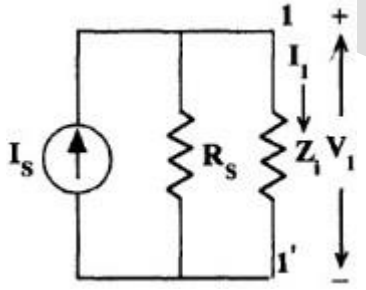


Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7

Overall Current Gain, $A_{is} = -I_2 / I_S = - I_2 I_1 / I_1 I_S = A_i I_1 / I_S$

From Fig. 1.7 $I_1 = I_S R_S / (R_S + Z_i) I_1 / I_S = R_S / (R_S + Z_i)$

and hence, $A_{is} = A_i R_S / (R_S + Z_i)$

Operating Power Gain (A_P)

The operating power gain A_P of the transistor is defined as

$$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$$

$$A_P = A_i^2 (Z_L / Z_i)$$

Small Signal analysis of a transistor amplifier

$A_i = - h_f / (1+ Z_L h_o)$	$A_v = A_i Z_L / Z_i$
$Z_i = h_i + h_r A_1 Z_L = h_i - h_f h_r / (Y_L + h_o)$	$A_{vs} = A_v Z_i / (Z_i + R_S) = A_i Z_L / (Z_i + R_S)$ $= A_{is} Z_L / R_S$
$Y_o = h_o - h_f h_r / (R_S + h_i) = 1 / Z_o$	$A_{is} = A_i R_S / (R_S + Z_i) = A_{vs} = A_{is} R_S / Z_L$

UNIT-IV

TRANSISTOR BIASING AND STABILIZATION

NEED FOR TRANSISTOR BIASING

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region. To establish an operating point (proper values of collector current I_c and collector to emitter voltage V_{CE}) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1) Emitter base junction must be forward biased (V_{BE}=0.7Vfor Si, 0.2V for Ge) and collector basejunction must be reverse biased for all levels of i/p signal.
2) V_{ce} voltage should not fall below $V_{CE\ (sat)}$ (0.3V for Si, 0.1V for Ge) for any part of the i/p signal.For V_{CE} less than $V_{CE\ (sat)}$ the collector base junction is not probably reverse biased.
3) The value of the signal I_c when no signal is applied should be at least equal to the max. collector current t due to signal alone.
4) Max. rating of the transistor $I_{c(max)}$, $V_{CE\ (max)}$ and $P_{D(max)}$ should not be exceeded at any value ofi/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, I_c=0, V_{CE} =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to $P_{D(max)}$ curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents

Hence operating point for a transistor amplifier is selected to be in the middle of active region.

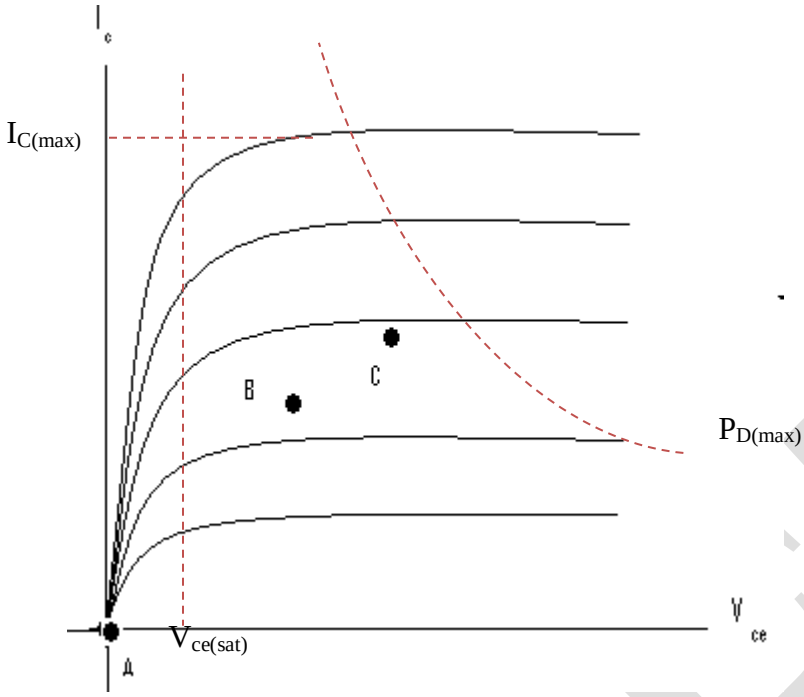


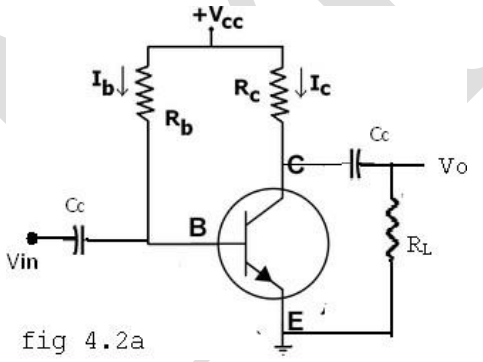
Fig 4.1CE Output Characteristics

DC LOAD LINE

Referring to the biasing circuit of fig 4.2a, the values of V_{CC} and R_C are fixed and Ic and V_{CE} are dependent on R_B.

Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$Vcc = IcRc + Vce$$



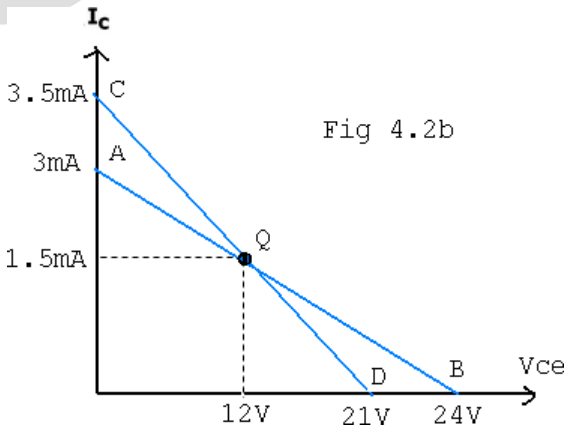


Fig 4.2b

Fig 4.2a CE Amplifier circuit (b) Load line

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting V_{CE} =0 in the above equation. Then $Ic = \frac{Vcc}{Rc}$. Therefore The coordinates of A are V_{CE} =0 and $Ic = \frac{Vcc}{Rc}$.

The coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are V_{CE} =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10°C raise in temperature
2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per °C
3) Transistor current gain, h_{FE} or β which increases with temperature.

If base current I_B is kept constant since I_B is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given I_B. Hence , in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

AC LOAD LINE

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance R_{ac}, is a combination of R_C parallel to R_L i.e.$R_{ac} = R_L \| R_C$. So the slope of the ac load line CQD will be $\left(\frac{-1}{R_{ac}}\right)$. To draw the ac load line, two end points, I.e. $V_{CE(max)}$ and $I_{C(max)}$ when the signal is applied are required.

$V_{CE(\max)} = V_{CEQ} + I_{CQ}R_{ac}$, which locates point D on the Vce axis.

$I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the I_C axis.

By joining points c and D, ac load line CD is constructed. As $R_C > R_{ac}$, The dc load line is less steep thanac load line.

STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, I_C also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which I_C is stabilized with varying I_C is measured by a stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}}, \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C , We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

METHODS OF TRANSISTOR BIASING

1) Fixed bias (base bias)

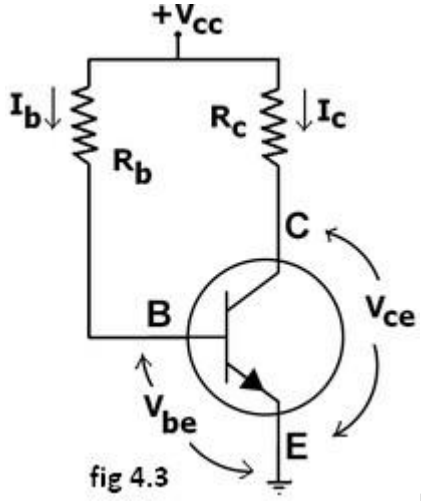


Fig 4.3 Fixed Biasing Circuit

This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example,battery) is used for both collector and base of a transistor, although separate batteries can also be used.

In the given circuit,

$V_{cc} = I_B R_B + V_{be}$

Therefore, $I_B = (V_{cc} - V_{be})/R_B$

Since the equation is independent of current I_CR, $dI_B/dI_C R = 0$ and the stability factor is given by the equation….. reduces to

$$S=1+\beta$$

Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used fo biasing.

For a given transistor, V_{be} does not vary significantly during use. As V_{cc} is of fixed value, on selection of Rthe base current I_B is fixed. Therefore this type is called *fixed bias* type of circuit.

Also for given circuit, $V_{cc} = I_C R_C + V_{ce}$

Therefore, $V_{ce} = V_{cc} - I_C R_C$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- Changes in V_{be} will change I_B and thus cause R_E to change. This in turn will alter the gainof the stage.
- When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

2) EMITTER-FEEDBACK BIAS:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizesthe Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is

$V_{Rb} = V_{CC} - I_e R_e - V_{be}$.

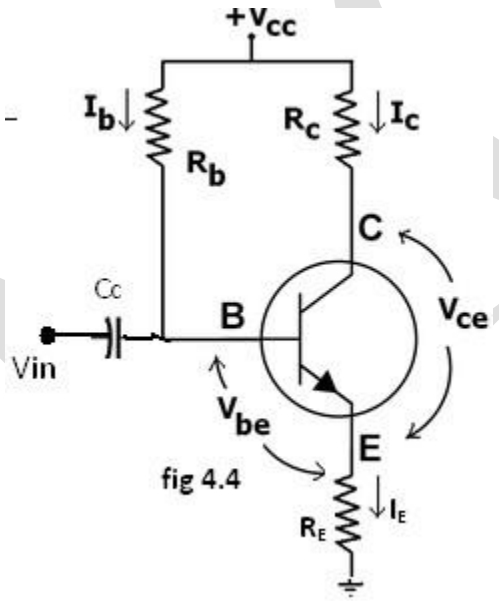


fig 4.4

Fig 4.4 Self Biasing Circuit

From Ohm's law, the base current is

$I_b = V_{Rb} / R_b$.

The way feedback controls the bias point is as follows. If V_{be} is held constant and temperature increases, emitter current increases. However, a larger I_e increases the emitter voltage $V_e = I_e R_e$, which in turn reduces the voltage V_{Rb} across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because $I_c = ß\ I_B$. Collector current and emitter current are related by $I_c = \alpha\ I_e$ with $\alpha \approx 1$, so increase in emitter current with temperature is opposed, and operating point is kept stable.

Similarly, if the transistor is replaced by another, there may be a change in I_C (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable.

For the given circuit,

$I_B = (V_{CC} - V_{be})/(R_B + (\beta+1)R_E)$.

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if $(\beta + 1)R_E >> R_B$.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E very large, or making R_B very low.
- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautionsnecessary while handling.
- If R_B is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical.
- In addition to the above, R_E causes ac feedback which reduces the voltage gain of the amplifier.

3)COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

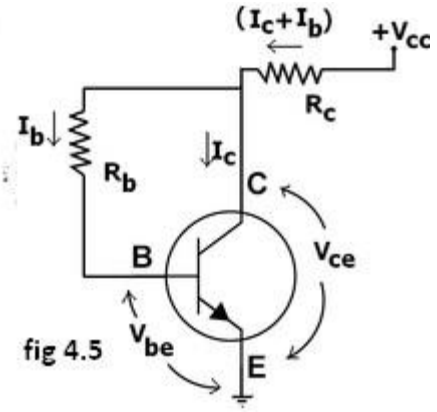


Fig 4.5 Collector to Base Biasing Circuit

This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

From Kirchhoff's voltage law, the voltage V_{R_b}across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If V_{be} is held constant and temperature increases, then the collector current I_c increases. However, a larger I_c causes the voltage drop across resistor R_c to increase, which in turn reduces the

voltage V_{R_b}across the base resistor R_b. A lower base-resistor voltage drop reduces the base current I_b, which results in less collector current I_c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

- Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

- In this circuit, to keep I_c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

- As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping R_c fairly large or making R_b very low.

- If R_c is large, a high V_{cc} is necessary, which increases cost as well as precautions necessary while handling.
- If R_b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.

- The resistor R_b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from thebase, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

4)COLLECTOR –EMITTER FEEDBACK BIAS:

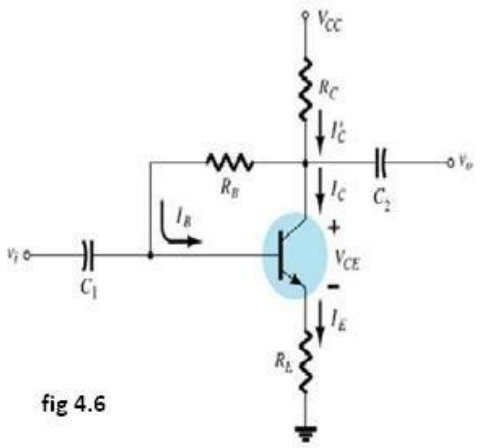


Fig 4.6 Collector-Emitter Biasing Circuit

The above fig4.6 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

5)VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS

The voltage divider as shown in the fig 4.7 is formed using external resistors R_1 and R_2. The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R_2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

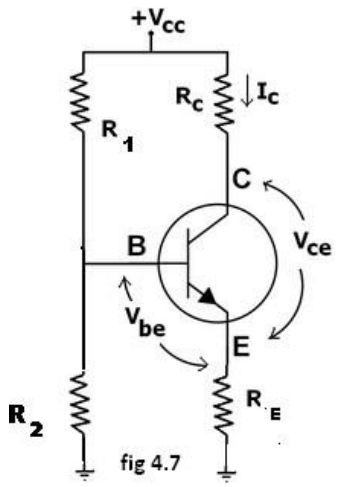


Fig 4.7 Voltage Divider Biasing Circuit

In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{ provided } I_B << I_2 = V_B/R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1+R_2}$$

$$V_2 = \frac{V_{CC}}{R_1+R_2}\cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases toits former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq} + R_E)}{R_{eq} + R_E(1+\beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1+\beta)\left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

Demerits:

- In this circuit, to keep I_C independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

where $R_1 \parallel R_2$ denotes the equivalent resistance of R_1 and R_2 connected in parallel.

- As β-value is fixed for a given transistor, this relation can be satisfied either by keeping R_E fairly large, or making $R_1 \parallel R_2$ very low.

- If R_E is of large value, high V_{CC} is necessary. This increases cost as well as precautions necessary while handling.
- If $R_1 \parallel R_2$ is low, either R_1 is low, or R_2 is low, or both are low. A low R_1 raises V_B closer to V_C, reducing the available swing in collector voltage, and limiting how large R_C can be made without driving the transistor out of active mode. A low R_2 lowers V_{be}, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

- AC as well as DC feedback is caused by R_E, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

BIAS COMPENSATION USING DIODE AND TRANSISTOR

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for variations in current.

DIODE COMPENSATION:

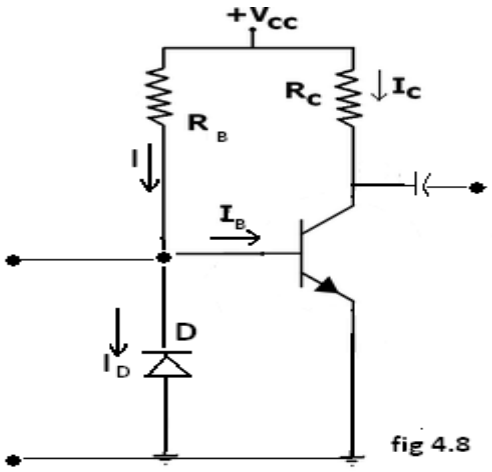


fig 4.8

The following fig4.8 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current I_{CO}. The diode is of the same material as the transistor and it is reverse biased by e the emitter-base junction voltage V_{BE}, allowing the diode reverse saturation current I_O to flow through diode D. The base current $I_B=I-I_O$.

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, I_{CO} of the transistor increases. Hence, to compensate for this, the base current I_B should be decreased.

The increase in temperature will also cause the leakage current I_O through D to increase and thereby decrease the base current I_B. This is the required action to keep Ic constant.

This type of bias compensation does not need a change in Ic to effect the change in I_C, as both I_O and I_{CO} can track almost equally according to the change in temperature.

THERMISTOR COMPENSATION:

The following fig4.9 a thermistor R_T, having a negative temperature coefficient is connected in parallel with R_2. The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage V_{BE}, reducing I_B and I_C.

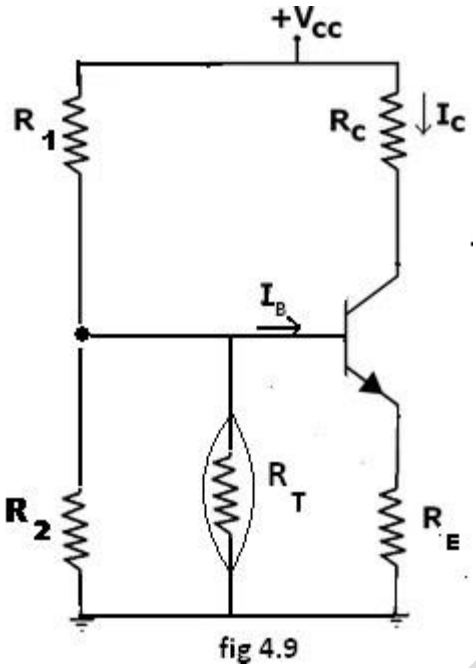


Fig 4.9 Thermistor Compensation

SENSISTOR COMPENSATION:

In the following fig4.10 shown a sensistor Rs having a positive temperature coefficient is connected across R_1 or R_E. Rs increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R1 and Rs also increases and hence V_{BE} decreases, reducing I_B and Ic. This reduced Ic compensates for increased Ic caused by the increase in V_{BE}, I_{CO} and β due to temperature.

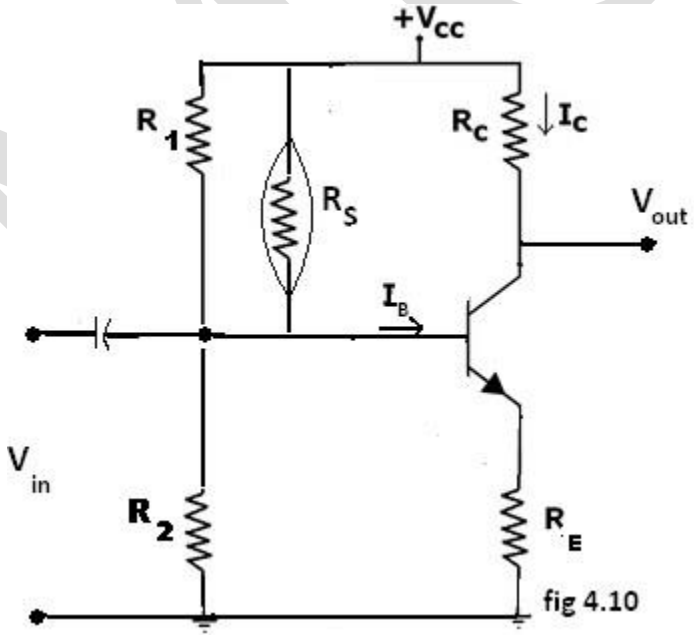


Fig 4.10 Sensistor Compensation

THERMAL RUNAWAY AND THERMAL STABILITY

THERMAL RUNAWAY:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1+\beta)I_{CO}$. The three variables in the equation, β, I_B, and I_{CO} increases with rise in temperature. In particular, the reverse saturation current or leakage current I_{CO} changes greatly with temperature. Specifically it doubles for every 10°C rise in temperature. The collector current $I_C$causes the collector base junction temperature to rise which in turn, increase I_{CO} , as a result I_C will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to *"thermal runaway"*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current I_B is made to decrease automatically with rise in temperature, then the decrease in βI_B will compensate for increase in the $(1+\beta)I_{CO}$, keeping I_C almost constant.

THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is T_A°C and the temperature of the collector-base junction of the transistor is T °C.

Due to heating within the transistor T_J is higher than T_A. As the temperature difference T_J- T_A is greater, the power dissipated in the transistor, P_D will be greater, i.e, T_J- T_A P_D

The equation can be written as T_J- T_A Θ P_D. , where Θ is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation Θ T_J- T_A /P_D. Hence is measured in °C/W which may be as small as 0.2 °C/W for a high power transistor that has an efficient heat sink or up to 1000°C/W for small signal, low power transistor which have no cooling provision.

As Θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as $\Theta_{J\text{-}A}$. However, for power transistors, thermal resistance is given form junction to case, $\Theta_{J\text{-}C}$.

The amount resistance from junction to ambience is considered to consist of 2 parts.

$$\Theta_{J-A} = \Theta_{J-C} - \Theta_{C-A}.$$

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence the power dissipated.

$$P_D = (T_J - T_A)/\Theta_{J-A}$$

$$=(T_J - T_A)/(\Theta_{J-C} + \Theta_{C-A})$$

Θ_{J-C} is determined by the type of manufacture of the transistor and how it is located I the case, but $\Theta_{C-A}$is determined by the surface area of the case or flange and its contact with air. If the effective surface area of the transistor case could be increased, the resistance to heat flows, or could be increased Θ_{C-A}, could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance Θ_{HS-A}.

This thermal resistance is not added to Θ_{C-A} in series, but is instead in parallel with it and if

Θ_{HS-A} is much less than Θ_{C-A}, then Θ_{C-A} will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

$\Theta_{J-A} = \Theta_{J-C} + \Theta_{C-A} \| \Theta_{HS-A}$.

CONDITION FOR THERMAL STABILITY

For preventing thermal runaway, the required condition I the rate at which the heat is releasedat the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence the condition to be satisfied to avoid thermal runaway is given by

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\Theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$$P_C = I_C V_{CB} \approx I_C V_{CE}$$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$$P_C = I_C V_{CC} - I_C^2(R_E + R_C) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

The condition to prevent thermal runaway can be written as

$$\frac{\partial P_C}{\partial I_C}\frac{\partial I_C}{\partial T_j} < \frac{1}{\Theta} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

As Θ and $\frac{\partial I_C}{\partial T_j}$ are positive, $\frac{\partial P_C}{\partial I_C}$ should be negative in order to satisfy the above condition.

Differentiating equation (1) w.r.t I_C we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C(R_E + R_C) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Hence to avoid thermal runaway it is necessary that

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

SinceVCE=VCC-IC(RE+RC) then eq(4) implies that VCE<VCC/2. IF the inequality of eq(4) is not satisfied and VCE<VCC/2, then from eq(3), $\frac{\partial P_C}{\partial I_C}$ is positive., and the corresponding eq(2) should be satisfied. Otherwise thermal runaway will occur.

UNIT 5

FIELD EFFECT TRANSISTOR

INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

1. Junction Field Effect Transistors

2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is ofP-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.

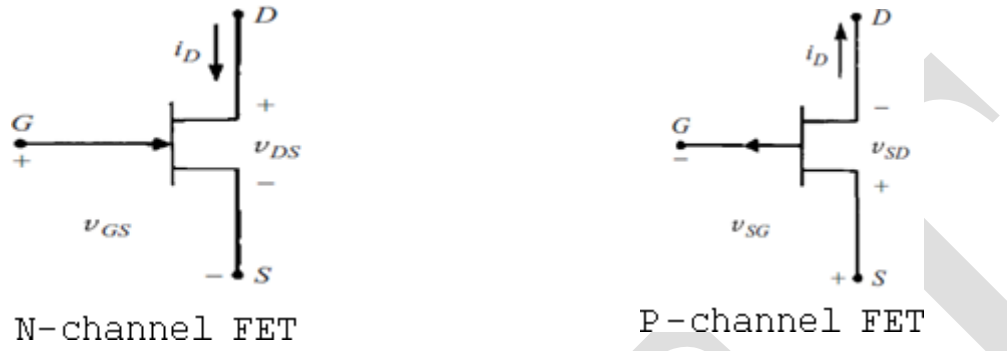


Fig 5.1 schematic symbols for the P-channel and N-channel JFET

CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET

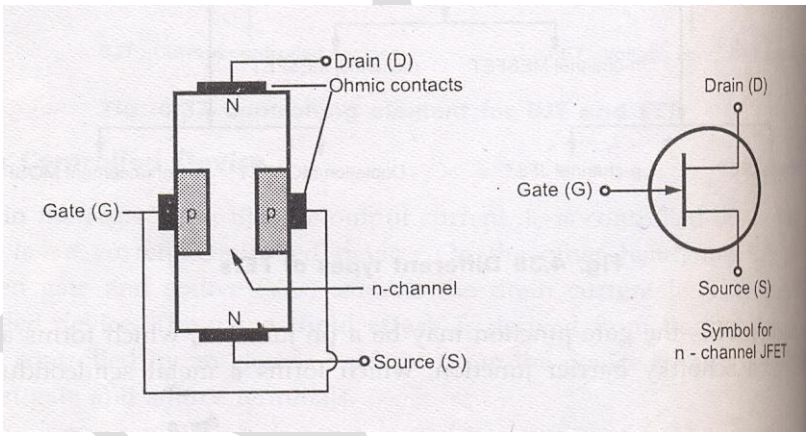


Fig 5.2 Construction of N-Channel JFET

A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source. And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

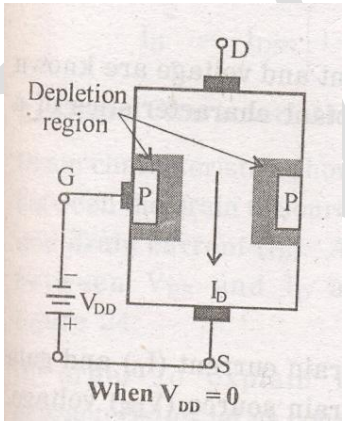
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

There are two ways to control the channel width

1. By varying the value of Vgs
2. And by Varying the value of Vds holding Vgs constant

1 By varying the value of Vgs :-

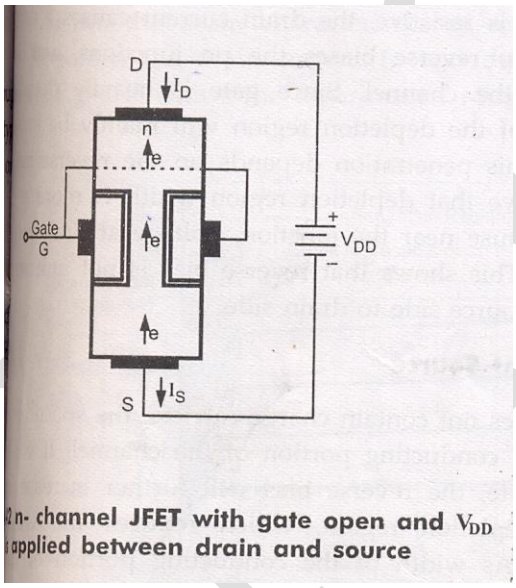
We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



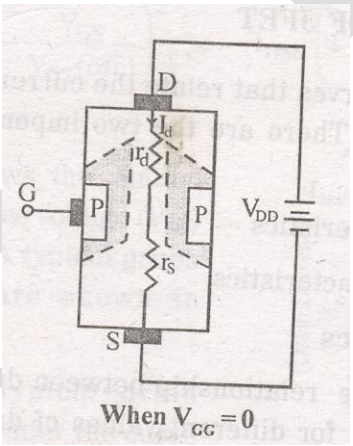
1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
6) By varying the value of Vgs we can vary the width of the channel.

2 Varying the value of Vds holding Vgs constant :-

1) When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current Id .
2) With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds .
3) The channel resistances are represented as rd and rs as shown in the fig.



2 n- channel JFET with gate open and V_{DD} applied between drain and source



4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical .

5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constant value.
7) So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:-

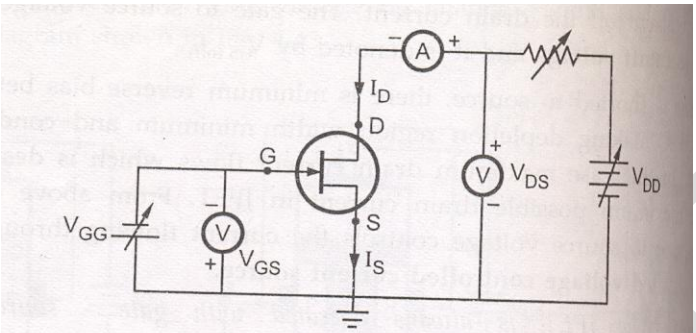
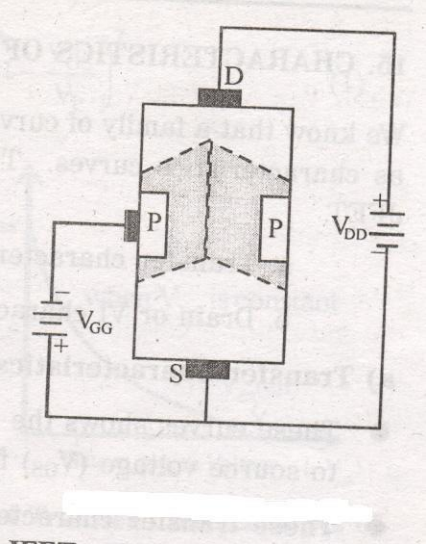


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current Id, its conventional direction is from drain to source.
2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.



3) When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
4) When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

CHARACTERISTICS OF N-CHANNEL JFET

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VI Characteristics
2) Transfer characteristics

1. Drain Characteristics:-

2. Drain characteristics shows the relation between the drain to source voltage Vds and drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1) When Vds is applied and it is increasing the drain current ID also increases linearly up to knee point.
2) This shows that FET behaves like an ordinary resistor.This region is called as ohmic region.
3) ID increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

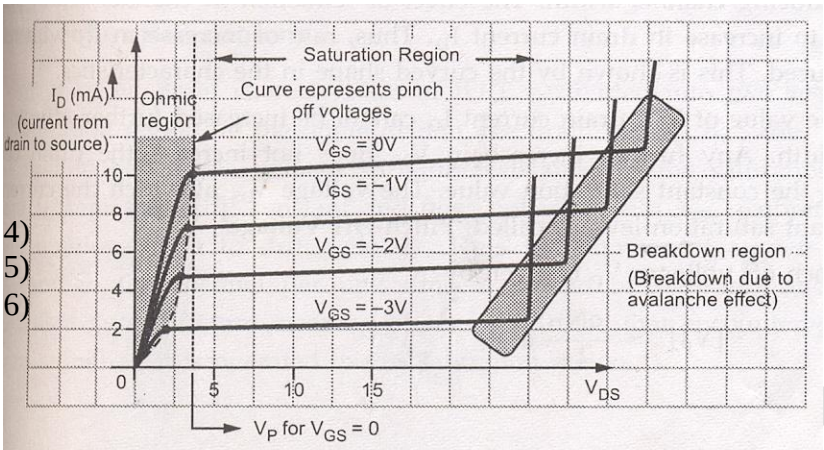


Fig. 4.44 Drain V-I characteristics of n-channel JFET

4)
5)
6)

4) It is because of the fact that there is an increase in VDS .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.

5) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(Vp).

PINCH OFF Region:-

1) This is the region shown by the curve as saturation region.
2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
3) In this drain current remains constant at its maximum value IDSS.

4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{dss} [1-V_{gs/Vp}]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
2) It is because of the gate to source junction due to avalanche effect.

3) The avalanche break down occurs at progressively lower value of VDS because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction

This causes

1. The maximum saturation drain current is smaller
2. The ohmic region portion decreased.

4) It is important to note that the maximum voltage VDS which can be applied to FET is the lowest voltage which causes available break down.

3. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current ID and gate to source voltage VGS for different values of VDS.

1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
2) Plot the graph between gate to source voltage along the horizontal axis and current ID on the vertical axis. We shall obtain a curve like this.

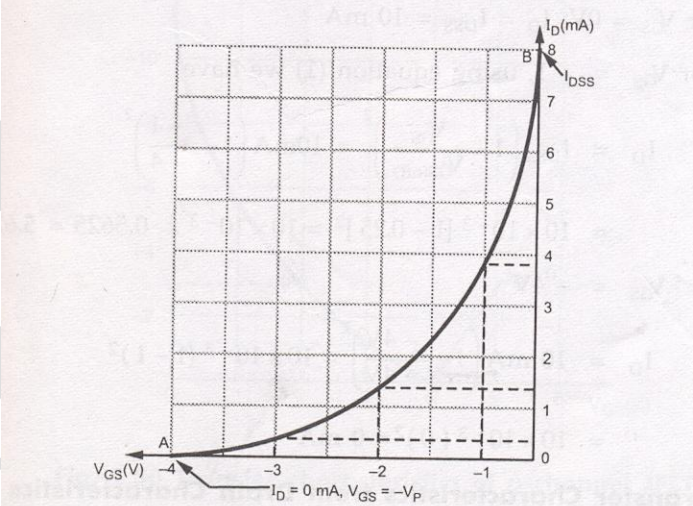


Fig. 4.48 Transfer characteristics of n-channel JFET

3) As we know that if V_{gs} is more negative curves drain current to reduce . where V_{gs} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{gs} at the cutoff point is designed as V_{gsoff}

4) The upper end of the curve as shown by the drain current value is equal to I_{dss} that is when V_{gs} = 0 the drain current is maximum.

5) While the lower end is indicated by a voltage equal to V_{gsoff}
6) If Vg_s continuously increasing , the channel width is reduced , then I_d =0
7) It may be noted that curve is part of the parabola; it may be expressed as

$I_d=I_{dss}[1-V_{gs/}V_{gsoff}]^2$

DIFFERENCE BETWEEN V_p AND V_{gsoff} –

Vp is the value of V_{gs} that causes the JFET to become constant current component, It is measured at V_{gs} =0V and has a constant drain current of I_d =I_{dss} .Where V_{gsoff} is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET 's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region.It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage $V_{gs.}$

Mathematically it is expressed as $r_d=\Delta V_{ds/}\Delta I_d$ where V_{gs} is held onstant.

TRANCE CONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m=\Delta I_d/\Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu=\Delta V_{ds}/\Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

$\mu=\Delta V_{ds}/\Delta V_{gs}=g_m\, r_d$

THE FET SMALL SIGNAL MODEL

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current iD as a function f of the gate voltage and drain voltage V_{ds}.

$I_d=f(V_{gs},V_{ds})$---------- (1)

The transconductance g_m and drain resistance r_d:-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylors series considering only the first two terms in the expansion

$$\Delta i_d=\frac{\partial id}{\partial Vgs}|v_{ds}=\text{constant}\ .\Delta v_{gs}+\frac{\partial id}{\partial Vds}|vgs=\text{constant}\Delta v_{ds}$$

we can write $\Delta i_d=i_d$

$\Delta v_{gs}=v_{gs}$

$\Delta v_{ds}=v_{ds}$

$$I_d=g_m\, v_{gs}+\frac{1}{rd}\ Vds\rightarrow(1)$$

Where $g_m=\frac{\partial id}{\partial Vgs}|Vds\ \cong\ \frac{\Delta id}{\Delta Vgs}|Vds$

$$g_m=\frac{id}{Vgs}|Vds$$

Is the mutual conductance or transconductance .It is also called as gfs or yfs common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d=\frac{\partial Vds}{\partial id}|_{Vgs} \cong \frac{\Delta vds}{\Delta ids}|_{Vgs}=\frac{Vds}{id}|_{Vgs}$$

$$r_d=\frac{Vds}{id}|_{Vgs}$$

The reciprocal of the rd is the drain conductance gd .It is also designated by Yos and Gos and called the common source output conductance . So the small signal equivalent circuit for FET can be drawn in two different ways.

1.small signal current –source model

2.small signal voltage-source model.

A small signal current –source model for FET in common source configuration can be drawn satisfying Eq→(1) as shown in the figure(a)

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to –source voltage. The proportionality factor is the transconductance 'g_m'. The output resistance is 'r_d'. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

The small signal voltage-source model is shown in the figure(b).

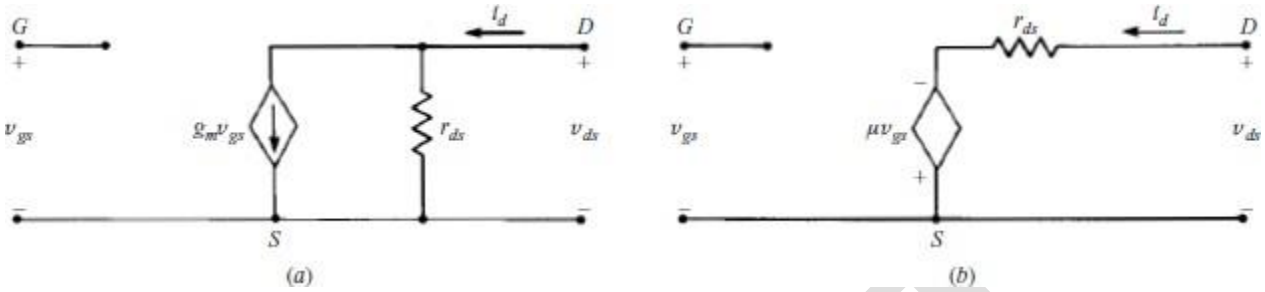
This can be derived by finding the Thevenin's equivalent for the output part of fig(a) .

These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

1.common source (CS) 2.common drain (CD) or source follower

3. common gate(CG).

(a)Small Signal Current source model for FET (b)Small Signal voltage source model for FET

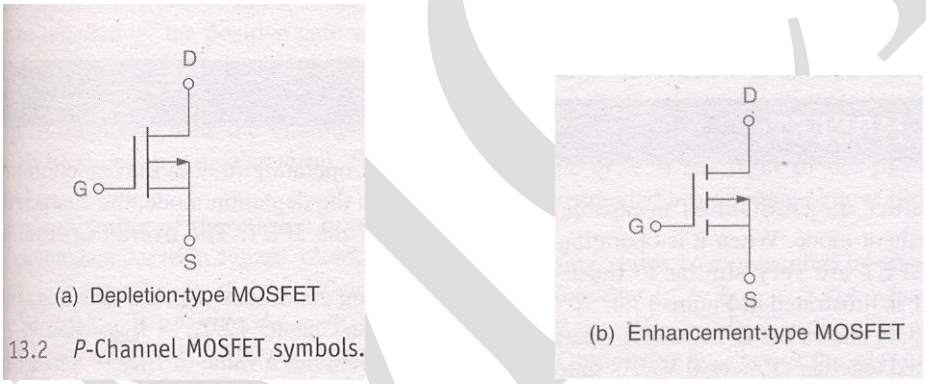


Here the input circuit is kept open because of having high input impedance and the output circuit satisfies the equation for ID

MOSFET

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.



(a) Depletion type MOSFET (b) Enhancement type MOSFET

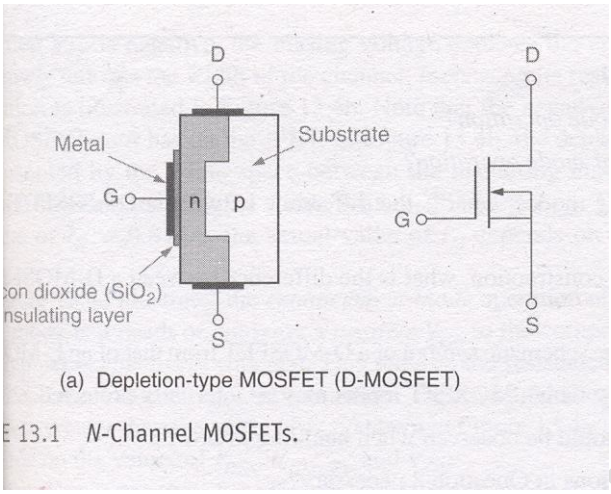
Both of them are P- channel

Here are two basic types of MOSFETS

(1) Depletion type (2) Enhancement type MOSFET.

D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

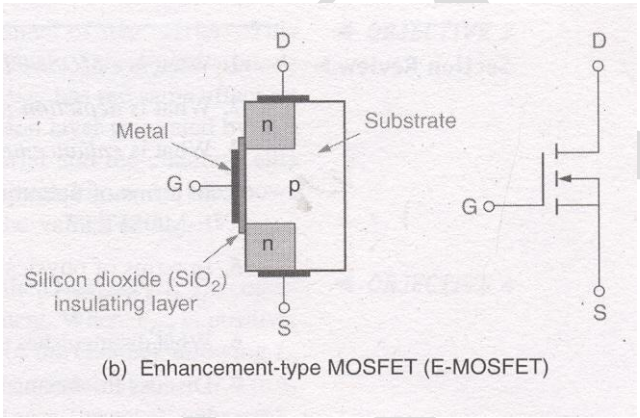
The construction difference between the two is shown in the fig given below.



(a) Depletion-type MOSFET (D-MOSFET)

E 13.1 *N*-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



(b) Enhancement-type MOSFET (E-MOSFET)

The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SIO_2 a glass like insulating material. The gate material is made up of

metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimesreferred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing inrepresents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:-

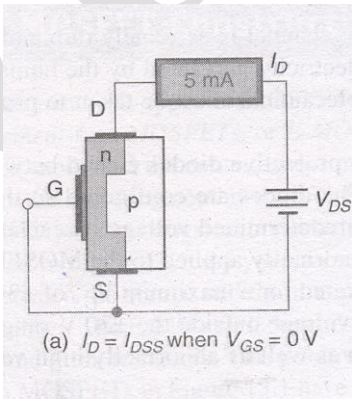
The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain.

A thin layer of insulation silicon dioxide (SIO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and sourceand the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio2

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

DEPLETION MOSFET

The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current IDSS flows foe zero gate to source voltage, Vgs=0.



Depletion mode operation:-

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=0V)

2) At this stage ID= IDSS where VGS=0V, with this voltage VDS, an appreciable drain current IDSSflows.

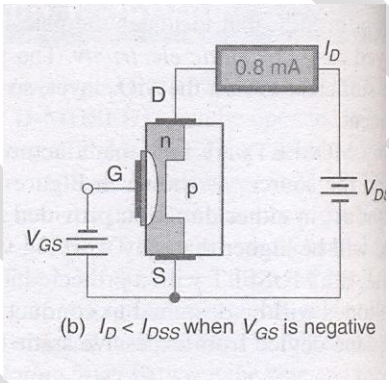
3) If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SIO2 of the gate capacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.

7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.



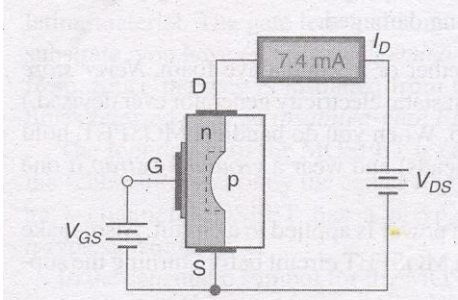
(b) $I_D < I_{DSS}$ when V_{GS} is negative

8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result ,Id<Idss.The actual value of ID depends on the value of Idss,Vgs(off) and Vgs.

Enhancement mode operation of the D-MOSFET:-

1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS
3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.

4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
6) The extended n type channel now allows more current, Id> Idss



(c) $I_D > I_{DSS}$ when V_{GS} is positive

FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

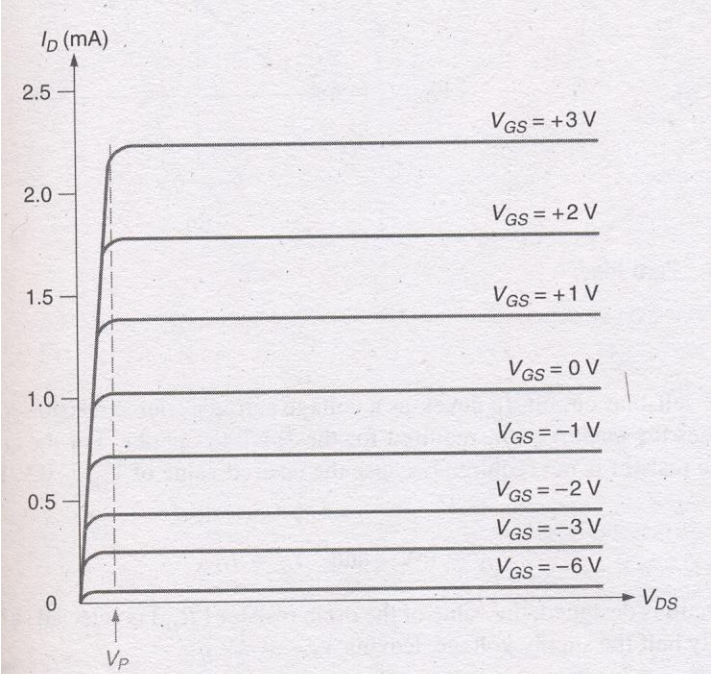
The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negative voltages
.
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive ,theMOSFET operates in the enhancement mode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values ofVgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.

5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

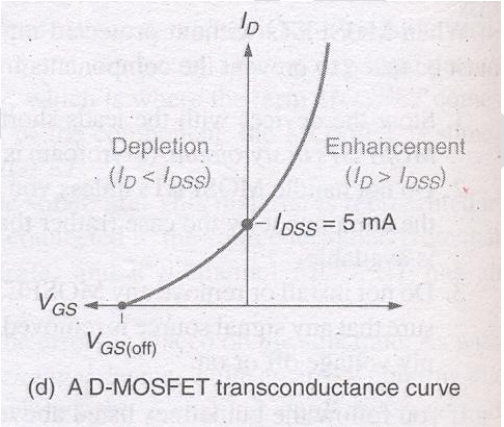
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6 MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.



(d) A D-MOSFET transconductance curve

1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.

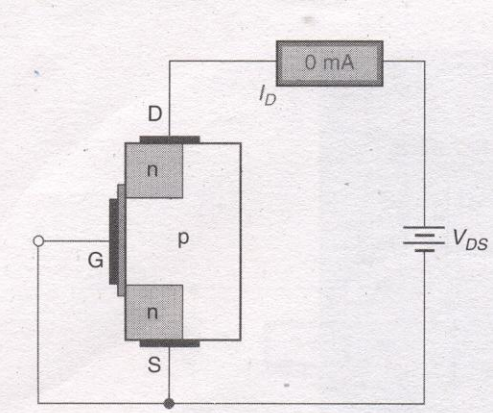
2) This curve extends for the positive values of Vgs

3) Note that Id=Idss for Vgs=0V when Vgs is negative,Id< Idss when Vgs= Vgs(off) ,Id is reduced to approximately omA.Where Vgs is positive Id>Idss.So obviously Idss is not the maximum possiblevalue of Id for a MOSFET.

4) The curves are similar to JFET so thet the D MOSFET have the same transconductance equation.

E-MOSFETS

The E MOSFET is capable of operating only in the enhancement mode.The gate potential must be positive w.r.t to source.



(a) $I_D = 0$ mA when $V_{GS} = 0$ V

1) when the value of Vgs=0V, there is no channel connecting the source and drain materials.

2) As aresult , there can be no significant amount of drain current.

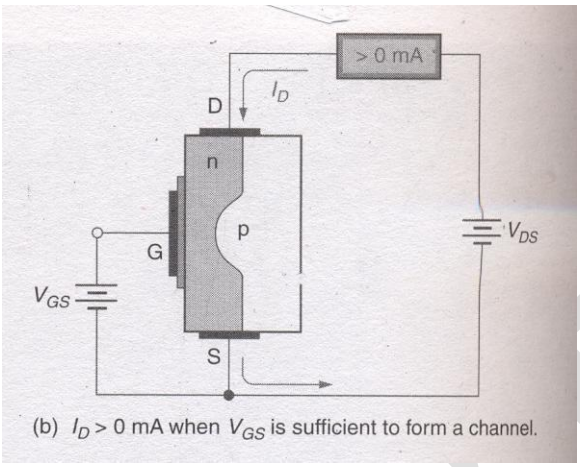
3) When Vgs=0, the Vdd supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at Vgs=0,

4) If Vgs is positive, it induces a negative charge in the p type substrate just adjacent to the SIO2 layer.

5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for drain current.

6) This +ve gate voltage forma a channel between the source and drain.

7) This produces a thin layer of N type channel in the P type substarate.This layer of free electrons is called N type inversion layer.



(b) $I_D > 0$ mA when V_{GS} is sufficient to form a channel.

8) The minimum Vgs which produces this inversion layer is called threshold voltage and is designated by Vgs(th).This is the point at which the device turns on is called the threshold voltage Vgs(th)
9) When the voltage Vgs is <Vgs (th) no current flows from drain to source.

10) How ever when the voltage Vgs > Vgs (th) the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E MOSFET:-

1. DRAIN CHARACTERISTICS

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the

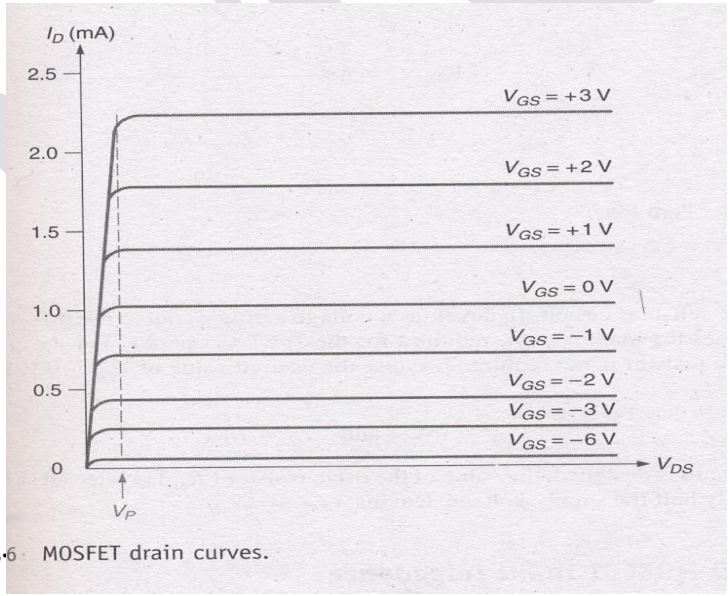


fig.6 MOSFET drain curves.

2. TRANSFER CHARACTERISTICS:-

1) The current Idss at Vgs≤ 0 is very small beinf of the order of a few nano amps.
2) As Vgs is made +ve , the current Id increases slowly at forst, and then much more rapidly with an increase in Vgs.
3) The standard transconductance formula will not work for the E MOSFET.
4) To determine the value of ID at a given value of VGs we must use the following relation

$$Id = K[V_{gs} - V_{gs(Th)}]^2$$

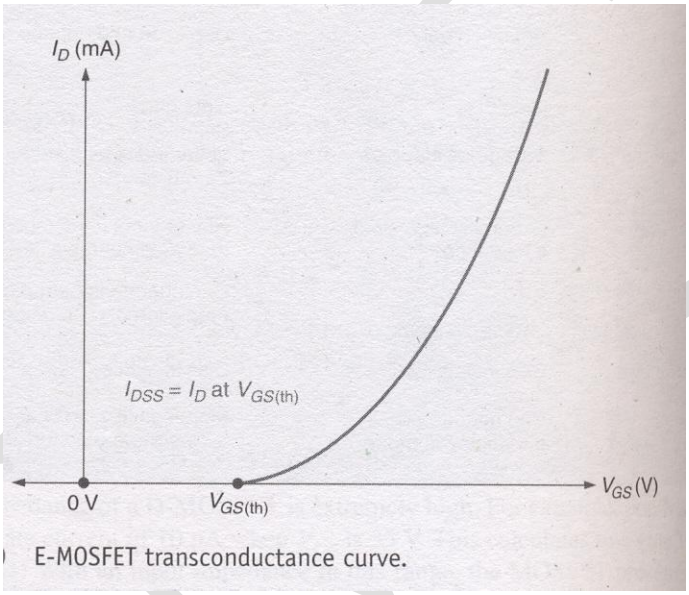
Where K is constant for the MOSFET . found as

$$K = \frac{Id(on)}{[vgs(on) - Vgs(Th)]2}$$

From the data specification sheets, the 2N7000 has the following ratings.

Id(on)= 75mA(minimum).

And Vgs(th)=0.8(minimum)



E-MOSFET transconductance curve.

APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage VGS and drain current ID which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference betweenJFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1) Self bias
2) Voltage divider bias.

SELF BIAS

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate. A self bias circuit is shown in the fig. Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative VGS for an N channel JFET and a positive VGS for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig. The gate resistor RG doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .RG is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor RS makes gate source junctionreverse biased.

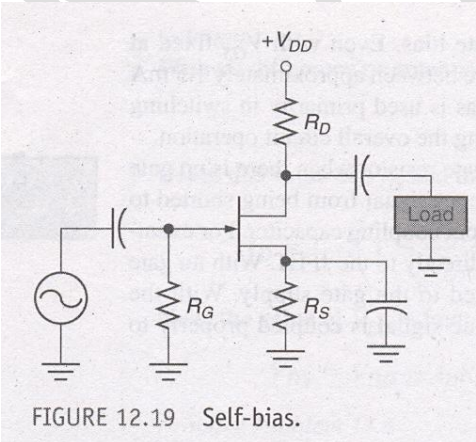


FIGURE 12.19 Self-bias.

For the dc analysis coupling capacitors are open circuits.

For the N channel FET in Fig (a)

IS produces a voltage drop across RS and makes the source positive w.r.t ground. In any JFET circuit all the source current passes through the device to the drain circuit .This is due to the fact that there is no significant gate current.

We can define source current as IS = ID

(VG =0 because there is no gate current flowing in RG So VG across RG is

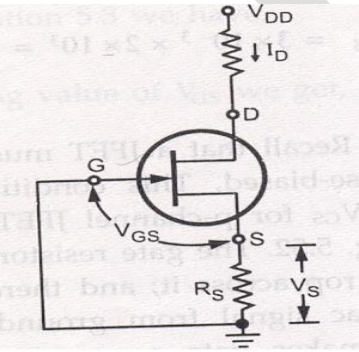
zero)VG =0 then VS= ISRS =ID RS

VGS = VG-VS =0-ID RS=- ID RS

DC analysis of self Bias:-

In the following DC analysis, the N channel J FET shown in the fig. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor RG by a short circuit equivalent.:. IG = 0.The relation between ID and VGS is given by



$$Id=Idss[1-\frac{Vgs}{Vp}]^2$$

VGS for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id=Idss[1-\frac{(-IdRs)}{Vp}]^2$$

$$Id=Idss[1+\frac{(IdRs)}{Vp}]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current. Therefore we can define source current as Is=Id and Vg=0 then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig.

The maximum drain current is 5mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

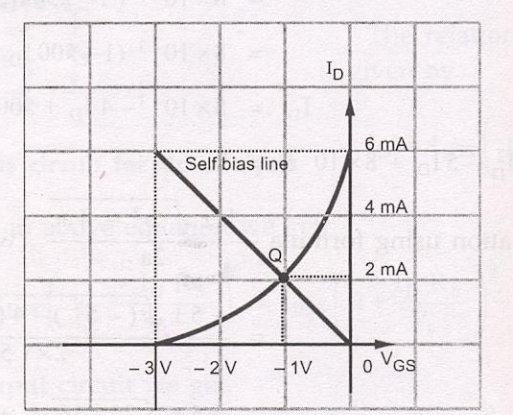


Fig. 5.55 Transfer characteristics

Now using the equation VGS = -IDRS and assuming RS of any suitable value we can draw the self biasline.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to ID = 0 and Id =

IDSSfor ID = 0

VGS = -ID RS

VGS = 0X (500.Ω) = 0V

So the first point is (0 ,0)

(I_d, VGS)

For ID= IDSS=5mA

VGS = (-5mA) (500 Ω) = -3V

So the 2nd Point will be (5mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line.The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the ID is slightly > than 2mA and VGS is slightly > -1V. The Q point for the self biasJFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve ,ID is small, when Rs is small Q point is far up on the curve , ID is large.

VOLTAGE DIVIDER BIAS:-

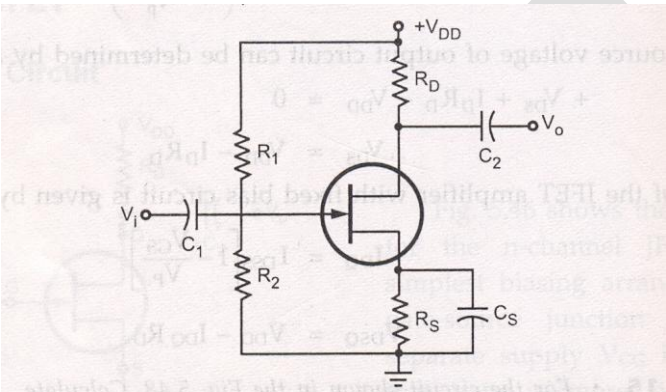


Fig. 5.49 Voltage divider bias for n-channel JFET

The fig. shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

VS = IDRS

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$Vg=\left(\frac{R2}{(R1+R2)}\right)Vdd$$

For dc analysis

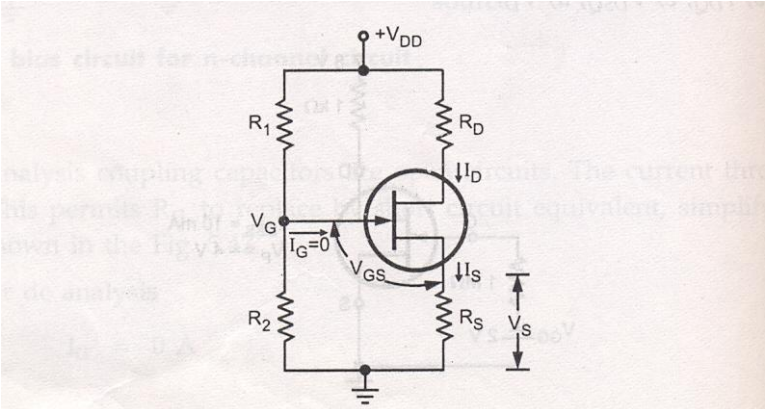


Fig. 5.50 Simplified voltage divider circuit for dc analysis

Applying KVL to the input

circuitVG-VGS-VS =0

:: VGS = VG-Vs=VG-

ISRS VGS = VG-IDRS ::

IS = ID

Applying KVL to the input circuit we

getVDS+IDRD+VS-VDD =0

::VDS = VDD-IDRD-

IDRS VDS = VDD-ID (

RD +RS)

The Q point of a JFET amplifier , using the voltage divider bias

isIDQ = IDSS [1-VGS/VP]2

VDSQ = VDD-ID (RD+RS)

COMPARISON OF MOSFET WITH JFET

a. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel.

b. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.

c. The gate leakage current in a MOSFET is of the order of 10^{-12}A. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate leakage current of a JFETis of the order of 10^{-9}A., and its input resistance is of the order of 10^{8}Ω.

d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to 1MΩ) is much higher than that of a MOSFET (1 to 50kΩ).

e. JFETs are operated only in the depletion mode. The depletion type MOSFET may beoperated in both depletion and enhancement mode.

f. Comparing to JFET, MOSFETs are easier to fabricate.

g. Special digital CMOS circuits are available which involve near zero power dissipation andvery low voltage and current requirements. This makes them suitable for portable systems.

STUDENT ROL LIST IV SEM ECE-B

Sl.No	ROLL NUMBER	STUDENT NAME
1.	160721735062	MOLUGURU PALLAVI
2.	160721735063	POTHULA SAI KRISHNA
3.	160721735064	NUNE VINOD
4.	160721735065	TIRUMALA KARTHIKEYA
5.	160721735067	P VENKATA SAI ANIL PATNAIK
6.	160721735068	RAMAVATH BHANU
7.	160721735069	R VARUN KUMAR REDDY
8.	160721735070	RATHOD PARASHURAM
9.	160721735071	SAAD KHAN
10.	160721735072	GOPARAJU SAI MADHAV
11.	160721735074	SHAIK SOHAIL
12.	160721735075	SHAIK ABUBAKAR SIDDIK
13.	160721735076	SHERLA SAI VARDHAN
14.	160721735077	SOBIA NAAZ
15.	160721735078	MD FURQUAN NAWAZ
16.	160721735079	SOMAROWTHU SAI BHASKAR
17.	160721735080	SR PREM KUMAR
18.	160721735081	PENUEL ZECHARAIAH JAMES
19.	160721735082	SYED IMAMUDDIN
20.	160721735083	TELLABOINA RAJESH
21.	160721735084	K ANIL KUMAR
22.	160721735085	TERALA VIGNESH
23.	160721735086	THADIGOPPULA SANNY
24.	160721735087	MUNIGALA SATHWIK
25.	160721735088	THATOJU ABHISHEK
26.	160721735089	UNNI KISHORE
27.	160721735090	CHENUMALLA KOUSHIK
28.	160721735091	VERTHE SURESH NAIK
29.	160721735092	VODNALA NITHIN
30.	160721735093	GARLAPALLI SAI RAJITHA
31.	160721735094	VARAGANTI PAVAN KUMAR
32.	160721735096	TIGULLA RAVISHWAS GOUD
33.	160721735301	BHAVANA GUNDLAPALLY
34.	160721735302	YADA AKSHAY KUMAR
35.	160721735303	TATIKONDA NAGA RAJ KOUSHIK

36.	160721735304	N SAI VENKAT KUMAR REDDY
37.	160721735305	KADABOINA GIRISH RAJ
38.	160721735306	YELLALA PARTHASARADHI REDDY
39.	160721735307	NANDURI NAGASAI
40.	160721735308	PUJALA SAI CHETAN
41.	160721735309	MOHAMMED SOFI SAMEER
42.	160721735310	IBRAHIM SHAIKH
43.	160721735311	CHOUTAKUR KEERTHANA
44.	160721735312	PIDISHETTY VAKYASRI
45.	160721735313	GUDURU MANISH
46.	160721735314	LAKKOJU SRI VIHAAN CHANDRA
47.	160721735315	PINNINTI THIRUPATHI REDDY
48.	160721735316	PALTAIAH SACHIN
49.	160721735317	PANTANGI VIVEK GOUD
50.	160721735318	N SRIKANTH
51.	160721735319	ABDUL GHAFOOR MOHAMMAD SIDDIQI
52.	160721735320	DANDU PRASHANTH
53.	160721735321	GOVULA SRI SOWMYA
54.	160721735322	ERUKONDA TRISHA
55.	160721735323	KASIREDDY KOMAL PRANAV
56.	160721735324	MEGAVATH MALLESH
57.	160721735325	NEELAKANTAM SHIVA RAM PRASAD
58.	160721735326	KOLLURU VIDYADHAR
59.	160721735327	ANNEBOINA PRAKASH
60.	160721735328	PERUGU UDAY KIRAN
61.	160721735329	MARLA SHIVAJI GOUD
62.	160721735330	VARSHA JYOTHIKA
63.	160721735331	MURAREKAR NITHIN RAJ

FACULTY: I.POORNA CHANDER

METHODIST
COLLEGE OF ENGINEERING & TECHNOLOGY
Estd : 2008
(An Autonomous Institution)
Approved by AICTE, New Delhi & Affiliated to Osmania University
Accredited by NBA and NAAC with A+ Grade
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ELECTRONIC DEVICES ASSIGNMENT-1

ECE III SEM, SEC-B
Date: - 9th NOV 2022 Last Date for Submission: - 20th NOV 2022

Short answer questions

1. Write briefly about drift and diffusion current?
2. Define static and dynamic resistance of PN diode?
3. Define the terms Rectifier & Efficiency?
4. Write any four applications of PN-Diode
5. Differentiate between Transition and Diffusion capacitance in PN junction Diode
6. The diode current is 0.6mA when the applied voltage is 400 mV, and 20mA when the applied voltage is 500mV. Determine ή. Assume kT/q=25mV
7. Compare Avalanche and Zener Breakdown mechanisms
8. A Halfwave rectifier, having a diode of resistance 1k ohm and a load of 1k ohm rectifies an a.c. voltage of 230V, peak value. Calculate peak, average and r.m.s. values of current.
9. Compare HWR,FWR and Bridge wave rectifiesrs
10. Draw the block diagram to get pure DC from AC
11. Draw the CLC filter with Full wave rectifier with its output wave form
12. What do you mean by clipping & what are clipping circuits?

Long answer questions

1. Explain the working operation of **PN** junction diode under forward bias and reverse bias with the help of neat diagram?
2. Write short notes on the following:
   a) Full wave rectifier (b) Photo diode (c)LED
3. With neat circuit diagram explain the working operation of a full wave Bridge rectifier and also derive Ripple factor & Efficiency,TUF
4. With the help of neat circuit diagram explain the following clipping circuits and also draw the transfer characteristics. a)+ve clipping with -2V ref. b)-ve clipping with +2V ref
5. With the help of neat circuit diagram explain the following clamping circuits and also draw the output waveforms. a)+ve clamping b)-ve clamping
6. Half wave rectifier circuit is supplied from a 230V,50HZ supply with a step down ratio of 3:1 to a resistive load of 10Kohm.the diode forward resistance is 75ohm while transformer secondary resistance is 10ohm.Calculate Average ,RMS values of current ,DC output voltage ,efficiency of rectification and ripple factor.
7. With neat circuit diagram explain the working operation of a full wave rectifier with capacitor filter and also derive Ripple factor
8. State and prove the clamping circuit theorem
9. Draw the circuit diagram of Slicer? Explain its Operation and also draw the output wave forms

Faculty
I.Poorna chander
Asst prof,ECE

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Estd : 2008

CIE-I QUESTION PAPER

Hall Tick No: | | | | | | | | | | | | |

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sub: Electronic Devices Date: **23-11-2022**
Branch: ECE Time: 10:00-11:10 Am. Max Marks:25

1. Answer all the Questions in PART-A
2. Answer any three Questions in PART-B

PART-A

Q.No.	Questions	Marks	CO	BL
1	Define the terms i) Mobility ii) Drift Current iii) Diffusion current	2	1	Remembering
2	Draw the following clipping circuit diagram with the neat input & output waveforms a)+ve clipping with -2V ref b)-ve clipping with +2V ref	2	2	Remembering
3	Draw the symbol for a) Tunnel diode b) SCR	2	2	Remembering
4	An Si diode has Reverse Saturation Current 10nA , Operating at 25°C . Calculate diode current for forward bias of 0.6 V	2	1	Understanding
5	What is the role of filters in rectifier circuits?	2	2	Understanding

PART-B

Q.No.	Questions	Marks	CO	BL
6	How is a p-n junction formed? Draw the circuit diagram of p-n junction diode in forward bias and reverse bias. Explain its operation and give V-I characteristics.	5	1	Remembering
7	With neat circuit diagram explain the working operation of a full wave rectifier and also derive Ripple factor & Efficiency.	5	2	Applying
8	Explain Hall Effect and its Applications ?	5	1	Remembering
9	Write short notes on the following: a) UJT b) Photo diode	5	2	Understanding

**********ALL THE BEST**********

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ELECTRONIC DEVICES MID-I QUESTION WISE INTERNAL MARKS

SUB:ELECTRONIC DEVICES I INTERNAL MARKS(DATE 23-11-2022)															
			SHORT ANSWER QUESTIONS					LONG ANSWER QUESTIONS							
S.NO	**ROLL NO**	**NAME OF THE STUDENT**	**Q1(2)**	**Q2(2)**	**Q3(2)**	**Q4(2)**	**Q5(2)**	**Q6((5)**	**Q7(5)**	**Q8(5)**	**Q9(5)**	**Descriptive**	**Quiz-1 (UNIT1,2)**	**ASSI**	SEMINAR /NOTES	**Total Mid-1**
		ATTEMPTED	**61**	**56**	**45**	**38**	**48**	**59**	**52**	**51**	**28**	**25 Marks**	**5 Marks**	**5 Marks**	**5 Marks**	**40 Marks**
		AVERAGE	**1.80**	**1.05**	**0.84**	**0.66**	**1.15**	**3.90**	**2.81**	**2.10**	**1.96**	**13.43**	**4.24**	**4.76**	**4.62**	
1	160721735062	MOLUGURU PALLAVI	2	1	0	0	2	5	2	5	0	**17**	**4**	**5**	5	31
2	160721735063	POTHULA SAI KRISHNA	1	1			0	2	3	1		**8**	**4**	**5**	4	21
3	160721735064	NUNE VINOD	2	1	0	1	2	5	4	3	2	**18**	**5**	**5**	4	32
4	160721735065	TIRUMALA KARTHIKEYA	2	0	0	1	2	4		5	2	**16**	**3**	**4**	4	27
5	160721735067	PATNAIKUNI VENKATA SAI ANIL PATNAIK	2	2	2	2	2	5	5	5		**25**	**5**	**5**	5	40
6	160721735068	RAMAVATH BHANU	2	0	1	0	0	5	5	1	2	**15**	**4**	**5**	4	28
7	160721735069	RACHAMALLU VARUN KUMAR REDDY	2	2	2	1	1	4	4	5	1	**21**	**4**	**5**	5	35
8	160721735070	RATHOD PARASHURAM	2	1	0	1		4		3	3	**14**	**5**	**5**	5	29
10	160721735072	GOPARAJU SAI MADHAV	2	2	0	0		4	4	4		**16**	**4**	**5**	5	30
12	160721735075	SHAIK ABUBAKAR SIDDIK	2	0	0	2	2	4	4	4		**18**	**4**	**4**	4	30
13	160721735076	SHERLA SAI VARDHAN	2	0		2	2	5	4	5		**20**	**5**	**5**	5	35
14	160721735077	SOBIA NAAZ	2	2		0	2	5	0	1		**12**	**4**	**5**	5	26
16	160721735079	SOMAROWTHU SAI BHASKAR	2	1		2	0	5	3	5		**18**	**5**	**5**	5	33
18	160721735081	PENUEL ZECHARAIAH JAMES	2		1		0	3	2		2	**10**	**4**	**5**	4	23
19	160721735082	SYED IMAMUDDIN	2	1	0	0	0	3	4	3		**13**	**5**	**4**	4	26
20	160721735083	TELLABOINA RAJESH	2	0			0	3	4	2		**11**	**4**	**5**	4	24
22	160721735085	TERALA VIGNESH	2	2	2	2	2	5	5	5		**25**	**5**	**5**	5	40
25	160721735088	THATOJU ABHISHEK	2	0	1	1	0	4	3	3		**14**	**4**	**5**	5	28

26	160721735089	UNNI KISHORE	2	1				5	3	3		**14**	**5**	**5**	5	29
28	160721735091	VERTHE SURESH NAIK	2	1	0		2	5	3	1		**14**	**4**	**5**	5	28
29	160721735092	VODNALA NITHIN	2	0				3	4		2	**11**	**4**	**5**	5	25
30	160721735093	GARLAPALLI SAI RAJITHA	2	0	0	0	0	3	4	0	0	**9**	**4**	**5**	5	23
33	160721735301	BHAVANA GUNDLAPALLY	2	2	1	0	2	5	4	5		**21**	**5**	**5**	5	36
34	160721735302	YADA AKSHAY KUMAR	2	1	2	0	2	5		3	5	**20**	**5**	**5**	5	35
35	160721735303	T NAGARAJ KOUSHIK	2		1	1	0	4	3	3		**14**	**5**	**5**	4	28
36	160721735304	N SAI VENKAT KUMAR REDDY	2	2	2		2	5	3		5	**21**	**5**	**4**	4	34
37	160721735305	KADABOINA GIRISH RAJ	2		2		2	3	3		2	**14**	**4**	**5**	4	27
38	160721735306	Y PARTHA SARADHI REDDY	2	1	1		0	4	3	4		**15**	**4**	**5**	5	29
39	160721735307	NANDURI NAGASAI	2	2	0		2	5		0	0	**11**	**5**	**5**	5	26
40	160721735308	PUJALA SAI CHETAN	0	2	2	0	2	3	2		3	**14**	**4**	**4**	4	26
41	160721735309	MD SOFT SAMEER	2	2	0	0	1	4		5	3	**17**	**5**	**5**	5	32
42	160721735310	IBRAHIM SHAIKH	2	1			2	4		5	0	**14**	**4**	**5**	5	28
43	160721735311	CHOUTAKUR KEERTHANA	2	2	1		1	4	3		1	**14**	**4**	**5**	5	28
44	160721735312	P VAKYASRI	2	0	1	0	2	5	2	1	2	**14**	**4**	**5**	5	28
45	160721735313	GUDURU MANISH	2	0	1	0		3	1	0		**7**	**4**	**5**	5	21
46	160721735314	L SRI VIHAAN CHANDRA	1	0	2	0	0	5	2		4	**14**	**5**	**5**	5	29
47	160721735315	P THIRUPATHI REDDY	2	1	0	0	2	4	3	2		**14**	**4**	**4**	4	26
48	160721735316	P SACHIN	2	0	1	0	2	5		0	4	**14**	**5**	**5**	5	29
49	160721735317	P VIVEK GOUD	2	1			2	5	1		0	**11**	**5**	**4**	4	24
50	160721735318	N SRIKANTH	1	2	2	2		5	3	0		**15**	**5**	**5**	4	29
52	160721735320	D PRASHANTH	1	2	2	0	1	4	3	1		**14**	**4**	**5**	5	28
53	160721735321	GOVULA SRI SOWMYA	2	0	0	0	1	5	3	0		**11**	**4**	**5**	5	25
54	160721735322	ERUKONDA TRISHA	2	2	1	1	2	4	4	0		**16**	**5**	**5**	5	31
55	160721735323	KASIREDDY KOMAL PRANAV	1	0	0	0		5	0	0		**6**	**5**	**4**	4	19
56	160721735324	MEGAVATH MALLESH	2	2	2			5	4	0		**15**	**5**	**5**	5	30
57	160721735325	N SHIVA RAM PRASAD	2	2		0	0	5	4	1		**14**	**5**	**5**	5	29
58	160721735326	KOLLURU VIDYADHAR	2	2	2		0	4	3		2	**15**	**5**	**5**	5	30
59	160721735327	ANNEBOINA PRAKASH	2	2	0	0	2	3	3	2		**14**	**4**	**5**	5	28
60	160721735328	PERUGU UDAY KIRAN	2	2		2	2	4	4	2		**18**	**3**	**4**	4	29
61	160721735329	MARLA SHIVAJI GOUD	2	1	1	0	0	3	3	2		**12**	**4**	**4**	4	24

62	160721735330	VARSHA JYOTHIKA	0	1	1		2	3	2	2		**11**	**4**	**5**	5	25
63	160721735331	M NITHIN RAJ	2	2	1	2		4	3	2	1	**16**	**5**	**4**	4	29
		ABOVE BENCH MARK	59	37	26	16	31	54	37	20	8	39	61	63	63	
		COUNT	61	56	45	38	48	59	52	51	28	61	63	63	63	
			96.72	66.07	57.78	42.11	64.58	91.53	71.15	39.22	28.57	63.93	96.83	100.00	100.00	

ATTAINMENTS CIE-I

	Part A				**Part B**							
Question number	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**QUIZ**	**ASSIGN MENT**	**class test**
Maximum Marks of the question	2	2	2	2	2	5	5	5	5	5	5	5
Average marks of student	**1.80**	**1.05**	**0.84**	**0.66**	**3.90**	**3.90**	**2.81**	**2.10**	**1.96**	4.24	4.76	4.62
Satisfactory mark set as base mark	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%
No. of students obtained base mark& above	59	37	26	16	31	54	37	20	8	61	63	63
No. of students attempted	61	56	45	38	59		52	51	28		97	97
% Students obtained base mark& above	96.72	66.07	57.78	42.11	64.58	91.53	71.15	39.22	28.57	96.83	100.00	100.00
CO Attainment												**Over all**
CO 1	96.72			42.11		91.53		39.22		100	100	78.26
CO 2		66.07	57.78		64.58		71.15		28.57	100	100	69.74
CO 3												
CO 4												
CO 5												
CO 6												

FACULTY: I.POORNA CHANDER
ASSISTANT PROF.
ECE DEPARTMENT,

9963390390, ipurnachander@methodist.edu.in

SUBJECT: ED SEM & SECTION: III

LIST OF SLOW LEARNERS AS PER INTERNAL MARKS (AT THE BEGINNING OF SEMESTER)

Sl.No	Roll Number	Name Of the Student
1.	160721735071	SAAD KHAN
2.	160721735074	SHAIK SOHAIL
3.	160721735078	MD FURQUAN NAWAZ
4.	160721735080	SR PREM KUMAR
5.	160721735084	K ANIL KUMAR
6.	160721735086	SUNNY T
7.	160721735087	MUNIGALA SATHWIK
8.	160721735090	CHENUMALLA KOUSHIK
9.	160721735094	VARAGANTIPAVANKUMAR
10.	160721735096	RAVISHWAS GOUD
11.	160721735319	ABDUL GHAFOOR MD SIDDIQI

FACULTY: **HOD:**

I POORNA CHANDER

Department of Electronics and communication Engineering

A.Y: SUBJECT: ED SEM & SECTION: III

LIST OF ADVANCED LEARNERS AS PER INTERNAL MARKS (AT THE BEGINNING OF THE SEMESTER)

Sl.No	Roll Number	Name Of the Student
1.	160721735064	NUNE VINOD
2.	160721735067	PATNAIKUNI VENKATA SAI ANIL PATNAIK
3.	160721735069	RACHAMALLU VARUN KUMAR REDDY
4.	160721735076	SHERLA SAI VARDHAN
5.	160721735079	SOMAROWTHU SAI BHASKAR
6.	160721735085	TERALA VIGNESH
7.	160721735301	BHAVANA GUNDLAPALLY
8.	160721735302	YADA AKSHAY KUMAR
9.	160721735304	N SAI VENKAT KUMAR REDDY
10.	160721735309	MD SOFT SAMEER

FACULTY: **HOD:**

I POORNA CHANDER

Academic Year – 2022 – 2023

Department of Electronics and communication Engineering

A.Y:2022-23 SUBJECT: ED SEM & SECTION: III

LIST OF SLOW LEARNERS AS PER INTERNAL – I

Sl.No	Roll Number	Name Of the Student
1.	160721735071	SAAD KHAN
2.	160721735074	SHAIK SOHAIL
3.	160721735078	MD FURQUAN NAWAZ
4.	160721735080	SR PREM KUMAR
5.	160721735086	SUNNY T
6.	160721735090	CHENUMALLA KOUSHIK
7.	160721735094	VARAGANTIPAVANKUMAR
8.	160721735096	RAVISHWAS GOUD
9.	160721735319	ABDUL GHAFOOR MD SIDDIQI
10.	160721735323	KASIREDDY KOMAL PRANAV

FACULTY: **HOD:**

I POORNA CHANDER

Department of Electronics and communication Engineering

A.Y: 2022-23 SUBJECT: ED SEM & SECTION: IV

LIST OF ADVANCED LEARNERS AS PER INTERNAL – I

Sl.No	Roll Number	Name Of the Student
11.	160721735064	NUNE VINOD
12.	160721735067	PATNAIKUNI VENKATA SAI ANIL PATNAIK
13.	160721735069	RACHAMALLU VARUN KUMAR REDDY
14.	160721735076	SHERLA SAI VARDHAN
15.	160721735079	SOMAROWTHU SAI BHASKAR
16.	160721735085	TERALA VIGNESH
17.	160721735301	BHAVANA GUNDLAPALLY
18.	160721735302	YADA AKSHAY KUMAR
19.	160721735304	N SAI VENKAT KUMAR REDDY
20.	160721735309	MD SOFT SAMEER

FACULTY: **HOD:**

I POORNA CHANDER DR. V S S N SRINIVASA BABA

Department of Electronics and Communication Engineering

B.E III SEM **YEAR 2022-23**

Branch: ECE – **A** Subject: **ED**

Class attendance sheet for Slow Learners

S.NO	ROLL NO	DATES					
		20/11/2022	27/11/2022	4/12/2022	18/12/2022	22/01/2023	29/01/2023
1	160721735071	P	P	A	P	P	P
2	160721735074	P	P	P	P	P	A
3	160721735078	A	P	P	P	P	P
4	160721735080	P	P	P	A	P	P
5	160721735086	A	P	P	P	P	P
6	160721735090	P	P	P	A	P	P
7	160721735094	P	P	P	A	P	P
8	160721735096	P	P	P	A	P	P
9	160721735319	P	P	P	A	P	P
10	160721735323	P	P	P	A	P	P

FACULTY **HOD**

Department of Electronics and Communication Engineering

Topics for Slow Learners

B.E III SEM **YEAR 2022-23**

Branch: ECE – **B** Subject: **ED**

1. What is a pn junction? How is it formed?.
2. Applications Of PN Junction Diode as Clippers, Clampers
3. Applications Of PN Junction Diode as Rectifiers, Filters
4. Construction and operation of BJT
5. Small signal Analysis of BJT& FET
6. Special purpose Diodes

Department of Electronics and Communication Engineering

Topics for Advanced Learners

B.E III SEM **YEAR 2022-23**

Branch: ECE – **B** Subject: **ED**

1. Diode current Equation, Problems
2. Applications Of PN Junction Diode as Clippers, Clampers
3. Applications Of PN Junction Diode as Rectifiers, Filters
4. Construction and operation of BJT
5. Small signal Analysis of BJT& FET Amplifiers
6. Special purpose Diodes
7. Construction and Formation of JFET & MOSFET and its characteristics'

ELECTRONIC DEVICES

ASSIGNMENT-2

Date: - 06 JAN 2023 **Last Date for Submission: - 20 Jan 2023**

Short answer questions

1. What is the need for biasing?
2. The following quantities are measured in a transistor I_C=5mA,I_B=100μA determine α,βand I_E
3. Draw the transistor hybrid model for CE transistor configuration
4. What is meant by thermal run away?
5. Compare BJT and FET
6. What are the characteristics and applications of common collector amplifier?
7. Draw the symbols of JFET, Depletion MOSFET, Enhancement MOSFET for n-channeland p-channel
8. Draw the transistor hybrid model for CB transistor configuration
9. Draw the transfer characteristics of MOSFET
10. Define Drain resistance r_d, Trans conductance g_d and amplification factor μ for JFET
11. Define stability factors S and S'

Long answer questions

1. Draw the circuit of self-biased CE-amplifier using diode compensation for Ico. Describehow bias compensation is achieved
2. A C.E amplifier is driven by a voltage source of internal resistance Rs = 800Ω, the load impedance is a of 2 k Ω. The h-parameters are hie = 1.1 k, hfe = 50, hoe= 25Micro ohms,hre = 2.5x10-4 . Compute the current gain Ai, input resistance Ri, output resistance Ro a.Also, voltage gain Aν calculate power gain Ap using approximate analysis.
3. (a) With the neat sketch explain input and output characteristics of CE configuration and derive its collector current equation.
   (b) For the self bias circuit R_1 = 20KΩ, R_2 = 80KΩ, R_C = 2KΩ, R_E = 1KΩ calculate Stability factor for beta = 100.
4. A common base transistor amplifier driven by a voltage source of internal resistance Rs = 1.2 , hrb =3x10-4Ω . The h - parameters are hib = 22Ω , the load impedance is 1 kΩk , hfb = -0.98 A/V, and hob = 0.5μ A/V Compute the current gain AI, Input Impedance Ri voltage gain Av, overall voltagegain Avs, overall current gain Ais, and power gain. Use exact analysis.
5. (a) Explain the basic operation and characteristics of enhancement type MOSFET
6. Write short noted on
   a. LED, (b) Tunnel diode and (c) Bias compensation techniques
7. (a)Draw and explain Self bias circuit and derive Stability factor S
   (b) Draw and explain fixed bias circuit and Stability factor S
8. Explain the basic construction and operation of a n-channel JFET. Draw and explain itscharacteristics.
9. Draw and explain small signal approximate model for CE Amplifier and derive the respective parameters

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CIE-II QUESTION PAPER

Hall Tick No: | | | | | | | | | | | | |

METHODIST
COLLEGE OF ENGINEERING & TECHNOLOGY
Accredited by NAAC with A+ and NBA
Estd : 2008 Affliated to Osmania University &Approved by AICTE

NATIONAL BOARD OF ACCREDITATION

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Sub: **Electronics Devices (ED) (5PC 301EC)** Date: **20-01-2023**
Branch: ECE Time: 10:00-11:10 Am. Max Marks:25

1. Answer all the Questions in PART-A
2. Answer any three Questions in PART-B

PART-A

Q.No.	Questions	Marks	CO	BL
1	Why BJT is called current controlled device and FET as voltage controlled device?	2	3	Understanding
2	Define α , β and γ relation	2	3	Remembering
3	Define μ, r_d & g_m of an FET and show that μ=$r_d * g_m$?	2	6	Remembering
4	Draw the symbols of JFET, Depletion MOSFET, Enhancement MOSFET for n-channel and p-channel	2	6	Remembering
5	Briefly explain the need of Biasing ?	2	5	Understanding

PART-B

Q.No.	Questions	Marks	CO	BL
6	Explain the construction and operation n-channel JFET With neat static characteristics curves and define the pinch-off voltage and indicate its location on drain characteristics	5	6	Understanding
7	Draw the approximate model of an emitter follower (CC Configuration) and derive the expression for its Current gain A_I, Input resistance R_i , voltage gain A_V, Output resistance R_O .	5	4	Applying
8	Explain input & output characteristics of CE configurations & Derive the equation for I_C .	5	3	Remembering
9	Write short notes on the following: a) Fixed bias b) Self bias	5	5	Remembering

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ED MID-II QUESTION WISE INTERNAL MARKS

SUB:ELECTRONIC DEVICES II INTERNAL MARKS(DATE 20-1-2023)																
			SHORT ANSWER QUESTIONS					LONG ANSWER QUESTIONS								
S.NO	**ROLL NO**	**NAME OF THE STUDENT**	**Q1(2)**	**Q2(2)**	**Q3(2)**	**Q4(2)**	**Q5(2)**	**Q6((5)**	**Q7(5)**	**Q8(5)**	**Q9(5)**	**Descriptive**	**Quiz-2 (UNIT 3,4,5)**	ASSI	SEMINAR /NOTES	**Total**
		ATTEMPTED	**60**	**39**	**34**	**56**	**57**	**58**	**43**	**52**	**33**	**25 Marks**	**5 Marks**	**5 Marks**	**5 Marks**	**40 Marks**
		AVERAGE	**1.08**	**0.62**	**0.97**	**1.41**	**1.11**	**2.47**	**0.86**	**1.62**	**0.91**	**9.25**	**3.71**	**3.90**	**5.00**	**21.86**
1	160721735062	MOLUGURU PALLAVI	2	2	2	2	2	5	0	3		18	4	5	5	32
2	160721735063	P.SAI KRISHNA	0	0		2	2	3		1	0	8	5	3	5	21
3	160721735064	NUNE VINOD	1			0	0	4		0	0	5	3	3	5	16
4	160721735065	TIRUMALA KARTHIKEYA	1	0	2	2	2	0	2		0	9	2	3	5	19
5	160721735067	P.VENKATA SAI ANIL PATNAIK	2	1	2	2	1	2	3	3	4	18	4	5	5	32
6	160721735068	RAMAVATH BHANU	2	0		2	0	0	1	1	0	6	4	3	5	18
7	160721735069	R.VARUN KUMAR REDDY	0	0	1	2	2	4	2	1	1	12	3	5	5	25
8	160721735070	RATHOD PARASHURAM	1	0		2	2	5		1	0	11	4	3	5	23
9	160721735071	SAAD KHAN	2			0	0	0	0	0	0	2	3	3	5	13
10	160721735072	GOPARAJU SAI MADHAV	2		1	1	2	5		5	1	17	4	5	5	31
11	160721735074	SHAIK SOHAIL	0	0	0		1	0	0	0	1	2	2	3	5	12
12	160721735075	SHAIK. ABUBAKAR SIDDIK	0		1	2	2	1	0	0		6	4	5	5	20
13	160721735076	S.SAI VARDHAN	2		0	2	1	1	1	4		11	4	5	5	25
14	160721735077	SOBIA NAAZ	2		1	2	2	3	0	1		11	4	5	5	25
15	160721735078	MD.FURQUAN NAWAZ	2			2	2	2	0	0		8	3	3	5	19
16	160721735079	SOMAROWTHU SAI BHASKAR	2	2	1	1	2	5		5	0	18	4	5	5	32
17	160721735080	SR.PREM KUMAR	2	0		0	0	1	0		0	3	3	3	5	14
18	160721735081	PENUEL ZECHARIAH	1			2	2	0		0	0	5	4	3	5	17

		JAMES														
19	160721735082	SYED IMAMUDDIN	2	0	1	0	0	3		0	0	6	4	3	5	18
20	160721735083	TELLABOINA RAJESH	0			2	2	0	0	0		4	3	3	5	15
21	160721735084	K ANIL KUMAR	0			0	0	0		2	0	2	4	3	5	14
22	160721735085	TERALA VIGNESH	2	1	1	2	2	5		4	5	22	3	5	5	35
23	160721735086	SUNNY T	0	0	0	0	0	1	0	1		2	5	3	5	15
24	160721735087	M. SATHWIK	0			0	0	1	0		1	2	4	3	5	14
25	160721735088	THATOJU ABHISHEK	0	0	1	2		0	0	3		6	4	3	5	18
26	160721735089	U KISHORE	0	2	1		2	5	5		4	19	4	5	5	33
27	160721735090	CH. KOUSHIK	0	0		2	2	1		2	0	7	4	3	5	19
28	160721735091	V.SURESH NAIK	0			0	1	5	1	0		7	4	5	5	21
29	160721735092	VODNALA NITHIN	0			0	0	4	0	0		4	4	3	5	16
30	160721735093	GARLAPALLI SAI RAJITHA	0		0	0	0	3	1	2	0	6	4	3	5	18
31	160721735094	VARAGANTIPAVANKUMAR	0						0	0	0	0	2	3	5	10
32	160721735096	RAVISHWAS GOUD	2	2	1	0	0	0	0	0		5	2	5	5	17
33	160721735301	BHAVANA GUNDLAPALLY	2	0	1	2	2	5		2	2	16	4	5	5	30
34	160721735302	YADA AKSHAY KUMAR	2	0	1	2	2	3	0	4		14	5	5	5	29
35	160721735303	T.NAGARAJ KOUSHIK	2	2	2	2	2	0	2	3		15	4	5	5	29
36	160721735304	N.SAI VENKAT KUMAR REDDY	2	1		2	2	5	0	1		13	3	3	5	24
37	160721735305	KADABOINA GIRISH RAJ	2	0		2	2	0	0	2		8	5	3	5	21
38	160721735306	Y. PARTHASARADHI REDDY	0	0		2	2	2	1	2		9	4	5	5	23
39	160721735307	NANDURI NAGASAI	2			1	2	3	0	1		9	4	3	5	21
40	160721735308	PUJALA SAI CHETAN	0	0	2	2	0	2		1	0	7	4	3	5	19
41	160721735309	MOHAMMED SOFI SAMEER	1			0	0	5		1	0	7	3	3	5	18
42	160721735310	IBRAHIM SHAIKH	1	1	1	2	2	0	0		2	9	3	3	5	20
43	160721735311	CHOUTAKUR KEERTHANA	2	0		2	0	2		1	0	7	4	3	5	19
44	160721735312	PIDISHETTY VAKYASRI	0	0	1	2	2	2	0	3		10	3	5	5	23
45	160721735313	GUDURU MANISH	2			2	1	0	0	3		8	5	5	5	23
46	160721735314	L SRI VIHAAN CHANDRA	2	0	0	1	0	5	4		4	16	4	5	5	30
47	160721735315	PINNINTI THIRUPATHI REDDY	2	0	1	2	2	3		2	2	14	3	5	5	27

48	160721735316	PALTAIAH SACHIN	1			1	1	2	2	3		10	4	5	5	24
49	160721735317	PANTANGI.VIVEK GOUD	0	0		0	1	2	1		0	4	4	3	5	16
50	160721735318	N SRIKANTH	2	0		2	2	2	2	0		10	5	5	5	25
51	160721735319	ABDUL GHAFOOR MD SIDDIQI	0			0	0	0	0		1	1	3	3	5	12
52	160721735320	DANDU PRASHANTH	2	2	1	2	0	3	1	2		13	2	5	5	25
53	160721735321	GOVULA SRI SOWMYA	0	1	0	2		5		3	2	13	4	5	5	27
54	160721735322	ERUKONDA THRISHA	2	2	1	2	2	5	5	4		23	4	5	5	37
55	160721735323	KASIREDDY KOMAL PRANAV	0	2	2		0	4	0	0		8	4	3	5	20
56	160721735324	MEGAVATH MALLESH	0	1	1	2	0	5	3	2		14	4	5	5	28
57	160721735325	N.SHIVA RAM PRASAD	2	0	0	2	0	5		2	0	11	4	3	5	23
58	160721735326	KOLLURU VIDYADHAR	2	2	2	2	2	1	0	3		14	4	3	5	26
59	160721735327	ANNEBOINA PRAKASH	0	0	0	2	0		0	0	0	2	4	5	5	16
60	160721735328	PERUGU UDAY KIRAN	2		1	2	0	3	0	0		8	3	3	5	19
61	160721735329	MARLA SHIVAJI GOUD	0	0	0	2	0	5	3	2		12	3	3	5	23
62	160721735330	VARSHA. JYOTHIKA	2		1	2	2	3	1		1	12	3	5	5	25
63	160721735331	MURAREKAR NITHIN RAJ	0	0		2	0	0		1	1	4	5	3	5	17
		ABOVE BENCH MARK	36	15	26	42	35	44	17	36	13	17	55	60	60	
		COUNT	60	39	34	56	57	58	43	52	33	60	60	60	60	
			60.00	38.46	76.47	75.00	61.40	75.86	39.53	69.23	39.39	28.33	91.67	100.00	100.00	

ATTAINMENTS CIE-II

	Part A				Part B							
Question number	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**QUIZ**	**ASSIGNMENT**	**class test**
Maximum Marks of the question	2	2	2	2	2	5	5	5	5	5	5	**5**
Average marks of student	**1.08**	**0.62**	**0.97**	**1.41**	**1.11**	**2.47**	**0.86**	**1.62**	**0.91**	3.71	3.9	**5**
Satisfactory mark set as base mark	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%	50%
No. of students obtained base mark& above	36	15	26	42	35	44	17	36	13	55	60	**60**
No. of students attempted	60	39	34	56	58		43	52	33		97	**97**
% Students obtained base mark& above	60.00	38.46	76.47	75.00	61.40	75.86	39.53	69.23	39.39	91.67	100.00	100.00
CO Attainment												**overall**
CO 1												
CO 2												
CO 3	60.00	39.00						69.23				56.08
CO 4							39.53			100	100	79.84
CO 5					75.862069				39.39	100	100	78.81
CO 6			76.47	75.00		75.86						75.78

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ELECTRONIC DEVICES EXTERNAL EDC MODEL PAPERS 1

Time: 3 hours **Max. Marks: 75**

PART-A

Answer all the following questions:

(a) What is a pn junction? How is it formed? (2M)

(b) Sketch the energy-band picture for (3M)

i} an intrinsic ii}n-type iii} a p-type semiconductor

Indicates the positions of the fermi, the donor &the acceptor levels.

(c) What is meant by rectifier? (2M)

(d) Compare the performance measure of different filters. (3M)

(e) Why Transistor is called Current Controlled Device? (2M)

(f)What is early effect? How does it modify the V-I characteristics of a BJT? (3M)

(g) What is meant by operating point? Explain its significance (2M)

(h)What is the condition for thermal stability and thermal resistance? (3M)

(i) Explain when a FET acts as a voltage variable resistor. (2M)

(j) Explain the drain and transfer characteristics of a JFET in details (3M)

Answer all the following questions **10x5=50**

2.a) Derive an expression for total diode current starting from Boltzmann relationship in terms of the applied voltage.

b) The reverse saturation current of a silicon p – n function diode at an operating temperature of 270C is 50 nA. Compute the dynamic forward and reverse resistances of the diode for applied voltages of 0.8 V and -0.4 V respectively.

OR

3.a) Explain the operation of silicon p – n junction diode and obtain the forward bias and reverse bias Volt – Ampere characteristics.

b) Obtain the transition capacitance C_T of a junction diode at a reverse bias voltage of 12 V if C_T of the diode is given as 15 PF at a reverse bias of 8 V. Differentiate between transition and diffusion capacitances.

4.a) Define the following terms of a rectifier and filter:

i) Ripple Factor

ii) Regulation

iii) Rectification Efficiency

iv) Form Factor

b) What is the ripple factor if a power supply of 220 V, 50 Hz is to be Full Wave rectified and filtered with a 220μF capacitor before delivering to a resistive load of 120Ω? Compute the value of the capacitor for the ripple factor to be less than 15%.

OR

5.a) Derive expressions for ripple factor of a Full Wave Rectifier with and without a capacitive filter.

b) Compute the average and RMS load currents, TUF of an unfiltered centre tapped Full Wave Rectifier specified below.

Input voltage to transformer = 220 V/50 Hz.

Step down ratio of centre tapped transformer = 4:1(Primary to each section secondary).

Sum of transformer secondary winding in each secondary segment and diode forward resistance = 100Ω. Load resistance, RL= 220Ω.

6.a) With the help of input & output characteristics, explain the operation of a BJT in Common Emitter Configuration.

b) For an NPN transistor with α_N= 0.98, I_{CO}= 2μA and I_{EO}= 1.6μA connected in Common Emitter Configuration, calculate the minimum base current for which the transistor enters into saturation region. V_{CC} and load resistance are given as 12 V and 4.0 KΩ respectively.

OR

7.a) Compare the characteristics of a BJT in CB, CE and CC configurations.

b) A Silicon BJT is connected in common Emitter configuration with collector – to –Base bias. Calculate the base resistance R_b for the quiescent collector – to – Emitter voltage, V_{CE} has to be 4 V. V_{CC} and R_C are given as 2 V and 1 KΩ respectively. Assume β= 100, V_{BE} to be zero volts. Also find the stability factor of the circuit.

8.a) Explain how self biasing can be done in a BJT with relevant sketches and waveforms.

b) Design a self bias circuit for the following specifications: V_{CC} = 12 V; V_{CE} = 2V; I_C = 4mA; h_{fe} = 80. Assume any other design parameters required. Draw the designed circuit.

OR

9.a) Explain how biasing is provided to a transistor through potential divider bias. List the assumptions made. List the need of bias compensation methods.

b) An NPN transistor with β= 50 is used in common Emitter configuration with V_{CC} = 10V and R_C = 2.2 KΩ. Biasing is done through a 100 KΩ resistance from collector – to – Base. Assuming V_{BE} to be zero volts, Find i) The quiescent point ii) The stability factor, „S".

10.a) Detail the construction of an n-channel MOSFET of depletion type. Draw and explain its characteristics.

b) A self biased p – channel JFET has a pinch – off voltage of VP = 5 V and IDSS = 12 mA. The supply voltage is 12 V. Determine the values of RD and RS so that ID = 5 mA and VDS = 6V.

OR

11.a) Explain the significance of threshold voltage of a MOSFET. Discuss the methods to reduce threshold voltage, V_T.

b) A FET follows the relation $I_D = I_{DSS}[1 - V_{GS}/V_p]^2$. What are the values of ID and gm for VGS = -1.5 V if IDSS and VP are given as 8.4 mA and -3V respectively.

ELECTRONIC DEVICES EXTERNAL EDC MODEL PAPERS 2

Time: 3 hours **Max. Marks: 75**

PART-A

1.Answer all the following questions:

(a)What do you mean by potential barrier for a p-n junction? (2M)

(b)What is the significance of negative resistance of a tunnel diode (3M)

(c) Define peak inverse voltage (PIV). (2M)

(d) Explain FWR working principle with circuit and waveforms. (3M)

(e)What are the three regions of a Transistor? (2M)

(f) What is thermal runway ? how can it avoided? (3M)

(g)What is faithful amplification? (2M)

(h) How α,β and γ are related to each other? (3M)

(i) Define the pinch off voltage (Vp) sketch the depletion region before and after pinchoff? (2M)

(j) Derive Expression for saturation drain current (3M)

Answer all the following questions: 5x10= 50 marks

1. Difference between

i) Static and dynamic resistances of a p – n diode.

ii) Transition and Diffusion capacitances of a p – n diode.

iii)Volt – Ampere characteristics of a single silicon p – n diode and two identical silicon p- n diodes connected in parallel.

iv) Avalanche and zener break down mechanisms

OR

3.a) Define the following terms for a PN diode

i) Dynamic resistance

ii) Load line

iii) Difference capacitance

iv) Reverse saturation current

b) A reverse bias voltage of 90V is applied to a Germanium diode through a resistance R. The reverse saturation current of the diode is 50 μA at an operating temperature of 250C. Compute the diode current and voltage for

i) R = 10 MΩ

ii) R = 100 KΩ

4.a) Define Ripple factor and form factor. Establish a relation between them.

b) Explain the necessity of a bleeder resistor in an L – section filter used with a Full Wave filter.

c) Compute ripple factor of an L – section choke input filter used at the output of a Full wave rectifier and capacitor values of the filter are given as 10 H and 8.2 μF respectively.

OR

5.a) List out the merits and demerits of Bridge type Full Wave rectifiers over centre tapped type Full Wave rectifiers.

b) The secondary voltages of a centre tapped transformer are given as 60V-0V-60V the total resistance of secondary coil and forward diode resistance of each section of transformer secondary is 62 Ω. Compute the following for a load resistance of 1 KΩ.

i) Average load current

ii) Percentage load regulation

iii) Rectification efficiency

iv) Ripple factor for 240 V/50Hz supply to primary of transformer.

c) What is bleeder resistance in L – section filters?

6.a) Describe the significance of the terms, „α" and „β". Establish a relation between them.

b) A transistor is operated at a forward emitter current of 2 mA and with the collector open – circuited. Assuming $\alpha_N = 0.98$, $I_{EO} = 1.6$ μA and $I_{CO} = 2$ μA, determine

i) The junction voltages V_C and V_E

ii) The collector to Emitter voltage V_{CE}

iii) The region of transistor operation (Saturation/Active/Cut-off).

Assume any other values necessary.

OR

7.a) Describe the functioning of a BJT in common base configuration.

b) Determine the collector current of a BJT with both of its junctions reverse biased. Assume $I_{CO} = 5$μA, $I_{EO} = 3.58$ μA, $\alpha_N = 0.98$ and any other parameter values as required.

c) How do you identify the region of operation of a BJT to be saturation region from the values of various circuit currents?

8.a) Justify statement "Potential divider bias is the most commonly used biasing method" for BJT circuits. Explain how bias compensation can be done in such biasing through diodes.

b) An NPN transistor with β= 100 is used in common Emitter configuration with Collector – to – Base bias. If VCC = 10 V, RC = 1 K and VBE = 0 V, determine i)Rb such that quiescent Collector – to – Emitter Voltage is 4V.

ii) The stability factor, „S".

OR

9.a) Define all the four hybrid parameters of a BJT in CE configuration. Draw the circuit and its equivalent circuit.

b) The source and load resistances connected to a BJT amplifier in

CE configuration are 680Ω and 1 KΩ respectively. Calculate the voltage gain AV and the input resistance R_i if the h-parameters are listed as h_{ie} = 1.1 kΩ ; $h_{re} = 2\times10^{-4}$; h_{fe}= 50 and h_{oe}= 20 μmhas. Compute A_V and R_i using both approximate and exact analysis.

10.a) With the help of a neat schematic, explain the functioning of a common source amplifier.

b) Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers.

OR

11.a) Differentiate between enhancement and depletion modes of a MOSFET with the help of its characteristics and construction.

b) Determine the pinch off voltage for an N – channel silicon. JFET if the thickness of its gate region is given as 3.2×10^{-4}cm and the donor density in n-type region is $1.2x10^{-5}/cm^3$.

c) Establish a relation between the three JFET parameters, μ, r_d and g_m.

ELECTRONIC DEVICES EXTERNAL EDC MODEL PAPERS 3

Time: 3 hours **Max. Marks: 75**

PART-A

Answer all the following questions:

(a)What is mean by zener breakdown (2M)

(b)Explain the effect of temperature on the V-I characteristics of pn junction diode (3M)

(c)What is meant by filter (2M)

(d)Bridge rectifier is becoming more and more popular, why? (3M)

(e)Write B.J.T specifications (2M)

(f) Explain how transistor acts as an Amplifier? (3M)

(g)What is meant by stabilization (2M)

(h)What is thermal runway? How can it avoid? (3M)

(i)State the application of JFET (2M)

(j) When FET acts as a voltage variable resistor (vvr)? (3M)

Answer all the following questions: 5x10= 50 marks

2.a) Explain the concept of diode capacitance. Derive expression for transition capacitance?

b) Find the value of D.C. resistance and A.C resistance of a Germanium junction diode at 25^0C with reverse saturation current, I_o= 25μA and at an applied voltage of 0.2V across the diode.

OR

3.a) What do you understand by depletion region at p-n junction? What is the effect of forward and reverse biasing of p-n junction on the depletion region? Explain with necessary diagrams.

b) Explain Zener and avalanche breakdown mechanisms in detail.

4. Define the following terms and derive the equations with respect to half-wave rectifier: i) Ripple factor ii) Peak inverse voltage iii) Rectification efficiency iv) % Regulation.

OR

5.a) Draw the circuit diagram of full-wave rectifier with inductor filter. Explain its operation with necessary equations.

b) A HWR circuit supplies 100mA DC current to a 250Ω load. Find the DC output voltage, PIV rating of a diode and the r.m.s. voltage for the transformer supplying the rectifier

6.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CB configuration. Also derive expression for output current.

b) Derive the relation among α, β and γ.

OR

7.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.

b) Calculate the collector current and emitter current for a transistor with α= 0.99 and ICBO= 50μA when the base current is 20μA.

8.a) Explain the basic requirements of transistor biasing. Verify these requirements in collector to base bias circuit.

b) Design a fixed bias circuit using silicon transistor, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ= 8V, ICQ = 4 mA & β= 50.

OR

9.a) What is thermal runaway in transistors? Obtain the condition for thermal stability in transistors.

b) Draw the circuit diagram, AC equivalent & small signal equivalent of Emitter Follower amplifier using accurate h-parameter model. Derive expressions for AVs , AIs, RI & RO.

10.a) Explain the construction & operation of an N-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.

b) Define pinch-off voltage and transconductance in field effect transistors.

OR

11(a) Write short notes on applications of FET as a voltage variable resistor.

b) Explain the principle of CS amplifier with the help of circuit diagram. Derive the expressions for A_V, input impedance and output impedance.

ELECTRONIC DEVICES EXTERNAL EDC MODEL PAPERS 4

Time: 3 hours **Max. Marks: 75**

PART-A

1. Answer all the following questions:

a) What is diode equation? (2M)

b) Draw the v-I characteristics of SCR & define all related terms. (3M)

c) What is the purpose of bleeder resistance in a rectifier circuit using LC filter? (2M)

d) Write short note on Full wave rectifier (FWR) along with input output waveforms. (3M)

e) Why hybrid parameters are called so? Define those (2M)

f) What factors are to be considered for selecting the operating point Q for an amplifier? (3M)

g) Why does potential divider method of biasing become universal? (2M)

h) What is the major difference between a BJT and FET? (3M)

i) Draw the symbols of JFET (N Channel/P channel) MOSFET (Depletion MOSFET (n-channel/p-channel)and Enhancement MOSFET (n-channel/p-channel) (2M)

j) Draw the low frequency hybrid equivalent circuit for C.E .C.B and CC (3M)

Answer all the following questions: 5x10= 50 marks

2.a) Explain about various current components in a forward biased p-n junction diode.

b) With neat sketches and necessary waveforms explain about the regulation characteristics

OR

3.a) With neat sketches and necessary waveforms explain the volt ampere characteristics of PN diode.

b) Explain the temperature dependence of VI characteristics of PN diode.

c) Compare ideal and practical diodes.

4.a) Draw the circuit of full-wave rectifier with capacitor filter. Explain its operation with necessary equations.

b) A full wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A DC voltmeter connected across the load of 1KΩ reads 55.4 volts. Calculate

i) Irms

ii) Average voltage across each diode

iii) ripple factor iv) Transformer secondary voltage rating.

OR

5.a) Draw the circuit of full-wave rectifier with L-section filter and derive expression for its ripple factor.

b) A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω,

determine

i) dc voltage across the load.

ii) dc current flowing through the load.

iii) dc power delivered to the load.

iv) PIV across each diode.

6.a) With neat sketches and necessary waveforms, explain the input and output characteristics of a BJT in CE configuration. Also derive expression for output current.

b) The reverse leakage current of the transistor when connected in CB configuration is 0.2 μA while it is 18 μA when the same transistor is connected in CE configuration. Calculate α and β of the transistor.

OR

7.a) With the help of a neat diagram explain different current components in an NPN bipolar junction transistor.

b) With reference to bipolar junction transistors, define the following terms and explain.

i) Emitter efficiency.

ii) Base Transportation factor.

iii) Large signal

8.a) Explain how ICO variations are compensated with the help of diode and thermistor in transistor biasing circuits?

b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ= 8V, ICQ= 4 mA & β= 50.

OR

9.a) Explain the basic requirements of transistor biasing. Verify these requirements in Emitter feedback bias circuit.

b) An NPN Silicon transistor with β=50 is used in a common emitter circuit with VCC=10V, RC=2K. The bias is obtained by connecting a 100K resistance from collector to base. Find i) Q-Point ii) Stability factor, S

10.a) Explain the construction & operation of an P-channel enhancement and depletion MOSFET with the help of static drain characteristics and transfer characteristics.

b) Explain why field effect transistor is called as unipolar and voltage controlled device

OR

11.a) With neat sketches, necessary equations explain the drain & transfercharacteristics of MOSFET in enhancement mode.

b) Why is a Field Effect Transistor called unipolar & voltage controlled device? Explain the drain &transfer characteristics of a JFET in detail.

PREVIOUS QUESTION PAPERS

Code No. D- 2359/N/AICTE

FACULTY OF ENGINEERING

B.E. (ECE) III - Semester (AICTE) (Main) Examination, March / April 2022

Subject: ELECTRONIC DEVICES

Time: 3 Hours

Max. Marks: 70

Note: (i) First question is compulsory and answer any four questions from the remaining six questions. Each Questions carries 14 Marks.

(ii) Answer to each question must be written at one place only and in the same order as they occur in the question paper.

(iii) Missing data, if any, may be suitably assumed.

1. (a) Explain about the energy bands in intrinsic and extrinsic Silicon
   (b) Compare Half wave rectifier, Full wave rectifier and Bridge rectifier
   (c) Define thermal runaway in transistor amplifier circuit
   (d) Draw the equivalent h- model for CB Configuration
   (e) An N-channel JFET has Idss = 10mA and V_P = - 4V. Determine the minimum value of V_{DS} and Drain current I_D? V_{GS} = - 2V in pinch-off region
   (f) Differentiate between exact and approximate model of a transistor at low frequencies
   (g) Draw the Low frequency small signal model of CS, CD and CG amplifiers.

2. (a) Draw the Energy band diagram of the PN junction diode and with the help of neat diagram explain its working under forward and reverse bias.
   (b) Explain Zener diode as voltage regulator and its limitation.

3. (a) Draw and explain the working of Full wave rectifier with L-section filter and derive its Ripple factor.
   (b) Explain the construction and working of Solar cell. What are its merit's?

4. (a) With the neat sketch explain input and output characteristics of CE configuration and derive its collector current equation.
   (b) For the self bias circuit R_1 = 20KΩ, R_2 = 60KΩ, R_C = 2KΩ, R_E = 1KΩ calculate Q point and Stability factor for beta = 100.

5. (a) Explain the High frequency - Π model of CE amplifier and derive A_I, A_V, R_I and R_O
   (b) For CE amplifier circuit V_{CC} = 20V, R_S = 900Ω, R_1 = 60KΩ, R_2 = 3KΩ, R_C = 5KΩ, R_L = 1.1KΩ h_{ie} = 1KΩ, h_{re} = $2x10^{-4}$, h_{fe} = 50, h_{oe} = 25μA/V Compute A_I, A_V, R_I and R_O using approximate analysis.

6. (a) Explain the construction and working of N- channel Enhance MOSFET with Drain and transfer characteristics.
   (b) A JFET amplifier with voltage divider biasing circuit has the parameter V_P = 2V, I_{DSS} = 4mA, R_D = 900Ω, V_{DD} = 24V, R_S = 2KΩ, R_2 = 8.57mΩ. Find the value of drain current I_D at the operating point.

7. (a) Explain the Bias Stabilizing techniques
   (b) Why bridge rectifier is preferred over center tapped rectifier

Code No. D- 2359/N/AICTE

FACULTY OF ENGINEERING

B.E. (ECE) III - Semester (AICTE) (Main) Examination, March / April 2022

Subject: ELECTRONIC DEVICES

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(e) An N-channel JFET has I_{DSS} = 10mA and V_P = - 4V Determine the minimum value of V_{DS} and Drain current I_D? V_{GS} = - 2V in pinch-off region

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3. (a) Draw and explain the working of Full wave rectifier with L-section filter and derive its Ripple factor.

(b) Explain the construction and working of Solar cell. What are its merit's?

4. (a) With the neat sketch explain input and output characteristics of CE configuration and derive its collector current equation.

(b) For the self bias circuit R_1 = 20KΩ, R_2 = 80KΩ, R_C = 2KΩ, R_E = 1KΩ calculate Q point and Stability factor for beta = 100.

5. (a) Explain the High frequency - Π model of CE amplifier and derive A_I, A_V, R_I and R_O.

(b) For CE amplifier circuit V_{CC} = 20V, R_S = 900Ω, R_1 = 60KΩ, R_2 = 3KΩ, R_C = 5KΩ, R_L = 1.1KΩ h_{ie} = 1KΩ, h_{re} = $2x10^{-4}$, h_{fe} = 50, h_{oe} = 25μA/V Compute A_I, A_V, R_I and R_O using approximate analysis.

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7. (a) Explain the Bias Stabilizing techniques

(b) Why bridge rectifier is preferred over center tapped rectifier

**

Code No.PC301EC

PART-B

Answer Any Five questions

Q.No.		Questions	Marks	CO	BTL
2.	a	Explain the current components of p-n junction diode and deduce the expression for the current in a diode due to a voltage applied?	5	1	4
	b	The voltage across a silicon diode at room temperature of 300°K is 0.7V when 2mA current flows through it. If the voltage increases to 0.77V, calculate the diode current. Assume V_T=26mV	3		
3.	a	Explain the operation of the half wave rectifier with necessary diagrams and waveforms?	4	2	4
	b	A sinusoidal voltage of 40V and frequency 50Hz is applied to a half wave rectifier, R_L=200ohm,Vγ=0,R_f=20ohm Find Vdc , Idc, Imax , Irms, Pdc, ripple factor ,η?	4		
4.	a	Explain operation of common base configuration of BJT to obtain input and output characteristics?	5	3	2
	b	What is thermal runaway in BJT? How can it be addressed?	3		
5.		Draw the circuit diagram of CE amplifier with emitter resistance and derive the expression for AI, AV, Ri and Ro using hybrid model.	8	4	4
6.	a	Define various FET parameters and obtain the relationship between them?	3	5	3
	b	Explain the operation of a MOSFET in enhancement mode?	5		
7.	a	Compare Zener and avalanche breakdowns?	4	1	4
	b	Explain the operation of the full wave rectifier with necessary diagrams and waveforms?	4	2	4
8.	a	Draw the circuit of self -biased CE amplifier using diode compensation for V_{BE}. Describe how bias compensation is achieved.	5	3	4
	b	Draw small signal h-parameter model for CB configuration.	3	4	2
9.	a	Compare BJT versus JFET?	4	5	4
	b	Compare Half wave, Full wave and bridge rectifiers.	4	1	2

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KEY PAPER

METHODIST COLLEGE OF ENGG & TECH (AUTONOMOUS)

Code No: PC301EC B.E (EEE) III - Semester (AICTE)(Regular) Exam Feb-23

Sub:- "ELECTRONIC DEVICES" (Key paper) ①

S.No

1

1 a) The Voltage at which the forward diode Current begins to start increasing rapidly is known as the cut-in voltage

Germanium diodes have cut-in voltage around 0.3V

1 b) From Diode Current eq'n $I_d = I_s [e^{V_d/\eta V_T} - 1]$

where $I_s = 1\mu A$, $V_T = 26mV$ at room temp

& $V_d = 200mV$. $\eta = 1$

$\therefore I_d = 10^{-6} [e^{200\times10^{-3}/1\times26\times10^{-3}} - 1] = 2.19mA$

$\therefore$ dc Resistance is $200/2.19 = 91.32\ \Omega$

1 c) Ripple factor:- It is defined as the R.M.S value of a.c. Component to the d.c. Component in the output is known as "Ripple factor".

for full wave $\Gamma = \frac{V_{ac}}{V_{dc}} = 0.483$

Efficiency:-(η) It is the ratio of d.c. Output power to the ac. input power. It Signifies, how efficiently the rectifier Circuit Converts a.c. power into d.c. power $\eta = \frac{\text{o/p power}}{\text{I/p power}} = \frac{P_{dc}}{P_{ac}} \times 100\% = 81.2\%$ (for full wave)

Peak Inverse Voltage (PIV):- It is defined as the maximum reverse voltage that a diode can with stand with out destroying the junction.

for full wave it is $2V_m$

1 d) * In Bridge type two extra diodes are used when Compared to Centertap

* Two diodes in Series Conduct at a time one alternate half-Cycles. This Creates a problem when low Dc voltages are Required this leads to poor voltage regulation

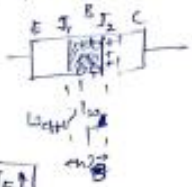
* Internal Resistance Voltage drop is twice than that of the Centertap ckt

1a

e) **Thermal Runaway:-** The problems with increasing temperature causing increasing Collector current is that more current increases its temperature this Self-reinforcing cycle is known as "thermal runaway which may destroy Transistor

$\uparrow I_C = \beta I_B + (1+\beta) I_{CBO} \uparrow$

Early effect:- The variation in the effective width of the base in a BJT due to a variation in applied base-to-collector voltage



$W_B = W_{eff} + W$

$\Rightarrow W_{eff} = W_B - W$

as $V_{CB} \uparrow \Rightarrow W \uparrow \Rightarrow W_{eff} \downarrow \Rightarrow I_E \uparrow$

$\Rightarrow V_{CB} \uparrow \Rightarrow I_E \uparrow$

1 f)

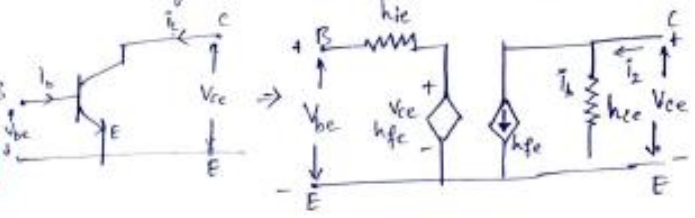
BJT	FET
* Low input Impedance	* High Input Impedance
* High output Impedance	* Low Output Impedance
* Bipolar device	* Unipolar device
* Noise is more	* less noise
* Gain is more	* less gain
* Current controlled device	* Voltage Control device

BJT amplifier is basically a BJT operated in active region. It increases the strength of the input signal and produces an amplified output

1g)

$V_{be} = h_{ie} i_b + h_{re} V_c$

$i_e = h_{fe} i_b + h_{oe} V_c$



1 h) Graphical representation of h-parameters are obtained from the static characteristic curve

1 i) FET Transistors are also called Unipolar transistor/device since they undergo the operation of a Single-carrier type i.e. either holes or electrons

1 j)
- MOSFETs have much higher input impedance compare to JFET
- They have high drain resistance due to lower resistance of channel
- They are easy to manufacture
- They support high speed of operation compare to JFETs

2) a) After Derivation of Diode Current equation

$$I_D = I_0\left[e^{V_D/\eta V_T} - 1\right]$$ where $V_T = kT/q$

V_D – diode terminal voltage
I_0 – temperature dependent Saturation Current, μA
T – absolute temperature of pn Jn, K
k – Boltzmann's Constant 1.38×10^{-23} J/K
q – electron charge 1.6×10^{-19} C
η – Empirical Constant 1 for Ge and 2 for Si

b) Sol:-

~~$I_D = 2\times10^{-3}[e$~~

$$I_D = I_0\left[e^{V/\eta V_T} - 1\right]$$

$V_T = \frac{kT}{q}$ at $T = 302K$ $V_T = 25.27mV$

$\eta = 1$ for Si

at $V_1 = 0.7V$, $I_D = 2.5mA$

If $V_2 = 0.77V$, $I_D' = ?$

$$\frac{I_d'}{I_d} = \frac{I_0}{I_0}\left[\frac{e^{V_2/\eta V_T} - 1}{e^{V_1/\eta V_T} - 1}\right]$$

$$\frac{I_d'}{I_d} = e^{\frac{1}{\eta V_T}\left[e^{V_2 - V_1}\right]}$$

$$\frac{I_d'}{I_d} = e^{\frac{1}{1\times25.27mV}[0.77 - 0.7]}$$

$$\frac{I_d'}{I_d} = e^{\frac{0.07}{25.27mV}}$$

$$\Rightarrow \boxed{I_d' = 2mA\ e^{\frac{0.07}{25.27mV}}}$$

3) a) Half wave Rectifier :-

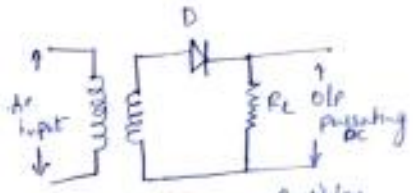
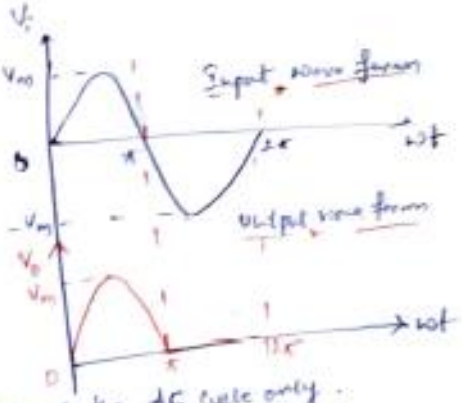


fig:- Half wave Rectifier



It converts an AC voltage into a pulsating DC voltage using only one half of the AC cycle only.
*The diode conducts during one half of Ac cycle only

Voltage to primary $V_i = V_m \sin \omega t$, $V_m \gg V_\gamma$ (cut in voltage)
of transformer

for +ve cycle 'D' is ON o/p is V_m at R_L
for -ve cycle 'D' is OFF o/p is 0 at R_L

b) Sinusoidal voltage $V_m = 40V$, freq = 50Hz, $R_L = 200\Omega$, $V_\gamma = 0$
$R_f = 20\Omega$, $V_{dc} = ?$, $I_{dc} = ?$ $I_{max} = ?$, $I_{rms} = ?$, $P_{dc} = ?$
& $P_{ac} = ?$, $\eta = ?$ $\frac{V_m}{\sqrt{2}} = 40 \Rightarrow V_m = 40 \times \sqrt{2} = 56.56$

$I_m = \frac{V_m}{(R_f + R_L)} = \frac{40\sqrt{2}}{200+20} = \frac{40\sqrt{2}}{220} = \frac{56.56}{220} = 0.257A$

$I_{dc} = \frac{I_m}{\pi} = \frac{0.257}{\pi} = 0.0818A$

$V_{dc} = I_{dc} \times R_L = 0.0818 \times 200 = 16.2V$

$I_{rms} = R.f \times I_{dc}$ or $\sqrt{I_{rms}}$

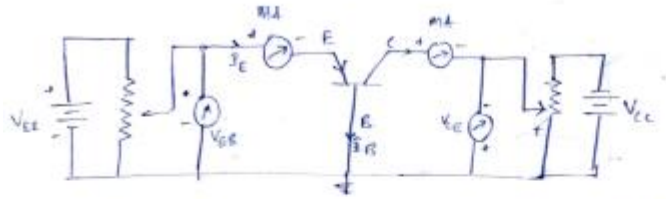
$I_{rms} = \frac{I_m}{2} = \frac{0.257}{2} = 0.1285A$

$P_{dc} = I_{dc}^2 \cdot R_L = (0.0818)^2 \times 200 =$

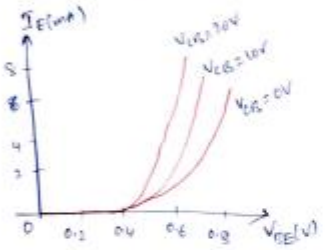
$P_{ac} = I_{rms}^2 (R_L + R_f) =$

$\eta = \frac{P_{dc}}{P_{ac}} \times 100$

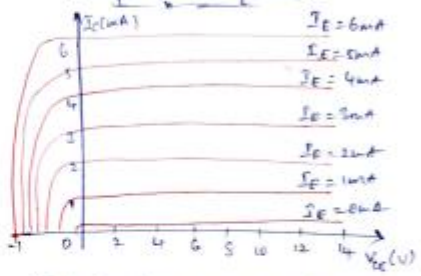
4) a) Common Base Configuration of BJT :-



Input characteristics



Output characteristics



To determine the input characteristics the collector base voltage V_{CB} is kept constant at 0 Volt & the emitter current is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}

To determine the output characteristics the input current I_E is kept constant and the V_{CB} is increased from 0 volt and the o/p current I_C is taken from the characteristics it is seen that for a constant value of I_E I_C is independent of V_{CB} & curves are parallel to the axis of V_{CB} further I_C flows even when $V_{CB}=0$

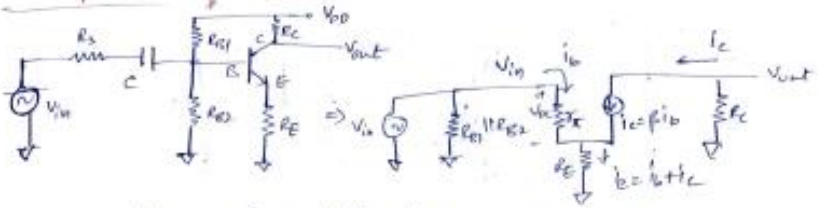
b) Thermal Runaway :- ~~Reverse Biasing~~ I(c)

$I_C = \beta I_B + (1+\beta) I_{CBO}$

I_{CBO} depends upon temperature and it produces heat in the transistor as Temp↑ → I_C ↑ → ↑T → This cumulative process may damage BJT.

→ The transistor is protected by thermal run away if its operating point makes stable by keeping collector current constant

5) CE amplifier with emitter Resistance:-



$V_{out} = -i_c R_c = -\beta i_b R_c$ | $V_{in} - i_b r_\pi - (i_b + i_c) R_E = 0$

$V_{out} = -\beta R_c \cdot \frac{V_{in}}{r_\pi + (1+\beta) R_E}$ $\Rightarrow i_b = \frac{V_{in}}{r_\pi + (1+\beta) R_E}$ — (1)

$\therefore A_v = \frac{V_{out}}{V_{in}} = -\frac{\beta R_c}{r_\pi + (1+\beta) R_E} = -\frac{\beta R_c}{\beta R_E}$ when $\beta \gg 1$, $r_\pi \ll (1+\beta) R_E$

$A_V = -\frac{R_c}{R_E}$; $A_I = \frac{I_c R_c}{V_T}$

6) a) FET parameters & Relation:-

* Transconductance:- $g_m = \frac{\delta I_D}{\delta V_{GS}}$ at constant V_{DS}

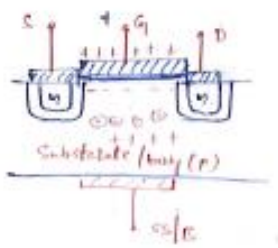
~~Drain current~~ I_D =

* Dynamic Resistance:- $r_d = \frac{\delta V_{DS}}{\delta I_D}$ at constant V_{GS}
* Amplification factor:- $\mu = \frac{\delta V_{DS}}{\delta V_{GS}}$ at constant I_D

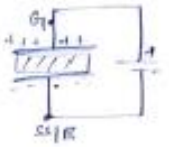
Relation between them

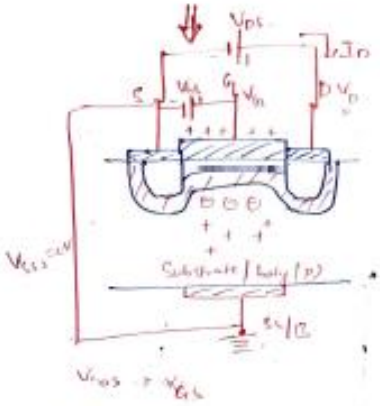
$\mu = \frac{\delta V_{DS}}{\delta V_{GS}} = \frac{\delta V_{DS}}{\delta I_D} \times \frac{\delta I_D}{\delta V_{GS}} \Rightarrow \boxed{\mu = r_d \times g_m}$

6) b) Construction & working of Enhancement-type MOSFET



maj. c.c = holes
min. c.c = e
mobile c.c = Immobile ions





$V_{GS} > 0V \Rightarrow$ Inv. $\Rightarrow$ Con. ch.

V_{GS} ↑ $\Rightarrow$ Ch. width/depth ↑

$V_G - V_{GS} + V_{DS} = V_D$

$V_{GD} = V_G - V_D = V_{GS} - V_{DS}$

Construction:-

It includes three layer gate, drain & Source. The body of MOSFET is known as Substrate that is connected Internally to the Source

Metalic gate terminal from the Semiconductor layer is insulated through a Sicicondioxide layer otherwise a dielectric layer

working:- Once the gate(G_1) is +ve then it attracts minority charge carriers like Electrons from P-substrate where these charge carriers will combine through the holes under the layer of SiO_2. Further V_{GS} is increased then the electrons will have enough potential to overcome and bonding and more charge carriers $\bar{e}$ gets deposited in the channel here dielectric is used to prevent the electrons movements across the SiO_2 the accumulation will result n-channel formation b/w Drain & Source this leads to I_D proportional to Channel Resistance

7) a)

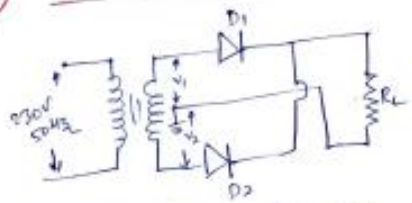
Zener Breakdown

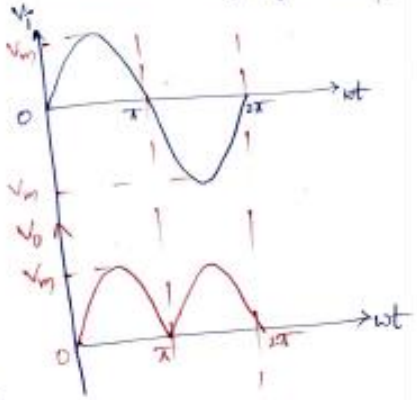
* Breaking of covalent bonds is due to intense electric field across the narrow depletion region. This generates large numbers of free electrons to cause breakdown
* This occurs for Zener diodes with $V_{BR} < 6V$
* The temperature co-efficient is -ve
* The breakdown voltage decreases as junction temperature increases
* Occurs in highly doped diodes

Avalanche Breakdown

* Breaking of covalent bonds is due to collision of accelerated charge carriers having large velocity & kinetic energy with adjacent atoms is called carrier multiplication.
* This occurs for Zener diodes with $V_{BR} > 6V$
* The temperature coefficient is +ve
* The breakdown voltage increases as junction temperature increases
* Occurs in lightly doped diodes

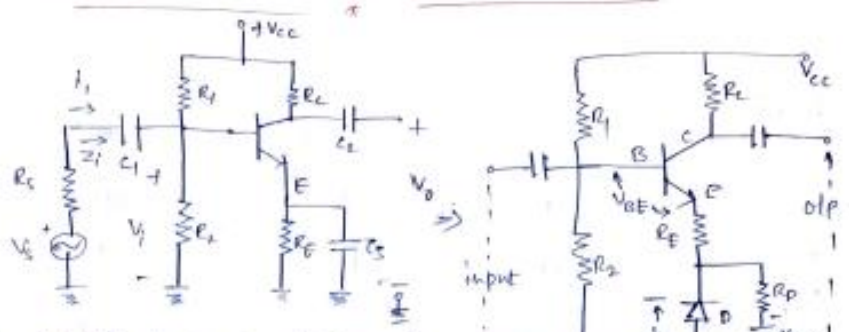
7 b) **Full wave Rectifier:-**





* It uses two diodes of which one conducts during one-half cycle while the other diode conducts during other half cycle of applied voltage
* During +ve half cycle 'D_1' is ON & 'D_2' is OFF
  During -ve half cycle 'D_1' is OFF & 'D_2' is ON
  for both condition the load current flows and drop across R_L will be Input voltage

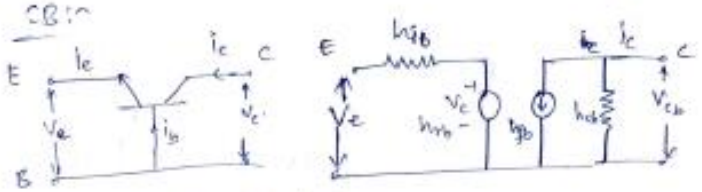
8) a) Common Emitter Self biased transistor amplifier



A diode can be employed in the emitter ckt in order to compensate the variations in V_{BE} or I_{CO}. As the diode and transistor used are of same material, the voltage V_D across the diode has same temperature coefficient as V_{BE} of the transistor

fig:- CE self biased diode compensation

b) CB:-



$V_e = h_{ib} i_e + h_{rb} V_c$

$i_c = h_{fb} i_e + h_{ob} V_c$

9) a)

BJT	FET
1) Current Control device	1) Voltage Controlled device
2) Bipolar device	2) Unipolar device
3) n-p-n & p-n-p	3) n-channel & p-channel
4) CE, CB, CC Configurations	4) CG, CS, CD Configurations
5) I/p resistance is less compared to FET	5) I/p resistance is high
6) Thermal runaway exists	6) No thermal run away

9) b) Comparison of Rectifiers

Particulars	Half wave	Full wave	Bridge wave
1) No. of diodes →	1	2	4
2) Maximum Efficiency →	40.6	81.2	81.2
3) V_{dc} (Max. load) ⇒	V_m/π	$2V_m/\pi$	$2V_m/\pi$
4) Average current for diode →	I_m/π	$2I_m/\pi$	$2I_m/\pi$
5) Ripple factor →	1.21	0.482	0.482
6) PIV →	V_m	$2V_m$	V_m
7) TUF →	0.287	0.693	0.821
8) form factor ⇒	1.57	1.11	1.11
9) Peak factor →	2	1.414	1.414

ELECTRONIC DEVICS EXTERNAL EXAM RESULTS (B)

Course Name with Code	Electronic Devices(5PC301EC)
Class	B.E III Sem ECE (B)
Faculty Name	Mr I.Poorna chander
Type of Exam	Semester Exam 2022-23 SEM III

S. No.	Roll No.	Name of the student	Ext Grades	Credits
1	160721735062	MOLUGURU PALLAVI	B	3
2	160721735063	POTHULA SAI KRISHNA	D	3
3	160721735064	NUNE VINOD	C	3
4	160721735065	TIRUMALA KARTHIKEYA	C	3
5	160721735067	PATNAIKUNI VENKATA SAI ANIL PATNAIK	A	3
6	160721735068	RAMAVATH BHANU	C	3
7	160721735069	RACHAMALLU VARUN KUMAR REDDY	B	3
8	160721735070	RATHOD PARASHURAM	C	3
9	160721735071	SAAD KHAN	E	3
10	160721735072	GOPARAJU SAI MADHAV	B	3
11	160721735074	SHAIK SOHAIL	F	0
12	160721735075	SHAIK ABUBAKAR SIDDIK	D	3
13	160721735076	SHERLA SAI VARDHAN	B	3
14	160721735077	SOBIA NAAZ	D	3
15	160721735078	MD FURQUAN NAWAZ	E	3
16	160721735079	SOMAROWTHU SAI BHASKAR	C	3
17	160721735080	SR PREM KUMAR	E	3
18	160721735081	PENUEL ZECHARAIAH JAMES	E	3
19	160721735082	SYED IMAMUDDIN	C	3
20	160721735083	TELLABOINA RAJESH	D	3
21	160721735084	K ANIL KUMAR	D	3
22	160721735085	TERALA VIGNESH	A	3
23	160721735086	SUNNY T	E	3
24	160721735087	MUNIGALA SATHWIK	F	0
25	160721735088	THATOJU ABHISHEK	E	3
26	160721735089	UNNI KISHORE	B	3
27	160721735090	CHENUMALLA KOUSHIK	E	3
28	160721735091	VERTHE SURESH NAIK	D	3
29	160721735092	VODNALA NITHIN	D	3

30	160721735093	GARLAPALLI SAI RAJITHA	D	3
31	160721735094	VARAGANTIPAVANKUMAR	F	0
32	160721735096	RAVISHWAS GOUD	F	0
33	160721735301	BHAVANA GUNDLAPALLY	B	3
34	160721735302	YADA AKSHAY KUMAR	C	3
35	160721735303	T NAGARAJ KOUSHIK	C	3
36	160721735304	N SAI VENKAT KUMAR REDDY	D	3
37	160721735305	KADABOINA GIRISH RAJ	E	3
38	160721735306	Y PARTHA SARADHI REDDY	C	3
39	160721735307	NANDURI NAGASAI	D	3
40	160721735308	PUJALA SAI CHETAN	C	3
41	160721735309	MD SOFT SAMEER	D	3
42	160721735310	IBRAHIM SHAIKH	D	3
43	160721735311	CHOUTAKUR KEERTHANA	D	3
44	160721735312	P VAKYASRI	C	3
45	160721735313	GUDURU MANISH	E	3
46	160721735314	L SRI VIHAAN CHANDRA	C	3
47	160721735315	P THIRUPATHI REDDY	C	3
48	160721735316	P SACHIN	C	3
49	160721735317	P VIVEK GOUD	D	3
50	160721735318	N SRIKANTH	C	3
51	160721735319	ABDUL GHAFOOR MD SIDDIQI	F	0
52	160721735320	D PRASHANTH	C	3
53	160721735321	GOVULA SRI SOWMYA	C	3
54	160721735322	ERUKONDA TRISHA	B	3
55	160721735323	KASIREDDY KOMAL PRANAV	D	3
56	160721735324	MEGAVATH MALLESH	C	3
57	160721735325	N SHIVA RAM PRASAD	C	3
58	160721735326	KOLLURU VIDYADHAR	D	3
59	160721735327	ANNEBOINA PRAKASH	D	3
60	160721735328	PERUGU UDAY KIRAN	D	3
61	160721735329	MARLA SHIVAJI GOUD	C	3
62	160721735330	VARSHA JYOTHIKA	D	3
63	160721735331	M NITHIN RAJ	C	3

SUBJECT NAME	CLASS /SECTION	S	A	B	C	D	E	F	TOTAL
ELECTRONIC DEVICES	**III B**	**0**	**2**	**7**	**21**	**19**	**9**	**5**	**63**

EXTERNAL EXAM ATTAINMENTS

University Examination	
Maximum External Marks	S
Satisfactory Set Grade	D
No. of students who attained Set Grade& above	49
No. of students attempted	63
% Students attained the Set Grade& above	77.78
CO Attainment	
CO 1	77.78
CO 2	77.78
CO 3	77.78
CO 4	77.78
CO 5	77.78
CO 6	77.78

FACULTY: I.POORNA CHANDER
ASSISTANT PROF.
ECE DEPARTMENT,

9963390390, ipurnachander@methodist.edu.in

SEMESTER QUESTION PAPER ANALYSIS

Course Name with Code	Electronic Devices(5PC301EC)
Class	B.E III Sem ECE (B)
Faculty Name	Mr I Poorna Chander
Type of Exam	Semester Exam 2022-23 SEM III

Question Number	Maximum Marks of Question	CO Number	BLL
1a	2	CO1	Remembering
b	2		Remembering
c	2	CO2	Remembering
d	2		Understanding
e	2	CO3	Remembering
f	2		Understanding
g	2	CO4	Understanding
h	2		Remembering
i	2	CO5	Understanding
j	2		Understanding
2) a	5	CO1	Understanding
b	3		Understanding
3) a	4	CO2	Analysing
b	4		Analysing
4)a	5	CO3	Understanding
b	3		Remembering
5	8	CO4	Evaluating
6) a	3	CO6	Understanding
b	5	CO5	Understanding
7) a	4	CO1	Remembering

b	4	CO2	Remembering
8) a	5	CO3	Remembering
b	3	CO4	Remembering
9) a	4	CO5	Remembering
b	4	CO1	Understanding

Taxonomy	Marks	%Marks
Remembering	33	39.29%
Understanding	35	41.67%
Analysing	8	9.52%
Applying	-	-
Evaluating	8	9.52%
Creating	-	-
Total	**84**	100.00%

CO No.	Marks	%Marks
CO1	20	23.81%
CO2	16	19.05%
CO3	17	20.24%
CO4	15	17.86%
CO5	13	15.48%
CO6	3	3.57%
Total	**84**	100.00%

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OVER ALL ATTAINMENTS

Course Name with Code	Electronic Devices(5PC301EC)
Class	B.E III Sem ECE (B)
Faculty Name	Mr. I.Poorna Chander
Type of Exam	Semester Exam 2022-23, III - SEM

CO No.	Course Outcomes	Average CO Attainment
5PC301EC.1	The concepts of semiconductor devices like PN junction diode, Transistor, and special diodes.	**2.6**
5PC301EC.2	The applications of diodes.	**2.51**
5PC301EC.3	To familiarize the students with various two terminal and three terminal electronic devices working and use in the design of real time electronic products.	**2.56**
5PC301EC.4	Design DC biasing techniques and evaluate A.C parameters for BJT in Amplifier	**2.53**
5PC301EC.5	Explore V-I characteristics of FETs, MOSFETs and study IC fabrication techniques	**2.51**
5PC301EC.6	Analysis of Small signal model analysis for FET	**2.51**
	Overall Course Attainment(Indirect)	**2.54**

CO Attainment	Internal I	Internal II	University Examination	Overall Direct (%)	Overall Direct (Rubric)	Overall Indirect (Rubric)	Overall CO Attainment
CO 1	**78.26**		77.778	78.02	3	2.6	2.92
CO 2	**69.74**		77.778	73.76	3	2.51	2.902
CO 3		**56.08**	77.778	66.93	3	2.56	2.912
CO 4		**79.84**	77.778	78.81	3	2.53	2.906
CO 5		**78.81**	77.778	78.30	3	2.51	2.902
CO 6		**75.78**	77.778	76.78	3	2.51	2.902
Overall Course Attainment					**3.00**	**2.54**	**2.91**
Set Target for the course					1.96	1.96	1.96
Course Attainment Status(Yes/No)					**Yes**	**Yes**	**Yes**

CO Percentage score	CO attainment rubric
%CO ≥ 60	3
50 <=%CO <60	2
%CO< 50	1

METHODIST
COLLEGE OF ENGINEERING & TECHNOLOGY
(An Autonomous Institution)
Approved by AICTE, New Delhi & Affiliated to Osmania University
Accredited by NBA and NAAC with A+ Grade
Estd : 2008

PO ATTAINMENT

Course Name with Code	Electronic Devices(5PC301EC)
Class	B.E III Sem ECE (B)
Faculty Name	Mr I.Poorna Chander
Type of Exam	Semester Exam 2022-23 SEM III

PO / CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PS01	PSO2	PSO3
5PC301EC.1	3	3	2					1	1	1			3	2	
5PC301EC.2	3	2	1	2	2			1	1	1			3	2	
5PC301EC.3	3	2	1	2	3			1	1	1			3	2	
5PC301EC.4	3	2	1	1	2			1	1	1			3	2	
5PC301EC.5	3	2	2	2	3			1	1	1			3	2	
5PC301EC.6	3	3	3	2	3			1	1	1			3	3	
5PC301EC	3.00	2.33	1.67	1.80	2.60			1.00	1.00	1.00			3.00	2.17	

1.96

PO / CO	CO ATTAINED	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PS01	PSO2	PSO3
5PC301EC.1	2.6	2.60	2.60	1.73					0.87	0.87	0.87			2.60	1.73	
5PC301EC.2	2.51	2.51	1.67	0.84	1.67	1.67			0.84	0.84	0.84			2.51	1.67	
5PC301EC.3	2.56	2.56	1.71	0.85	1.71	2.56			0.85	0.85	0.85			2.56	1.71	
5PC301EC.4	2.53	2.53	1.69	0.84	0.84	1.69			0.84	0.84	0.84			2.53	1.69	
5PC301EC.5	2.51	2.51	1.67	1.67	1.67	2.51			0.84	0.84	0.84			2.51	1.67	
5PC301EC.6	2.51	2.51	2.51	2.51	1.67	2.51			0.84	0.84	0.84			2.51	2.51	

FACULTY: I.POORNA CHANDER
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IMPROVEMENTS FOR COURSE ASSESSMENTS

Course Name with Code	Electronic Devices(5PC301EC)
Class	B.E III Sem ECE (B)
Faculty Name	Mr.I.Poorna Chander
Type of Exam	Semester Exam 2022-23, III - SEM

CO No.	Course Outcomes
5PC301EC.1	The concepts of semiconductor devices like PN junction diode, Transistor, and special diodes.
5PC301EC.2	The applications of diodes.
5PC301EC.3	To familiarize the students with various two terminal and three terminal electronic devices working and use in the design of real time electronic products.
5PC301EC.4	Design DC biasing techniques and evaluate A.C parameters for BJT in Amplifier
5PC301EC.5	Explore V-I characteristics of FETs, MOSFETs and study IC fabrication techniques
5PC301EC.6	Analysis of Small signal model analysis for FET

Best Performing COs	CO1,CO3,
Least Performing COs	CO2,CO5,CO6

BEST PERFORMING COURSE OUTCOME: 97.3% (CO1, CO3)
LEAST PERFORMING COURSE OUTCOME: 96.7 %(C02 , CO5 & CO6)

Observations:

1	The set target for the course is attained, due to the following Teaching Strategy. As this course was important, lots of videos, e-resources and pictorial illustrations were presented to enhance learning. Students were also made to prepare topics and prepare seminars, which helped them learn by teaching to peers.
2	The course lacks practical real life exposure and modern tools ,which could enhance learning even better

Plan of Action:

1	Arranging guest lecturers for practical real life exposure and organizing workshops for modern tools will enrich the learning levels beyond “understanding “to “evaluate levels”. These features can be added to the course.

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ELECTRONIC DEVICES QUIZ1

UNIT-1(2022-2026 BATCH)

* Indicates required question

1. Email *

Candidate Registration

2. Device *

Mark only one oval.

- Smart Phone
- Tablet
- Laptop
- Desktop

3. Mobile No *

4. Branch *

Mark only one oval.

- ECE

5. Section *

Mark only one oval.

- A
- B

6. Roll No *

_____

7. Name of the Student *

_____

Instructions to the students for Online 2nd internal examination

Before You start taking Examination :

1. Please ensure that you have smartphone/computer/laptop/tablet with proper internet facility.
2. It is recommended to use devices that have battery backup to avoid the issues of power failure.
3. A link will be sent to your Gmail ID/Class Whats app group/ Google Classroom just before the exam. by clicking that link, you can get access to the exam.

While You start taking Examination :

4. Exam can be attempted only once, so please be careful while answering and submitting the test.
5. All your answers will be LOST if you open other tab or refresh or press back button or the device shuts down.
6. You have to press SUBMIT button to successfully complete the test. Other wise it will be considered as not submitted.
7. The 1 Internal quiz examination will be in the form of 20 MCQ's Carrying 20 Marks.
8. Total allotted time is 30 Minutes (20 Minutes for the test and additional 10 minutes for filling your details, review & submission).
9. The test must be completed and submitted with in 30 Minutes.
10. The online Quiz platform will stop receiving submission at the end of the 30 minutes.

" UNIT-1" ELECTRONIC DEVICES

8. The doping level in a zener diode is …… that of a PN diode *

Mark only one oval.

- the same as above
- less than
- more than
- none of the above

9. What is the cut in voltage for silicon *

Mark only one oval.

- 0.3V
- 1V
- 0.7V
- 0.2V

10. A diode conducts when it is forward-biased, and the anode is connected to the _____ through a limiting resistor. *

Mark only one oval.

- positive supply
- negative supply
- cathode
- anode

11. *

For a forward-biased diode, the barrier potential _____ as temperature increases

Mark only one oval.

- remains constant
- increases
- decreases
- none of the above

12. Which of the following is not a physical component of an electronic circuit? *

Mark only one oval.

- Capacitor
- Inductor
- Diode
- Temperature

13. Hall effect can be used to measure *

Mark only one oval.

- Magnetic field intensity
- Electric field intensity
- Carrier concentration
- None of the above

14. The process of adding an impurity to an intrinsic semiconductor is called--------- * ---

Mark only one oval.

- Ionization
- Doping
- Recombination
- Atomic

15. *

An ideal diode presents acts as _____ when reversed-biased and _____ when forward-biased.

Mark only one oval.

- open, short
- short, open
- open, open
- short, short

16. One eV is equal to _____ J. *

Mark only one oval.

- 6.02 × 10^23
- 1.6 × 10^−19
- 6.25 × 10^18
- 1.66 × 10^−24

17. A zener diode is used as ……. *

Mark only one oval.

- an amplifier
- a rectifier
- a voltage regulator
- multivibrator

ELECTRONIC DEVICES QUIZ -2

UNITS-3,4,5

* Indicates required question

1. Email *

Skip to question 2Skip to question 2

Candidate Registration

2. Device *

Mark only one oval.

- Smart Phone
- Tablet
- Laptop
- Desktop

STUDENT DETAILS

3. Mobile No *

4. Branch *

Mark only one oval.

- ECE

5. Section *

Mark only one oval.

- A
- B

6. Roll No *

_____

7. Name of the Student *

_____

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Before You start taking Examination :

1. Please ensure that you have smartphone/computer/laptop/tablet with proper internet facility.
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While You start taking Examination :

4. Exam can be attempted only once, so please be careful while answering and submitting the test.
5. All your answers will be LOST if you open other tab or refresh or press back button or the device shuts down.
6. You have to press SUBMIT button to successfully complete the test. Other wise it will be considered as not submitted.
7. The 1 Internal quiz examination will be in the form of 20 MCQ's Carrying 20 Marks.
8. Total allotted time is 30 Minutes
9. The test must be completed and submitted with in 30 Minutes.
10. The online Quiz platform will stop receiving submission at the end of the 30 minutes.

Unit 3 questions

BJT & BIASING

8. In the saturated region, the transistor acts like a * 1 point

Mark only one oval.

- poor transistor
- amplifier
- open switch
- closed switch

9. If the emitter-base junction is forward biased and the collector-base junction is reverse biased, what will be the region of operation for a transistor? * 1 point

Mark only one oval.

- cut off region
- saturated region
- inverted region
- active region

10. The transfer of a signal in a transistor is 1 point

Mark only one oval.

- low to high resistance
- high to low resistance
- collector to base junction
- emitter to base junction

11. A transistor has an IC of 100mA and IB of 0.5mA. What is the value of αdc? * 1 point

Mark only one oval.

- 0.565
- 0.754
- 1.24
- 0.995

12. The emitter current IE in a transistor is 3mA. If the leakage current ICBO is 5μA and α=0.98, calculate the collector and base current. * 1 point

Mark only one oval.

- 3.64mA and 35μA
- 2.945mA and 55μA
- 3.64mA and 33μA
- 5.89mA and 65μA

13. The relation between α and β is * 1 point

Mark only one oval.

- β=α/(1-α)
- α= β/(1+β)
- β=α/(1+α)
- α= β/(1- β)

14. The base current amplification factor β is given by * 1 point

Mark only one oval.

- IC/IB
- IB/IC
- IE/IB
- IB/IE

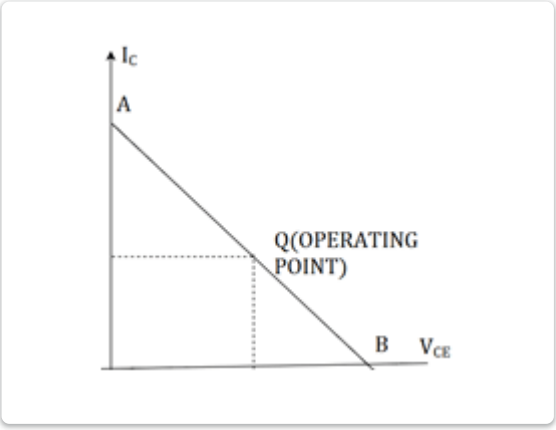
15. In ICEO, wt does the subscript ‘CEO’ mean? * 1 point

Mark only one oval.

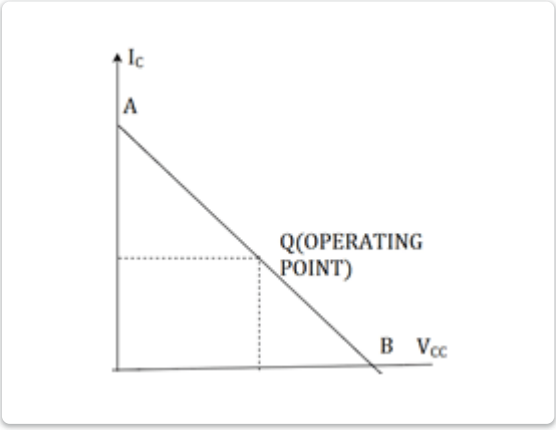
- collector to base emitter open
- emitter to base collector open
- collector to emitter base open
- emitter to collector base open

16. Which of the following depicts the DC load line? * 1 point

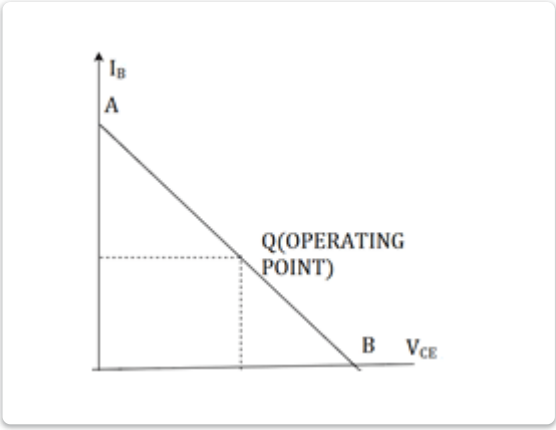
Mark only one oval.



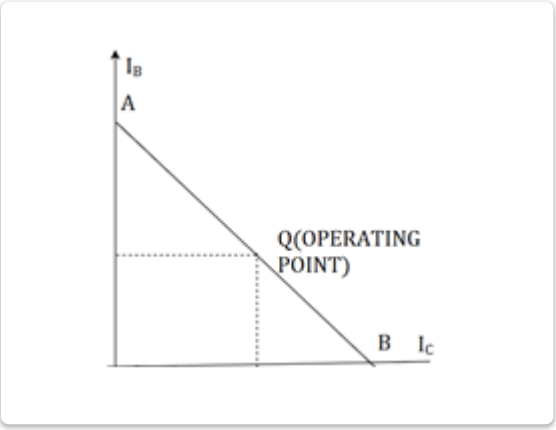
a)



b)



c)



d)

17. Which type of temperature dependent resistor exhibits a positive temperature coefficient of resistivity? * 1 point

Mark only one oval.

- Thermistor
- Sensistor
- Varistor
- Photoresistor

UNIT-4

small signal analysis -h-parameters

18. How do we determine the hybrid parameters h11 and h21of a two – port network? * 1 point

Mark only one oval.

- Short circuiting the input terminal
- Open circuiting the input terminal
- Short circuiting the output terminal
- Open circuiting the output terminal

19. In a hybrid model of a two – port network, parameter h11 is also known as? * 1 point

Mark only one oval.

- Input conductance
- Input resistance
- Output conductance
- Output resistance

20. The dimensions of hie parameters are _____ * 1 point

Mark only one oval.

- MHO
- OHM
- Farad
- Ampere

21. How many h-parameters of a transistor are dimensionless? * 1 point

Mark only one oval.

- Four
- Two
- Three
- One

22. What is the approximate hybrid parameter current gain of a CE amplifier? * 1 point

Mark only one oval.

- -hfe
- hfe
- -hfc
- hfc

23. What is the approximate hybrid parameter current gain of a CB amplifier? * 1 point

Mark only one oval.

- -hfe / 1 + hfe
- -hfe / 1 − hfe
- hfe / 1 + hfe
- hfe / 1 − hfe

24. What is the approximate hybrid parameter current gain of a CC amplifier? * 1 point

Mark only one oval.

- 1 + hoe
- 1 − hoe
- 1 + hfe
- 1 − hfe

25. What is the approximate hybrid parameter voltage gain of a CE amplifier? * 1 point

Mark only one oval.

- hfe × RL / hie
- -hfe × RL / hie
- hfe × RL / hoe
- -hfe × RL / hoe

26. Which of the following statements are correct for basic transistor configurations? * 1 point

Mark only one oval.

- CB Amplifiers has low input impedance and low current gain
- CC Amplifiers has low input impedance and high current gain
- CE Amplifiers has very poor voltage gain but very high input impedance
- The current gain of CB Amplifier is higher than the current gain of CC Amplifiers

27. Which of the following is true? * 1 point

Mark only one oval.

- CC amplifier has a large current gain
- CE amplifier has a large current gain
- CB amplifier has low voltage gain
- CC amplifier has low current gain

UNIT-5

FET'S

28. FET is a voltage controlled device. * 1 point

Mark only one oval.

- True
- False

29. For a FET when will maximum current flows? * 1 point

Mark only one oval.

- Vgs = 0V
- Vgs = 0v and Vds >= |Vp|
- VDS >= |Vp|
- Vp = 0

30. For an n-channel FET, What is the direction of current flow? * 1 point

Mark only one oval.

- Source to drain
- Drain to source
- Gate to source
- Gate to drain

31. What is pinch off voltage? * 1 point

Mark only one oval.

- The minimum voltage required to turn on the FET
- The maximum voltage a FET can withstand
- Current amplification factor/voltage gain
- The value of voltage at which the current gets pinched to zero

32. For NMOS transistor which of the following is not true? * 1 point

Mark only one oval.

- The substrate is of p-type semiconductor
- Option Inversion layer or induced channel is of n type
- Threshold voltage is negative
- None of the mentioned

33. **What does MOSFET stands for?** * 1 point

Mark only one oval.

- Metal Oxide Semiconductor Field Effect Transistor
- Modern Oxidized Silicon based Field Effect Transistor
- Modern Oxidized Silicon based Force Effect Transistor
- Metal Oxide silicon Field Equivalent Transistor

34. **MOSFET is a _____ device.** * 1 point

Mark only one oval.

- Tri-terminal
- Unipolar
- Voltage-controlled
- All as mentioned earlier

35. The constant current region of JFET lies between * 1 point

Mark only one oval.

- cut off and saturation
- cut off and pinch-off
- 0 and IDSS
- pinch-off and breakdown

36. If the reverse bias on gate of the JFET is increased,the width of the conducting channel * 1 point

Mark only one oval.

- is decreased
- is increased
- remains same
- none of the above

37. **How many terminals does the FET transistor have?** * 1 point

Mark only one oval.

- One
- Two
- Three
- Four

ELECTRONIC DEVICES QUIZ (UNIT-3)

UNIT-3(III SEM 22 BATCH STUDENTS)

* Indicates required question

1. Email *

Candidate Registration

2. Device *

Mark only one oval.

- Smart Phone
- Tablet
- Laptop
- Desktop

STUDENT DETAILS

3. Mobile No *

4. Branch *

Mark only one oval.

- ECE

5. Section *

Mark only one oval.

- A
- B

6. Roll No *

_____

7. Name of the Student *

_____

Instructions to the students for Online 2nd internal Quiz examination

Before You start taking Examination :

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While You start taking Examination :

4. Exam can be attempted only once, so please be careful while answering and submitting the test.
5. All your answers will be LOST if you open other tab or refresh or press back button or the device shuts down.
6. You have to press SUBMIT button to successfully complete the test. Other wise it will be considered as not
   submitted.
7. The 1 Internal quiz examination will be in the form of 20 MCQ's Carrying 10 Marks.
8. Total allotted time is 15 Minutes
9. The test must be completed and submitted with in 15 Minutes.
10. The online Quiz platform will stop receiving submission at the end of the 20 minutes.

Unit 3 questions

BJT & BIASING

8. In the saturated region, the transistor acts like a *

Mark only one oval.

- poor transistor
- amplifier
- open switch
- closed switch

9. If the emitter-base junction is forward biased and the collector-base junction is reverse biased, what will be the region of operation for a transistor? *

Mark only one oval.

- cut off region
- saturated region
- inverted region
- active region

10. The transfer of a signal in a transistor is

Mark only one oval.

- low to high resistance
- high to low resistance
- collector to base junction
- emitter to base junction

11. A transistor has an IC of 100mA and IB of 0.5mA. What is the value of αdc? *

Mark only one oval.

- 0.565
- 0.754
- 1.24
- 0.995

12. The emitter current IE in a transistor is 3mA. If the leakage current ICBO is 5μA and α=0.98, calculate the collector and base current. *

Mark only one oval.

- 3.64mA and 35μA
- 2.945mA and 55μA
- 3.64mA and 33μA
- 5.89mA and 65μA

13. The relation between α and β is *

Mark only one oval.

- β=α/(1-α)
- α= β/(1+β)
- β=α/(1+α)
- α= β/(1- β)

14. The base current amplification factor β is given by *

Mark only one oval.

- IC/IB
- IB/IC
- IE/IB
- IB/IE

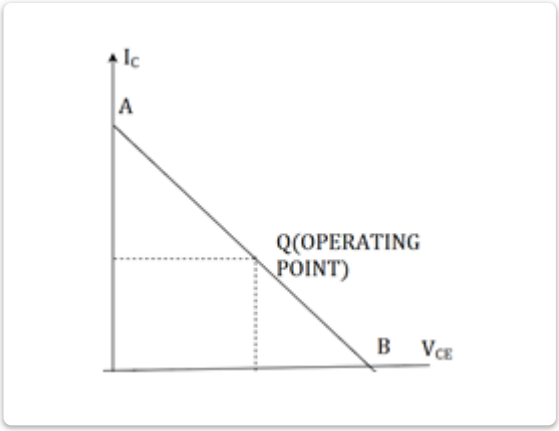
15. In ICEO, wt does the subscript 'CEO' mean? *

Mark only one oval.

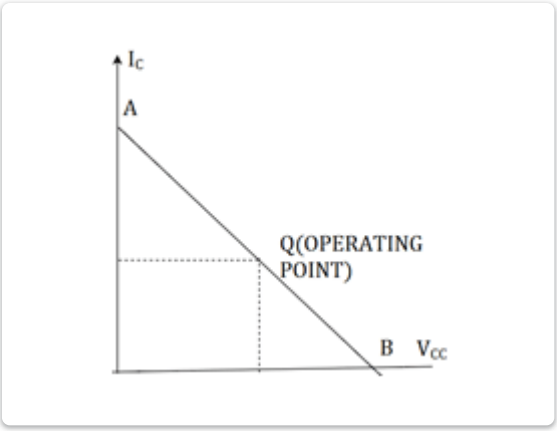
- collector to base emitter open
- emitter to base collector open
- collector to emitter base open
- emitter to collector base open

16. Which of the following depicts the DC load line? *

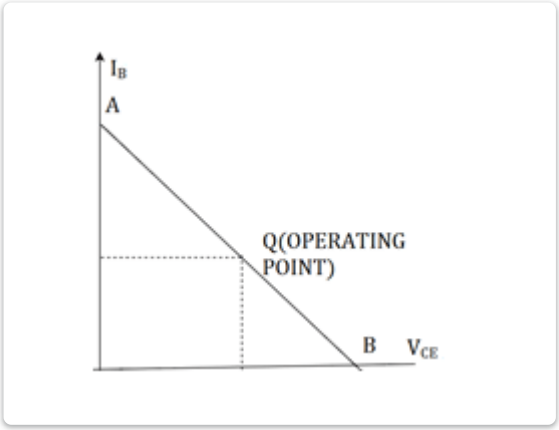
Mark only one oval.



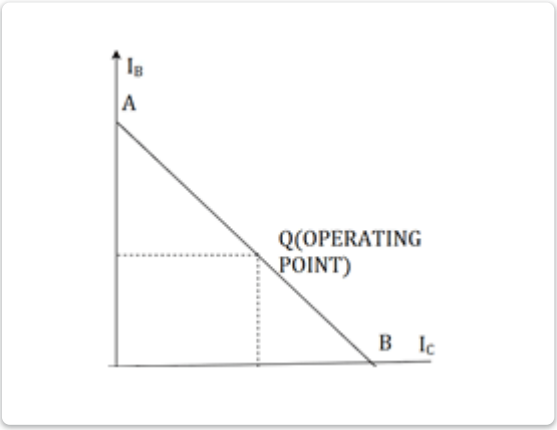
a)



b)



c)



d)

17. Which type of temperature dependent resistor exhibits a positive temperature coefficient of resistivity? *

Mark only one oval.

- Thermistor
- Sensistor
- Varistor
- Photoresistor

ELECTRONIC DEVICES QUIZ(UNIT-4)

III SEM ECE BATCH-22

* Indicates required question

1. Email *

Candidate Registration

2. Device *

Mark only one oval.

- Smart Phone
- Tablet
- Laptop
- Desktop

STUDENT DETAILS

3. Mobile No *

4. Branch *

Mark only one oval.

- ECE

5. Section *

Mark only one oval.

- A
- B

6. Roll No *

_____

7. Name of the Student *

_____

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   submitted.
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8. Total allotted time is 15 Minutes
9. The test must be completed and submitted with in 15 Minutes.
10. The online Quiz platform will stop receiving submission at the end of the 20 minutes.

UNIT-4

small signal analysis -h-parameters

8. How do we determine the hybrid parameters h11 and h21of a two – port network? *

Mark only one oval.

- ◯ Short circuiting the input terminal
- ◯ Open circuiting the input terminal
- ◯ Short circuiting the output terminal
- ◯ Open circuiting the output terminal

9. In a hybrid model of a two – port network, parameter h11 is also known as? *

Mark only one oval.

- Input conductance
- Input resistance
- Output conductance
- Output resistance

10. The dimensions of hie parameters are _____ *

Mark only one oval.

- MHO
- OHM
- Farad
- Ampere

11. How many h-parameters of a transistor are dimensionless? *

Mark only one oval.

- Four
- Two
- Three
- One

12. What is the approximate hybrid parameter current gain of a CE amplifier? *

Mark only one oval.

- -hfe
- hfe
- -hfc
- hfc

13. What is the approximate hybrid parameter current gain of a CB amplifier? *

Mark only one oval.

- -hfe / 1 + hfe
- -hfe / 1 – hfe
- hfe / 1 + hfe
- hfe / 1 – hfe

14. What is the approximate hybrid parameter current gain of a CC amplifier? *

Mark only one oval.

- 1 + hoe
- 1 – hoe
- 1 + hfe
- 1 – hfe

15. What is the approximate hybrid parameter voltage gain of a CE amplifier? *

Mark only one oval.

- hfe × RL / hie
- -hfe × RL / hie
- hfe × RL / hoe
- -hfe × RL / hoe

16. Which of the following statements are correct for basic transistor configurations? *

Mark only one oval.

- CB Amplifiers has low input impedance and low current gain
- CC Amplifiers has low input impedance and high current gain
- CE Amplifiers has very poor voltage gain but very high input impedance
- The current gain of CB Amplifier is higher than the current gain of CC Amplifiers

17. Which of the following is true? *

Mark only one oval.

- CC amplifier has a large current gain
- CE amplifier has a large current gain
- CB amplifier has low voltage gain
- CC amplifier has low current gain

ELECTRONIC DEVICES QUIZ(UNIT-5)

III SEM ECE BATCH-22

* Indicates required question

1. Email *

Candidate Registration

2. Device *

Mark only one oval.

- Smart Phone
- Tablet
- Laptop
- Desktop

STUDENT DETAILS

3. Mobile No *

4. Branch *

Mark only one oval.

- ECE

5. Section *

Mark only one oval.

- A
- B

6. Roll No *

_____

7. Name of the Student *

_____

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9. The test must be completed and submitted with in 30 Minutes.
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UNIT-5

FET'S

8. FET is a voltage controlled device. *

Mark only one oval.

- ◯ True
- ◯ False

9. For a FET when will maximum current flows? *

Mark only one oval.

- Vgs = 0V
- Vgs = 0v and Vds >= |Vp|
- VDS >= |Vp|
- Vp = 0

10. For an n-channel FET, What is the direction of current flow? *

Mark only one oval.

- Source to drain
- Drain to source
- Gate to source
- Gate to drain

11. What is pinch off voltage? *

Mark only one oval.

- The minimum voltage required to turn on the FET
- The maximum voltage a FET can withstand
- Current amplification factor/voltage gain
- The value of voltage at which the current gets pinched to zero

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Mark only one oval.

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- Threshold voltage is negative
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13. **What does MOSFET stands for?** *

Mark only one oval.

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- Metal Oxide silicon Field Equivalent Transistor

14. **MOSFET is a _____ device.** *

Mark only one oval.

- Tri-terminal
- Unipolar
- Voltage-controlled
- All as mentioned earlier

15. The constant current region of JFET lies between *

Mark only one oval.

- cut off and saturation
- cut off and pinch-off
- 0 and IDSS
- pinch-off and breakdown

16. If the reverse bias on gate of the JFET is increased,the width of the conducting channel *

Mark only one oval.

- is decreased
- is increased
- remains same
- none of the above

17. **How many terminals does the FET transistor have?** *

Mark only one oval.

- One
- Two
- Three
- Four