**UNIT-V SHORT QUESTIONS**

**1.**           **What are the advantages of static RAM and Dynamic Ram?**

**Static RAM:**

              Access time is less.

              Fast operation.

**Dynamic Ram**

              It consumes less power.

              Cost is low.

**2.**           **What is difference between PAL and PLA?**

PLA:

* Both AND and OR arrays are programmable and Complex
* Costlier than PAL



PAL:

* AND arrays are programmable OR arrays are fixed
* Cheaper and Simpler

**.**           **Compare Dynamic RAM with Static RAM.**

              Static Ram is very costly.

              Dynamic Ram is cheaper.

              Static Ram contains Transistors.

              Dynamic Ram contains Capacitors.

              Static Ram is used in L1 and L2 cache.

              Dynamic Ram is used in system RAM.

**4.**           **What is meant by memory Expansion? Mention its limit.**

The memory expansion can be achieved in two ways: by expanding word size and expanding memory capacity.

**Limitations:**

* Memory capacity upto 16Mbytes.
* 24 address lines and 16 data lines.

**5.**           **Mention few applications of PLA and PAL.**

              Implement combinational circuits

              Implement sequential circuits

              Code converters

              Microprocessor based systems

**6.**           **What are the different types of programmable logic devices?**

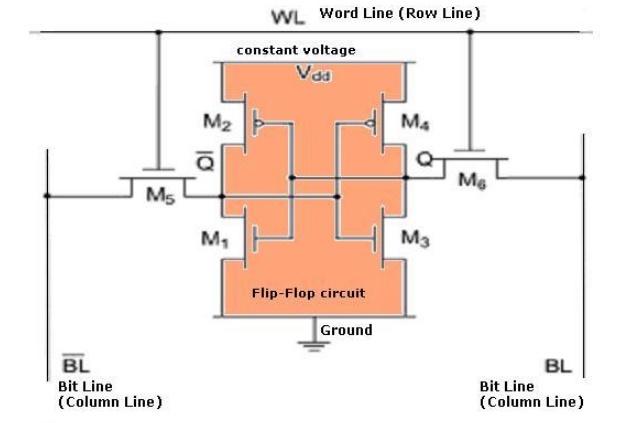
(a).SPLDs (Simple Programmable Logic Devices)

* ROM (Read-Only Memory)
* PLA (Programmable Logic Array)
* PAL (Programmable Array Logic)
* GAL (Generic Array Logic)

(b).CPLD (Complex Programmable Logic Device)

(c).FPGA (Field-Programmable Gate Array**)**

**7.**           **Draw the structure of a static RAM cell.**



**8.**           **List the advantages of PLDs.**

              low and fixed (two gate) propagation delays (typically down to 5 ns),

              simple,

              low-cost (free),

              design tools.

**9.**      **What is PAL?**

PAL is programmable array logic, PAL consists of a programmable AND array and a fixed OR array with output logic**.**

**10.**      **What is access time and cycle time of a memory?**

Access time is the maximum specified time within which a valid new data is put on the data bus after an address is applied.

Cycle time is the minimum time for which an address must be held stable on the address bus in read cycle.

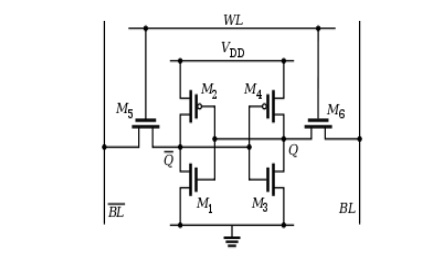
**11.**      **How the memories are classified?**

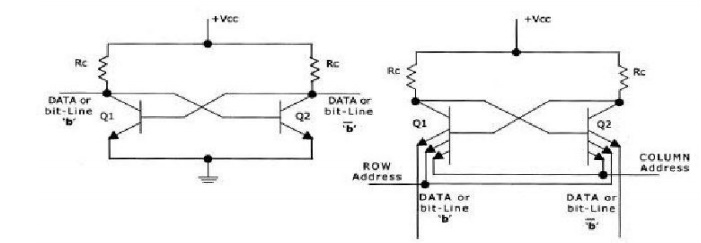
It is classified into two types:

              volatile

              non-volatile memory

**12.**      **Draw the logic diagram of a static RAM cell and Bipolar cell.**





**13.**    **What is volatile and non-volatile memory?**

* The memory which cannot hold the data when power is turned off is known as volatile memory.
* The memory which can hold the data when power is turned off is known as non-volatile memory

**14.**    **Give the advantages of RAM.**

              Read and write the data.

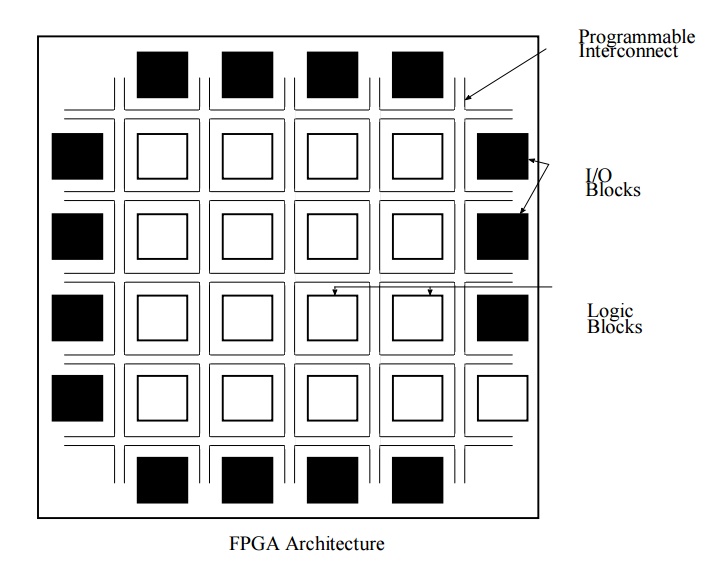
              Data is accessed by using address of the memory location.

              Higher speed.

**15. What is FPGA.**

A *field-programmable gate array* (FPGA) uses an array of logic blocks, which can be configured by the user. The term ‘field-programmable’ here signifies that the device is programmable outside the factory where it is manufactured. The internal architecture of an FPGA device has three main parts, namely the array of logic blocks, the programmable interconnects and the I/O blocks.

Each of the I/O blocks provides an individually selectable input, output or bidirectional access to one of the general-purpose I/O pins on the FPGA package. The logic blocks in an FPGA are no more complex than a couple of logic gates or a look-up table feeding a flip-flop. The programmable interconnects connect logic blocks to logic blocks and also I/O blocks to logic blocks.



**16. What is an ASIC.**

ASICs are silicon chips that have been designed for a specific application. Putting

in other words, it is a chip designed to perform a particular operation as opposed to

general purpose integrated circuits:

• An ASIC is NOT software programmable to perform different tasks.

• ICs that are not ASICs are :

– DRAM

– SRAM

– 74xx series ICs

• ICs which are ASICs:

– Baseband processor in mobile phone

– Chipsets in PCs

– MPEG encoders/ decoders

– DSP functions in hardware, e.g. FFT

**17.Difference between ASIC and FPGA.**

* An ASIC is a unique type of integrated circuit meant for a specific application while an FPGA is a reprogrammable integrated circuit.
* An ASIC can no longer be altered once created while an FPGA can.
* It is common practice to design and test on an FPGA before implementing on an ASIC.
* An ASIC wastes very little material compared to an FPGA and the recurring costs are low.
* FPGA is better than an ASIC when building low volume production circuits.

**UNIT-IV SHORT QUESTIONS**

**1.What is flow chart**

A flow chart is a convenient way to specify the sequence of procedural steps and decision paths for an algorithm. A flow chart for a hardware algorithm translates the word statement to an information diagram that enumerates the sequence of operations together with the conditions necessary for their execution.

**2.Define ASM Chart.**

A special flow chart that has been developed specifically to define digital hardware algorithms.

**3. What are the elements of ASM chat.**

(a).State box.

(b). Decision box

(c). Conditional output box.

An ASM chart has an entry point and is constructed with blocks.  A block is constucted with the following type of symbols.

|  |  |
| --- | --- |
| http://uhaweb.hartford.edu/kmhill/suppnotes/AsmChart/box1.png | One state box.  The state box has a name and lists outputs that are asserted when the system is in that state.  These outputs are called synchronous or *Moore* type outputs. |
| http://uhaweb.hartford.edu/kmhill/suppnotes/AsmChart/decision1.png | Optional decision box(es).  A decision box may be conditioned on a signal or a test of some kind. |
| http://uhaweb.hartford.edu/kmhill/suppnotes/AsmChart/output1.png | Optional conditional output box(es).  Such an ouput box indicates outputs that are conditionally asserted.  These outputs are called asynchrous or *Mealy* outputs. |

**4.Define State box.**

State name state code

A rectangle describes one state of the synchronous sequential digital system. It is similar to a circle representing a state of a state diagram. The main difference is that it only has one output transition (exit path). The state block symbol contains a listing of all unconditional actions and (Moore) outputs associated with that state. The outputs are updated concurrently when the state is entered after an active clock edge.

**5.Define decision box**.

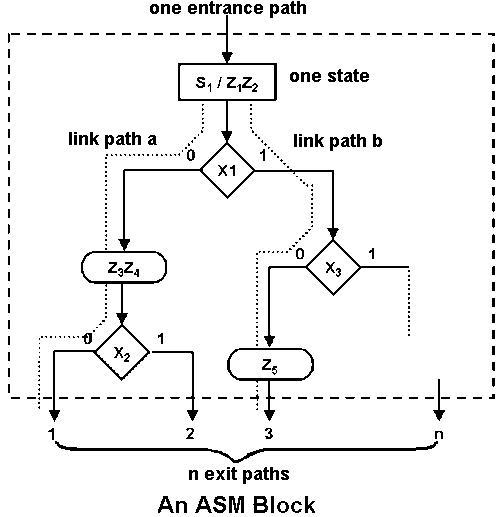
**False True**

A diamond shape contains the input condition on which depends the branching from a given state. It has one entry point and two exit path. Condition symbols can be concatenated.

**6.Define conditional box**.

An oval or rectangular with rounded edges represents an action, i.e. signal assignment or calculation, that is taken if an input condition is fulfilled. Conditional output boxes are only used to depict Mealy-type outputs. The entry path to the symbol is always from a decision symbol, but its exit path can be either to a state box or to another decision symbol.

**7.ASM Block**  
  
 An ASM block is a structure consisting of one state box and all the decision and conditional boxes connected to its exit path. An ASM block has one entrance path and one or more exit paths.



Write about Asynchronous sequential circuits.

**8.**  **What is state table?**

The state table representation of a sequential circuit consists of three sections labelled *present state*, *next state* and *output*. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

**9.What is transition table?**

Transition table is useful to analyze an asynchronous circuit from the circuit diagram  Procedure to obtain transition table: 1. Determine all feedback loops in the circuits 2. Mark the input (yi ) and output (Yi ) of each feedback loop 3. Derive the Boolean functions of all Y’s 4. Plot each Y function in a map and combine all maps into one table 5. Circle those values of Y in each square that are equal to the value of y in the same row

**10.What is flow table.**

Similar to a transition table except the states are represented by letter symbols  Can also include the output values  Suitable to obtain the logic diagram from it

**11.Primitive flow table**

In a flow table if each row consists of only one stable state then it is called as Primitive flow table

**12.What are hazard free digital circuits?**

A circuit which has no hazard like static-0-hazard and static-1-hazard is called hazard free digital circuit.

**13.**           **What are Hazards?**

The unwanted switching transients (glitches) that may appear at the output of a circuit are called Hazards.

**14.**           **Distinguish between a flowchart and an ASM chart.**

   A conventional flow chart describes the square of procedural steps and decision paths for an algorithm without concern for their time relationship.

   The ASM chart describes the sequence of event as well as timing relationship between the states of a sequential controller and the events that occur while going from one state to the next.

**15.** **What is a state diagram? Give an example.**

A state diagram is a type of diagram used in computer science and related fields to describe the behavior of systems. State diagrams require that the system described is composed of a finite number of states; sometimes, this is indeed the case, while at other times this is a reasonable abstraction. Many forms of state diagrams exist, which differ slightly and have different semantics.