LECTURE NOTES

ON

ANALOG ELECTRONIC CIRCUITS

2019 – 2020

B.E IV Semester

UNIT I
SMALL SIGNAL AMPLIFIERS

Introduction

An electronic amplifier circuit is one, which modifies the characteristics of the input signal, when delivered the output side. The modification in the characteristics of the input signal can be with respect to voltage, current, power or phase. Anyone or all these characteristics power, or phase may be changed by the amplifier circuit.

Classification of Amplifiers

There are many forms of electronic circuits classed as amplifiers, from Operational Amplifiers and Small Signal Amplifiers up to Large Signal and Power Amplifiers. The classification of an amplifier depends upon the size of the signal, large or small, its physical configuration and how it processes the input signal that is the relationship between input signal and current flowing in the load.

The type or classification of an amplifier is given in the following table.

Type of Signal	Type of Configuration	Classification	Frequency of Operation	Type of coupling	Based on the output	Number of stages
Small Signal	Common Emitter	Class A Amplifier	Direct Current (DC)	a. RC coupled amplifiers	a. Voltage amplifiers	a. Single stage amplifiers
Large Signal	Common Base	Class B Amplifier	Audio Frequencies (AF)	b. Inductive coupled amplifiers	b. Power amplifiers	b. Two stage amplifiers
	Common Collector	Class AB Amplifier	Radio Frequencies (RF)	c. Transformer coupled amplifiers and		c. Multistage amplifiers.
		Class C Amplifier	VHF, UHF and SHF Frequencies	d. Direct coupled amplifiers.		the number of stages,

Characteristics of amplifiers:

Amplifiers can be thought of as a simple box or block containing the amplifying device, such as a **Transistor**, **Field Effect Transistor** or **Op-amp**, which has two input terminals and two output terminals (ground being common) with the output signal being much greater than that of the input signal as it has been–Amplified‖.

Generally, an ideal signal amplifier has three main properties, Input Resistance or (Rin), Output Resistance or (Rout) and of course amplification known commonly as Gain or (A). No matter how complicated an amplifier circuit is, a general amplifier model can still be used to show the relationship of these three properties.

To choose a right kind of amplifier for a purpose it is necessary to know the general characteristics of amplifiers. They are: Current gain, Voltage gain, Power gain, Input impedance, Output impedance, Bandwidth.

1. Voltagegain:

Voltage gain of an amplifier is the ratio of the change in output voltage to the corresponding change in the input voltage.

$$A_V = \Delta V_0 / \Delta V_I$$

2. Current gain: Current gain of an amplifier is the ratio of the change in output current to the corresponding change in the inputcurrent

$$A_I = \Delta I_0 / \Delta I_I$$

3. Power gain: Power gain of an amplifier is the ratio of the change in output power to the corresponding change in the input power. wherepo and pi are the output power and input power respectively. Since power p = v × i, The power gain

$$A_P = P_O / P_I$$

$$A_P = A_V \text{ x } A_I$$

(Power amplification of the input signal takes place at the expense of the d.c. energy.)

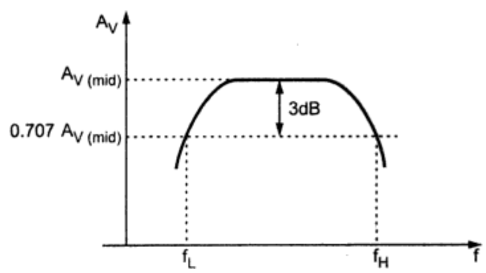
4. Input impedance (Zi): Input impedance of an amplifier is the impedance offered by the amplifier circuit as seen through the input terminals and is given by the ratio of the input voltage to the inputcurrent

$$Z_I = \Delta V_I / \Delta I_I$$

5. Output impedance (Z0): Output impedance of an amplifier is the impedance offered by the amplifier circuit as seen through the output terminals and is given by the ratio of theoutput

$$Z_O = \Delta V_O / \Delta I_O \text{ (At } V_s=0)$$

6. Band width (BW): The range of frequencies over which the gain (voltage gain or current gain) of an amplifier is equal to and greater than 0.707 times the maximum gain is called thebandwidth.



In figure shown, f_L and f_H are the lower and upper cutoff frequencies where the voltage or the current gain falls to 70.7% of the maximum gain.

Bandwidth $BW=(f_H - f_L)$.

Bandwidth is also defined as the range of frequencies over which the power gain of amplifier is equal to and greater than 50% of the maximum power gain.

The cutoff frequencies are also defined as the frequencies where the power gain falls to 50% of the maximum gain. Therefore, the cutoff frequencies are also called as Half power frequencies.

Comparison of CB, CE and CC amplifiers:

Parameters	CB	CE	CC
1. Current gain	Less than 1($\alpha \approx 1$)	High (β>1)	Highest (γ>1) (γ= β+1)
2. Voltage gain	High	Very high	Less than 1
3. Power gain	High	Highest	>1 (low when compared to CB & CE amplifiers)
4.Input impedance	Lowest	Moderate	Highest
5.Output impedance	Highest	Moderate	Lowest
6.Phase difference	0^0 or 2π	180^0or (2n+1) π	0^0 or 2π
7. Applica-tions	Used mainly as HF amplifier	Used as a (voltage amplifier)	Used as a Buffer amplifier, impedance matching unit

Classification of amplifiers, Methods of coupling**,** Cascade transistor amplifier and its analysis, Cascode amplifier, Darlington pair and its analysis, Boot-strap emitter follower, Effect of cascading on Bandwidth.

Classification of Amplifiers

Amplifiers can be classified as follows:

1. Based on the transistor configuration
   (a) Common emitter amplifier
   (b) Common collector amplifier
   (c) Common base amplifier
2. Based on the active device
   (a) BJT amplifier
   (b) FET amplifier
3. Based on the Q-point (operating condition)
   (a) Class A amplifier
   (b) Class B amplifier
   (c) Class AB amplifier
   (d) Class C amplifier
4. Based on the number of stages
   (a) Single stage amplifier
   (b) Multistage amplifier
5. Based on the output
   (a) Voltage amplifier
   (b) Power amplifier
6. Based on the frequency response
   (a) Audio frequency (AF) amplifier
   (b) Intermediate frequency (IF) amplifier
   (c) Radio frequency (RF) amplifier
7. Based on the bandwidth
   (a) Narrow band amplifier (normally RF amplifier)
   (b) Wide band amplifier (normally video amplifier)

Multistage Amplifiers:

If the voltage or power gain obtained from a single stage small signal amplifier is not sufficient for a practical application, one have to use more than one stage of amplification to achieve necessary voltage and power gain. Such an amplifier is called a multistage amplifier. In multistage amplifier, the output of one stage is fed as the input to the next as shown in Fig. 10.1. Such a connection is commonly referred to as cascading. In amplifiers, cascading is also done to achieve correct input and output impedances for specific applications. Depending upon the type of amplifier used in individual stages, multistage amplifiers can be classified into several types. A multistage amplifier using two or more single stage common emitter amplifier is called as cascaded amplifiers. A multistage amplifier with common emitter as the first stage and common base as the second stage is called as cascode amplifier. Such cascade and cascode connections are also possible in FET amplifiers.

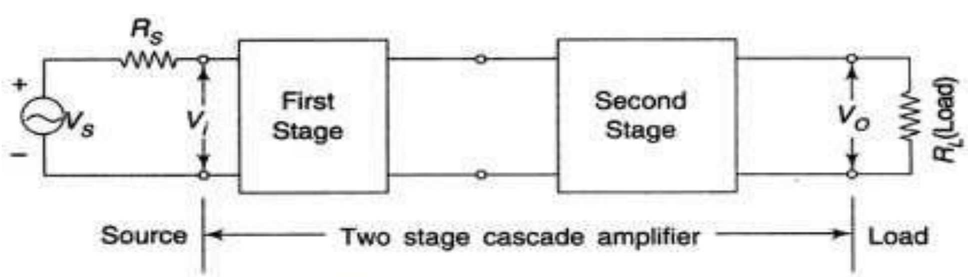


Fig. 10.1 Multistage amplifier

10.2 DIFFERENT COUPLING SCHEMES USED IN AMPLIFIERS

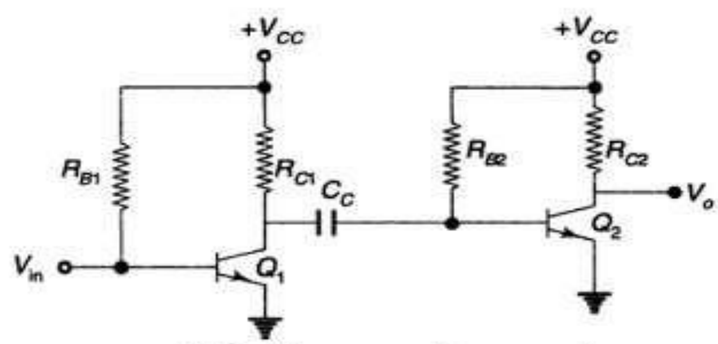
When amplifiers are cascaded, it is necessary to use a coupling network between the output of one amplifier and the input of the following amplifier. This type of coupling is called inter stage coupling. Basically, these coupling networks serve the following two purposes.

(1) It transfers the a.c. output of one stage to the input of the next stage.
(2) It isolates the d.c. conditions of one stage to the next.

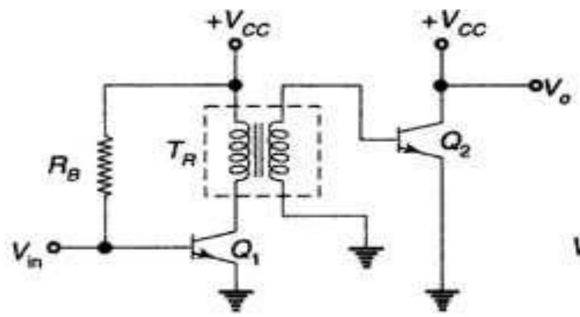
1. Resistance-capacitance (RC) coupling It is the most commonly used discrete device amplifiers as it is least expensive and has satisfactory frequency response. In this method the signal developed across the collector resistor R_c of each stage is coupled through capacitor C_c into the base of the next stage as shown in Fig. 10.2(a). The coupling capacitor C_c isolates the d.c. conditions of one stage from the following stage. The amplifiers using this coupling scheme are called RC-coupled amplifiers.

2. Transformer coupling In this method, the primary winding of the transformer acts as a collector load and the secondary winding transfers the a.c. output signal directly to the base of the next stage as shown in Fig. 10.2(b). Such a coupling increases the overall circuit gain and the level of inter stage impedance matching. However, transformers with broad frequency response are very expensive and hence, this type of coupling is restricted mostly to power amplifiers where efficient impedance matching is a critical requirement for maximum power transfer and efficiency. The amplifiers using this coupling scheme are called Transformer-coupled amplifiers.

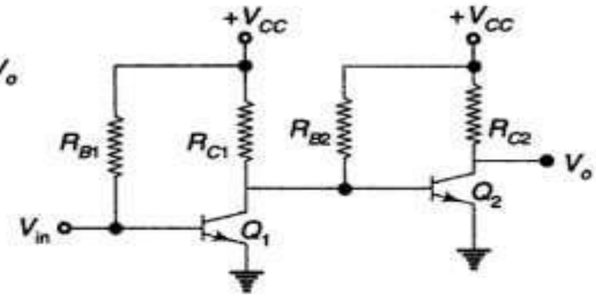
3. Direct coupling In this method the a.c. output signal is fed directly to the next stage as shown in Fig. 10.2(c). No reactance is included in the coupling network. Special d.c. voltage level circuits are used to match the output d.c. levels. It is used when amplification of low frequency signals is to be done. Further, coupling devices such as capacitors, transformers cannot be used at low frequencies because their



(a) Resistance-capacitance coupling



(b) Transformer coupling



(c) Direct coupling

Fig. 10.2

size becomes very large. The amplifiers using this coupling schemes are called direct-coupled amplifiers or d.c. amplifiers.

7.6.4 Comparison between Various Cascading Methods

Parameter	RC coupled	Transformer coupled	Direct coupled
Coupling components	Resistor and Capacitor	Impedance matching transformer	–
Block d.c.	Yes	Yes	No
Frequency response	Flat at middle frequencies	Not uniform, high at resonant frequency and low at other frequencies	Flat at middle frequencies and improvement in the low frequency response
Impedance matching	Not achieved	Achieved	Not achieved
d.c. amplification	No	No	Yes
Weight	Light	Bulky and heavy	-
Drift	Not present	Not present	Present
Hum	Not present	Present	Not present
Application	Used in all audio small signal amplifiers. Used in record players, tape recorders, public address systems, radio receivers and television receivers.	Used in amplifier where impedance matching is an important criteria. Used in the output stage of the public, address system to match the impedance of loudspeaker. Used in the RF amplifier stage of the receiver as a tuhed voltage amplifier.	Used in amplification of slow varying parameters and where DC amplification is required.

Table 7.2

10.3 GENERAL ANALYSIS OF CASCADE AMPLIFIER

The most popular cascade amplifier is formed by cascading several CE amplifier stages. Before considering the analysis of any specific type of multistage amplifiers the analysis of a general '*n*' stage CE amplifier shown in Fig. 10.6 is done in this section.

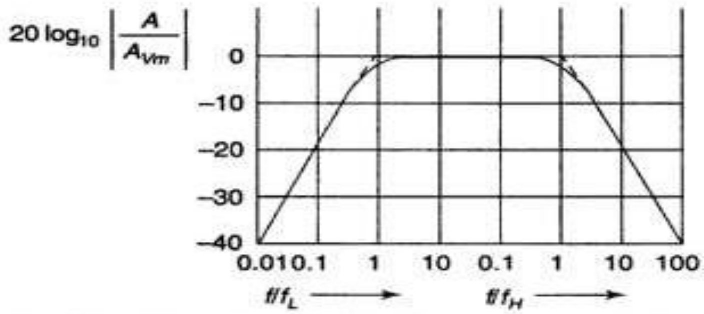


Fig. 10.5 Plot of gain versus frequency for an RC coupled amplifier

Biasing arrangements and coupling elements are omitted for simplicity. The expressions for quantities such as voltage gain, current gain, power gain, input impedance and output impedance of this 'n' stage CE amplifier are to be derived.

(a) Voltage gain In a multistage amplifier the output voltage of the first stage acts as the input voltage of second stage and so on. The voltage gain of the complete cascade amplifier is equal to the product of the voltage gains of the individual stages.

Proof: The voltage gain of the first stage

$$\bar{A}_{V1} = \frac{\bar{V}_2}{\bar{V}_1} = \frac{\text{output voltage of the first stage}}{\text{input voltage of the first stage}}$$

$$= A_{V1} \angle\theta_1$$

where A_{V1} is the magnitude of voltage gain and θ_1 is phase angle of the output voltage relative to input voltage. Similarly,

$$\bar{A}_{V2} = \frac{\bar{V}_3}{\bar{V}_2} = \frac{\text{output voltage of the second stage}}{\text{input voltage of the second stage}}$$

$$= A_{V2} \angle\theta_2$$

Similar expressions can be written for all the 'n' stages of the cascade amplifier. The resultant voltage gain,

$$\bar{A}_V = \frac{\bar{V}_0}{\bar{V}_1} = \frac{\text{output voltage of the } n\text{th stage}}{\text{input voltage of the first stage}}$$

$$= A_V \angle\theta$$

But

$$\frac{\bar{V}_0}{\bar{V}_1} = \frac{\bar{V}_2}{\bar{V}_1} \times \frac{\bar{V}_3}{\bar{V}_2} \times \frac{\bar{V}_4}{\bar{V}_3} \cdots \frac{\bar{V}_n}{\bar{V}_{(n-1)}} \times \frac{\bar{V}_0}{\bar{V}_n}$$

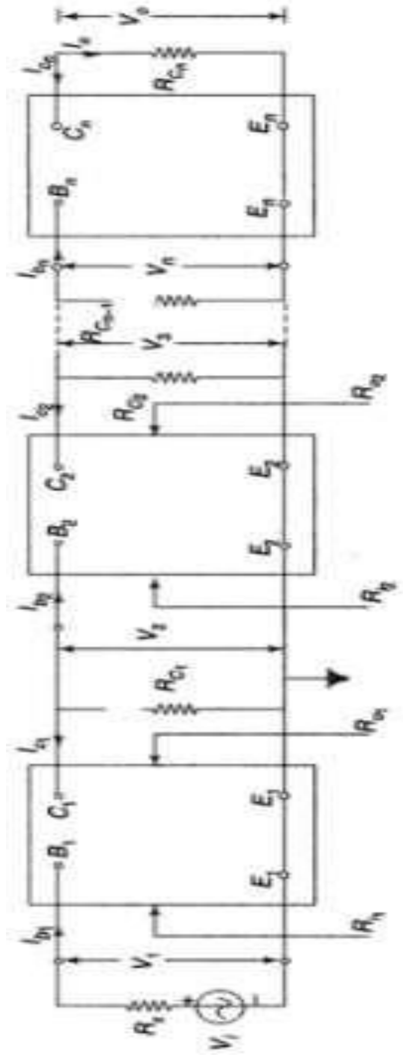


Fig. 10.6 'n' stage CE amplifier

Hence, it follows that

$$\bar{A}_V = \bar{A}_{V1} \cdot \bar{A}_{V2} \cdot \bar{A}_{V3} \ldots \bar{A}_{Vn} \tag{10.1}$$

$$= A_{V1} \cdot A_{V2} \cdot A_{V3} \ldots A_{Vn} \ldots \angle\theta_1 + \angle\theta_2 + \angle\theta_3 + \ldots \angle\theta_n$$

$$= A_V \angle \theta$$

Hence,

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3} \ldots A_{Vn} \tag{10.2}$$

and

$$\theta = \theta_1 + \theta_2 + \theta_3 \ldots + \theta_n \tag{10.3}$$

From Eqns (10.2) and (10.3), one can conclude that (i) the magnitude of the resultant voltage gain equals the product of the magnitudes of the voltage gains of the individual stages, and (ii) the phase shift of the resultant voltage gain equals the sum of the phase shifts of the individual stages comprising the multistage cascade amplifier.

Figure 10.7 shows a particular stage, say, the K^{th} stage, say of the n stage cascaded amplifier. From Eqn. (10.3), the voltage gain of the K^{th} stage is given by

$$\bar{A}_{VK} = \frac{\bar{A}_{IK}\, R_{LK}}{R_{iK}} \tag{10.4}$$

where R_{LK} is the effective load impedance at the collector of the K^{th} stage and R_{iK} is the input impedance of the K^{th} stage.

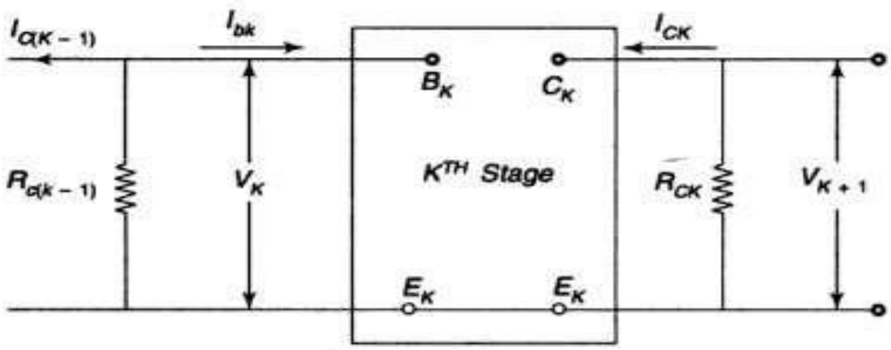


Fig. 10.7 K^{th} stage of a cascaded amplifier

The terms $\bar{A}_{IK}$, R_{LK} and R_{iK} may be evaluated by starting from the last stage and proceeding backward to the first stage.

From the Eqn. (9.123), the current gain

$$A_{In} = \frac{-h_{fe}}{1 + h_{oe}\, R_{Ln}}$$

and from Eqn. (9.125),

$$R_{in} = h_{ie} + h_{re}\, A_{In}\, R_{Ln}$$

where R_{Ln} is the effective load impedance for the last stage and equals R_{cn}.

The effective load impedance $R_{L\,(n-1)}$ of the $(n-1)^{th}$ stage is equal to

$$R_{C\,(n-1)} \,||\, R_{i(n)}$$

Thus,

$$R_{L\,(n-1)} = \frac{R_{C\,(n-1)} \times R_{i\,(n)}}{R_{C\,(n-1)} + R_{i\,(n)}} \tag{10.5}$$

Having known $R_{L(n-1)}$ $A_{I(n-1)}$ can be found out from

$$A_{I(n-1)} = \frac{-h_{fe}}{1 + h_{oe}\, R_{L\,(n-1)}} \tag{10.6}$$

and $R_{i(n-1)}$ can be found from

$$R_{i\,(n-1)} = h_{ie} + h_{re}\, A_{I(n-1)}\, R_{L(n-1)} \tag{10.7}$$

By proceeding in this manner one can calculate the current gain and input impedance of each stage including the first. The voltage gain of each stage can be obtained from Eqn. (10.4) for that stage.

Current gain In order to find the resultant voltage gain, the voltage gain of the individual stages can be found out and the product of these gains gives the resultant voltage gain. Alternatively, the resultant voltage gain can be found directly by the relation

$$\overline{A}_V = \frac{\overline{A}_I R_{Cn}}{R_{i1}}$$

where $\overline{A}_I$ is the current gain of the complete n-stage amplifier.

Now, $\overline{A}_I$ is given by

$$\overline{A}_I = \frac{\overline{I}_o}{\overline{I}_{b1}} = \frac{-\overline{I}_{cn}}{\overline{I}_{b1}}$$

Now,
$$\frac{-\overline{I}_{cn}}{\overline{I}_{b1}} = \frac{-\overline{I}_{c1}}{\overline{I}_{b1}} \cdot \frac{\overline{I}_{c2}}{\overline{I}_{c1}} \cdots \frac{\overline{I}_{cn}}{\overline{I}_{c(n-1)}}$$

or

$$\overline{A}_I = \overline{A}_{I1} \cdot \overline{A}_{I2}' \cdot \overline{A}_{I3}' \cdots \overline{A}_{In}' \tag{10.8}$$

Here, $\overline{A}_{I1}$ is the base to collector gain of the first stage and equals $\dfrac{-\overline{I}_{c1}}{\overline{I}_{b1}}$,

while $\overline{A}_{I2}'$, $\overline{A}_{I3}'$ are the collector to collector current gains of second and third stages.

For K^{th} stage the collector to collector current gain is given by

$$\overline{A}_{IK}' = \frac{\overline{I}_{CK}}{\overline{I}_{C(K-1)}}$$

For the same K^{th} stage, the base to collector current gain is given by

$$\overline{A}_{IK} = -\frac{\overline{I}_{CK}}{\overline{I}_{bK}}$$

These two current gains can be related by the equation,

$$\overline{A}_{IK}' = \overline{A}_{IK} \frac{R_{C(K-1)}}{R_{C(K-1)} + R_{iK}} \tag{10.9}$$

This may be substituted in Eqn. (10.8) to give the resultant current gain $\overline{A}_I$.

The procedure for calculating the resultant current gain $\overline{A}_I$ is as follows.

(i) Find the base to collector current gain $\overline{A}_{In}$ for the last stage, i.e. n^{th} stage using

$$\overline{A}_{In} = \frac{-h_{fe}}{1 + h_{oe} R_{Ln}}$$

(ii) Find input impedance,

$$R_{in} = h_{ie} + h_{re} A_{In} R_{Ln}$$

(iii) Calculate the effective load resistance $R_{L(n-1)}$ for the last stage

$$R_{L(n-1)} = R_{C(n-1)} \parallel R_{i(n)}$$

(iv) Calculate

$$\bar{A}_{I(n-1)} = \frac{-h_{fe}}{1+h_{oe}\, R_{L(n-1)}}$$

Proceed in this manner to find $\bar{A}_{IK}$

(v) Find the collector to collector current gain $\bar{A}_{IK}'$ for the K^{th} stage using

$$\bar{A}_{IK}' = \bar{A}_{IK}\, \frac{R_{C(K-1)}}{\bar{R}_{C(K-1)} + R_{iK}}$$

(vi) Find the resultant current gain $\bar{A}_I$ of the n-stage cascaded amplifier using

$$\bar{A}_I = \bar{A}_{I1}\, .\bar{A}_{I2}'\, .\bar{A}_{I3}' \ldots \bar{A}_{In}'$$

Power gain The power gain of n-stage amplifier is given by

$$\bar{A}_P = \frac{\text{output power of last stage}}{\text{input power of first stage}}$$

$$= \frac{\bar{V}_o \bar{I}_o}{\bar{V}_1 \bar{I}_{b1}} = \frac{-\bar{V}_o \bar{I}_{cn}}{\bar{V}_1 \bar{I}_{b1}}$$

$$= \bar{A}_V\ \bar{A}_I \tag{10.10}$$

Substituting $\bar{A}_V = \bar{A}_I \dfrac{R_{cn}}{R_{i1}}$,

$$\bar{A}_P = (\bar{A}_I)^2 \frac{R_{cn}}{R_{i1}}$$

Input impedance By starting from last stage and proceeding towards the first stage, the input impedance can be found out as follows.

Find (i) $\bar{A}_{In} = \dfrac{-h_{fe}}{1+h_{oe} R_{Ln}}$

(ii) $\bar{R}_{in} = h_{ie} + h_{re}\bar{A}_{In} R_{Ln}$

(iii) $\bar{R}_{L(n-1)} = R_{C(n-1)} \| R_{i(n)}$

$\bar{R}_{L(n-1)}$ is the effective load impedance of the $(n-1)^{th}$ stage.

(iv) Calculate $\bar{A}_{I(n-1)}$, $\bar{R}_{i(n-1)}$ and $\bar{R}_{L(n-2)}$ from the above equations.

(v) Proceed in this manner to find the effective input impedance (R_i) of the first stage.

Input impedance By starting from last stage and proceeding towards the first stage, the input impedance can be found out as follows.

Find (i) $\bar{A}_{In} = \dfrac{-h_{fe}}{1 + h_{oe} R_{Ln}}$

(ii) $\bar{R}_{in} = h_{ie} + h_{re} \bar{A}_{In} R_{Ln}$

(iii) $\bar{R}_{L(n-1)} = R_{C(n-1)} \| R_{i(n)}$

$\bar{R}_{L(n-1)}$ is the effective load impedance of the $(n-1)^{th}$ stage.

(iv) Calculate $\bar{A}_{I(n-1)}$, $\bar{R}_{i(n-1)}$ and $\bar{R}_{L(n-2)}$ from the above equations.

(v) Proceed in this manner to find the effective input impedance (R_i) of the first stage.

Output impedance The output impedance of each transistor amplifier stage and that of the complete multistage amplifiers may be calculated starting from the first stage. From Eqn. (10.6) the output admittance of first transistor,

$$Y_{o1} = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} \quad (10.11)$$

$R_{o1} = \dfrac{1}{Y_{o1}}$ gives the output impedance of the first transistor.

Parallel combination of R_{o1} with R_{c1} forms the output impedance of the first stage.

$$R_{ot1} = \frac{R_{o1} R_{c1}}{R_{o1} + R_{c1}}$$

This R_{ot1} forms the source impedance of the second stage. Once again use Eqn. (3.10) to find Y_{o2} with R_s replaced by R_{ot1}.

Find $R_{ot2} = R_{o2} \| R_{c2}$, where $R_{o2} = \dfrac{1}{Y_{o2}}$

Similarly, proceed to find output impedance of the last stage.

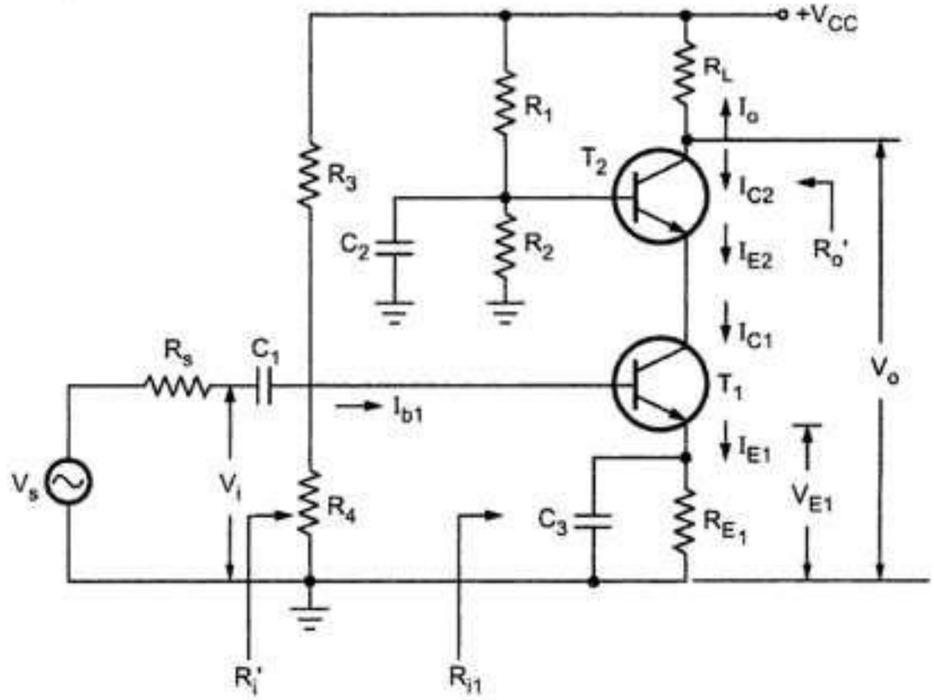
The above methods can be used for common base and common collector configurations, also as well as for combination of these three configurations.

Cascode Amplifier:

The cascode amplifier consists of a common emitter amplifier stage in series with a common base amplifier stage as shown in the Fig. B.1. It is one approach to solve the low impedance problem of a common base circuit. Transistor, T_1 and its associated components operate as a common emitter amplifier stage, while the circuit of T_2 functions as a common base output stage. The cascode amplifier gives the high input impedance of a common emitter amplifier, as well as the good voltage gain and high frequency performance of a common base circuit.

▶ **Figure B.1**

Cascode amplifier



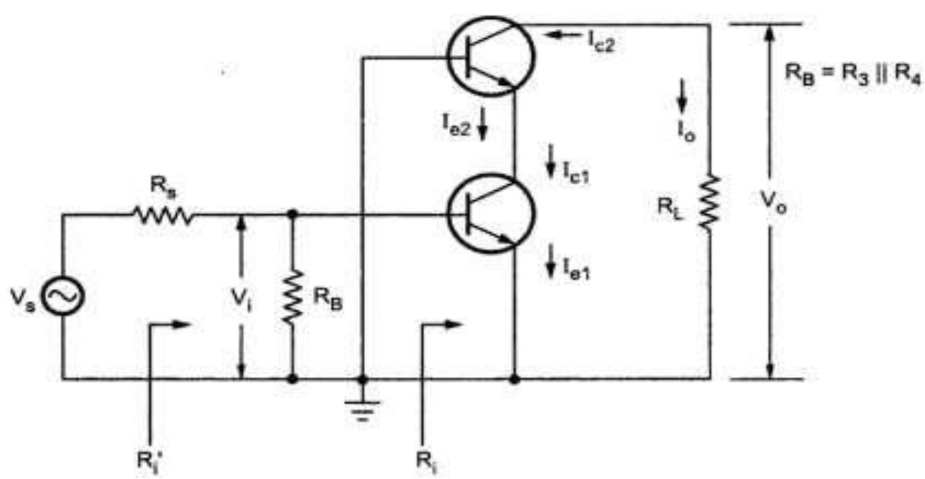
For the dc bias conditions of the circuit, it is seen that the emitter current for T_1 is set by V_{E1} and R_{E1}. Collector current I_{C1} approximately equals I_{E1}, and I_{E2} is same as I_{C1}.

Therefore, I_{C2} approximately equals I_{E1}. This current remains constant regardless of the level of V_{B2}, as long as V_{CE1} remains large enough for current operation of T_1 .

Fig. B.2 shows the ac equivalent circuit for cascode amplifier. It is drawn by shorting dc supply and capacitors.

▶ **Figure B.2**

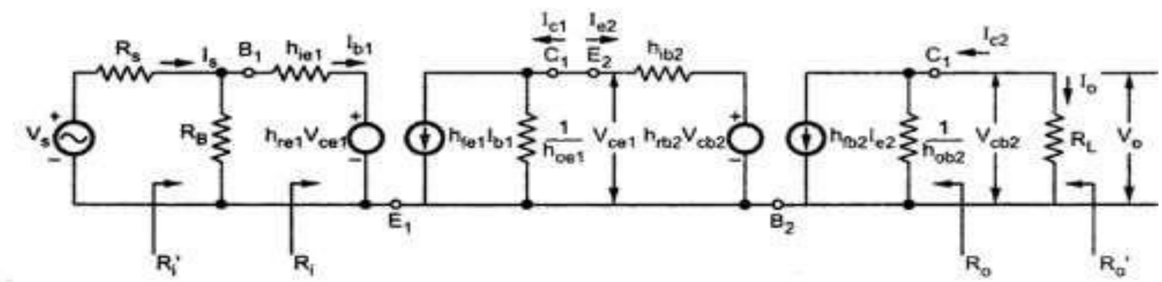
AC equivalent circuit



The h-parameter equivalent circuit for cascode amplifier is drawn by replacing transistors with their equivalent circuits, as shown in the Fig. B.3.

▶ Figure B.3

h-parameter equivalent circuit for cascode amplifier



Derivation of parameter values for cascode amplifier

Input Resistance (h_{11}) :

The input resistance with output short circuited is given as

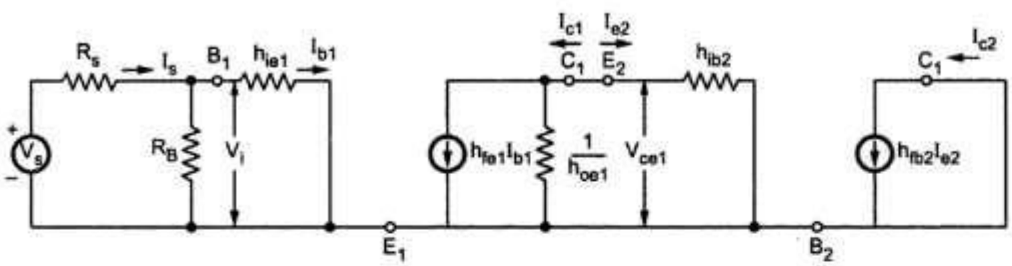
$$h_{11} = \left.\frac{V_i}{I_b}\right|_{V_{cb2}=0}$$

The input impedance of CB configuration, h_{ib2} is nearly 20 Ω,

Therefore, transistor T_1 is effectively short circuited and $h_{re1}\ V_{ce1} = 0$, as shown in the Fig. B.4.

▶ Figure B.4

h-parameter equivalent circuit when output shorted



Looking at Fig. B.4, we can write,

$$h_{11} = \left.\frac{V_i}{I_{b1}}\right|_{V_{cb2}=0} = h_{ie} \qquad \text{... (B.1)}$$

Similarly, short circuit current gain is given as,

$$h_{21} = \left.\frac{I_{c2}}{I_{b1}}\right|_{V_{cb2}=0} = \frac{I_{c2}}{I_{e2}} \times \frac{I_{e2}}{I_{c1}} \times \frac{I_{c1}}{I_{b1}}$$

$$\approx h_{fb} \times -1 \times h_{fe}$$

$$\approx -h_{fb}\ h_{fe} \qquad \text{... (B.2)}$$

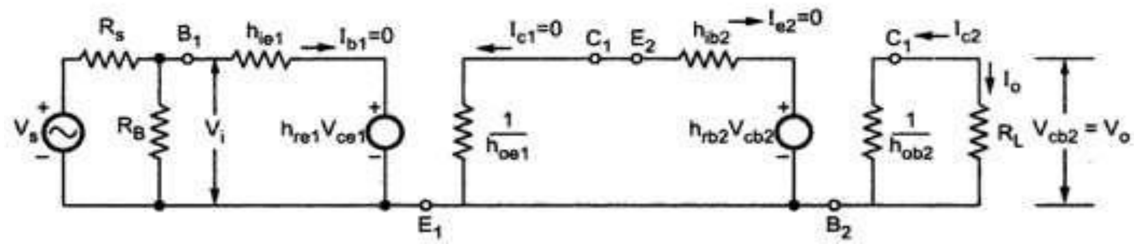
The reverse voltage amplification with input open circuited is given as

$$h_{12} = \left.\frac{V_i}{V_{cb2}}\right|_{I_b=0}$$

The Fig. B.5 shows the equivalent circuit when $I_b = 0$

Figure B.5

h-parameter equivalent circuit when $I_b = 0$



As $I_{b1} = 0$, $\quad V_i = h_{re1} V_{ce1}$ and

as $I_{e2} = 0$, $\quad V_{ce1} = h_{rb2} V_{cb2}$

$$\therefore \quad V_{cb2} = \frac{V_{ce1}}{h_{rb2}}$$

Substituting values of V_i and V_{cb2} we have

$$h_{12} = \frac{h_{re1} V_{ce1}}{\frac{V_{ce1}}{h_{rb2}}} = h_{re1}\, h_{rb2} \qquad \dots \text{(B.3)}$$

Looking at Fig. B.5 output admittance with input open circuited is given as

$$h_{22} = h_{rb2} \qquad \dots \text{(B.4)}$$

Therefore, h-parameters for cascode amplifier are as follows :

$h_{11} = h_{ie}$ $\qquad h_{21} = -h_{fb}\, h_{fe}$

$h_{12} = h_{re1}\, h_{rb2}$ $\qquad h_{22} = h_{ob2}$

Example B.1 : *For a cascode amplifier, $h_{ie1} = 1.1$ K, $h_{re1} = 2.5 \times 10^{-4}$, $h_{fe1} = 50$, $h_{oe1} = 2.4 \times 10^{-5}$, $h_{ib2} = 21.6\ \Omega$, $h_{fb2} = -0.98$, $h_{rb2} = 2.9 \times 10^{-4}$ $h_{ob2} = 0.49 \times 10^{-6}$, $R_S = 1$ K, $R_L = 3$K. Calculate A_i, A_v, A_{vs}, R_i' and R_o'. Assume $R_3 = 200$ K, $R_4 = 10$ K.*

Solution :

$$\textbf{Current Gain } (A_i) = \frac{I_o}{I_i} = \frac{-I_{C2}}{I_{b1}}$$

Substituting value of I_{C2}/I_{b1} from equation (B.2) we get,

$$A_i = \frac{-I_{C2}}{I_{b1}} = h_{fb}\, h_{fe} = -0.98 \times 50$$

$$= -49$$

Input Resistance (R_i) $\qquad R_i = h_{ie1} = 1.1$ K

Voltage Gain (A_V) : $\qquad A_V = \frac{A_i R_L}{R_i} = \frac{(-49) \times 3K}{1.1 K} = -133.64$

Input Resistance R_i' $\qquad R_i' = R_i \parallel R_B = R_i \parallel R_3 \parallel R_4$

$$= 1.1\text{ K} \parallel 200\text{ K} \parallel 10\text{ K} = 986\ \Omega$$

Voltage Gain (A_{VS}) $\qquad A_{VS} = \frac{A_V R_i'}{R_s + R_i'} = \frac{-133.64 \times 986}{1K + 986}$

$$= -66.35$$

Current Gain (A_{is}) $$A_{is} = \frac{I_o}{I_s} = \frac{I_o}{I_{b1}} \times \frac{I_{b1}}{I_s}$$

where $$\frac{I_{b1}}{I_s} = \frac{R_s || R_3 || R_4}{R_s || R_3 || R_4 + R_i} = \frac{1\text{ K} || 200\text{ K} || 10\text{ K}}{1\text{ K} || 200\text{ K} || 10\text{ K} + 1.1\text{ K}}$$

$$= 0.451$$

$\therefore$ $$A_{is} = A_i \times 0.451 = -49 \times 0.451 = -22.1$$

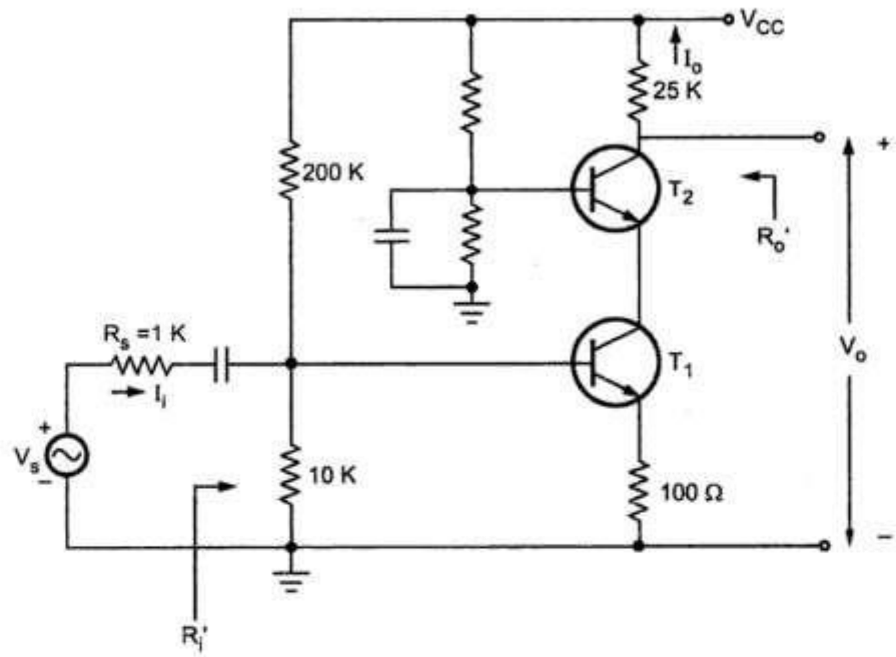
Output Resistance (R_o) $$R_o = \frac{1}{h_{ob2}} = \frac{1}{0.49 \times 10^{-6}} = 2040.8\text{ K}$$

Output Resistance (R'_o) : $$R'_o = R_o \parallel R_L = 2040.8\text{ K} \parallel 3\text{K} = 2995.6\ \Omega$$

Example B.2 : *Calculate $A_i = I_o/I_i$, A_v, A_{vs}, R'_i and R'_o for the cascode circuit shown in the Fig. B.6.*

Figure B.6

Transistor parameters are :



$h_{ie1} = 1.1$ K, $h_{fe} = 49$, $h_{oe} = 0.49 \times 10^{-6}$, $h_{re} = 7.25 \times 10^{-8}$, $h_{fb} \approx -1$, and $h_{ob} = 0.49 \times 10^{-6}$.

Solution : Current Gain (A_i) : $$A_i = \frac{I_o}{I_i} = \frac{-I_{C2}}{I_{b1}}$$

$$= h_{fb}\, h_{fe} = -1 \times 49 = -49$$

Input Resistance (R_i) : $$R_i = h_{ie1} + (1 + h_{fe})\, R_E = 1.1\text{ K} + 50 \times 0.1\text{ K}$$

$$= 6.1\text{ K}$$

Voltage Gain (A_V) :

$$A_v = \frac{A_i R_L}{R_i} = \frac{-49 \times 25K}{6.1\,K}$$
$$= -200.8$$

Input Resistance (R_i')

$$R_i' = R_i \parallel 10\,K \parallel 200\,K$$
$$= 6.1\,K \parallel 10\,K \parallel 200\,K$$
$$= 3.72\,K$$

Voltage Gain (A_{VS})

$$A_{VS} = A_V \frac{R_i'}{R_s + R_i'} = -200.8 \times \frac{3.72}{1K + 3.72\,K}$$
$$= -158.26$$

Output Resistance (R_o) :

$$R_o = \frac{1}{h_{ob}} = \frac{1}{0.49 \times 10^{-6}} = 2040.8\,K$$

Output Resistance (R_o')

$$R_o' = R_o \parallel R_L = 2040.8\,K \parallel 25\,K = 24.69\,K$$

2.12 Techniques of Improving Input Impedance

We have seen that out of three configurations (CB, CC and CE), common collector or emitter follower circuit has high input impedance. Typically it is 200 kΩ to 300 kΩ. A single stage emitter follower circuit can give input impedance upto 500 kΩ. However, the input impedance considering biasing resistors is significantly less. Because $R_i' = R_1 \parallel R_2 \parallel R_i$. The input impedance of the circuit can be improved by direct coupling of two stages of emitter follower amplifier. The input impedance can be increased using two techniques :

- Using direct coupling (Darlington connection)
- Using Bootstrap technique

2.12.1 Darlington Transistors

Fig. 2.59 shows the direct coupling of two stages of emitter follower amplifier. This cascaded connection of two emitter followers is called the Darlington connection.

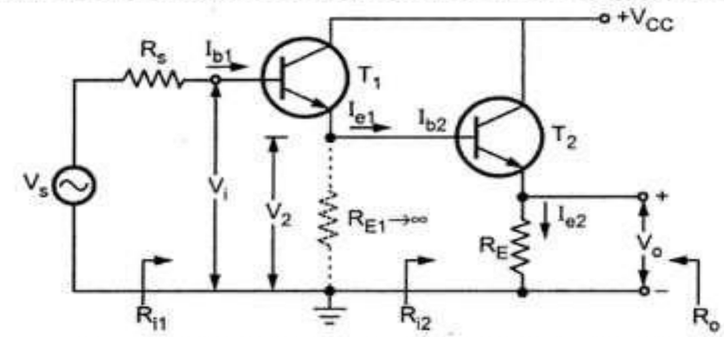


Fig. 2.59 Darlington emitter follower circuit

AC Equivalent Circuit :

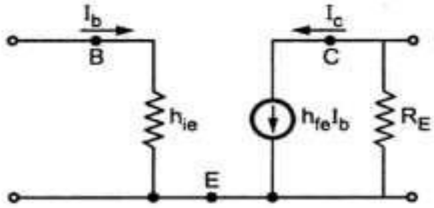


Fig. 2.60

Assume that the load resistance R_L is such that $R_L\, h_{oe} < 0.1$, therefore we can use approximate analysis method for analysing second stage.

Fig. 2.60 shows approximate h-parameter (AC) equivalent circuit for common emitter configuration.

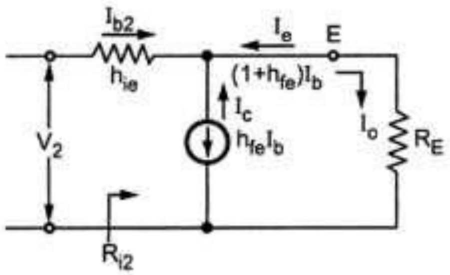


Fig. 2.61

The same circuit can be redrawn by making collector common to have approximate h-parameter equivalent circuit for common collector configuration as shown in Fig. 2.61.

Analysis of second stage :

a) Current Gain (A_{i2}) : $A_{i2} = \frac{I_o}{I_b} = -\frac{I_e}{I_b} = \frac{I_b + h_{fe} I_b}{I_b} = \frac{I_b(1+h_{fe})}{I_b}$

$$\therefore \quad \boxed{A_{i2} = 1 + h_{fe}} \qquad \ldots (1)$$

b) Input Resistance (R_{i2}) : $R_{i2} = \frac{V_2}{I_{b2}}$

Applying KVL to outer loop we get,

$$V_2 - I_{b2} h_{ie} - I_o R_E = 0$$

$$\therefore \quad V_2 = I_{b2} h_{ie} + I_o R_E$$

$$\therefore \quad \frac{V_2}{I_{b2}} = h_{ie} + \frac{I_o}{I_{b2}} R_E$$

$$\therefore \quad R_{i2} = h_{ie} + A_{i2} R_E \quad \text{since, } \frac{I_o}{I_{b2}} = A_{i2}$$

$$\therefore \quad \boxed{R_{i2} = h_{ie} + (1 + h_{fe}) R_E} \qquad \ldots (2)$$

$$R_{i2} = (1 + h_{fe}) R_E \qquad \because h_{ie} << (1 + h_{fe}) R_E \qquad \ldots (3)$$

Analysis of first stage :

Looking at Fig. 2.60 we can see that load resistance of the first stage is the input resistance of the second stage i.e. R_{i2}. As R_{i2} is high, usually it does not meet the requirement $h_{oe} R_{i2} < 0.1$, and hence we have to use the exact analysis method for analysis of the first stage.

Fig. 2.62 shows the h-parameter equivalent circuit for common emitter configuration.

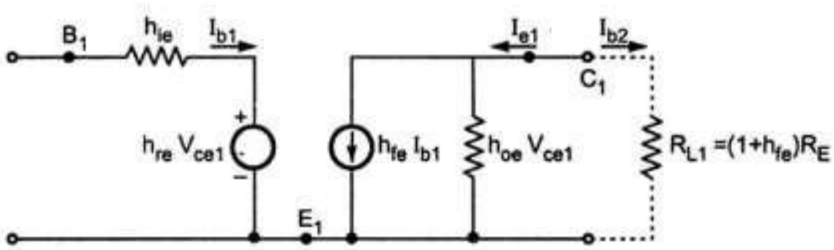


Fig. 2.62

The same circuit can be redrawn by making collector common to have h-parameter equivalent circuit for common collector configuration.

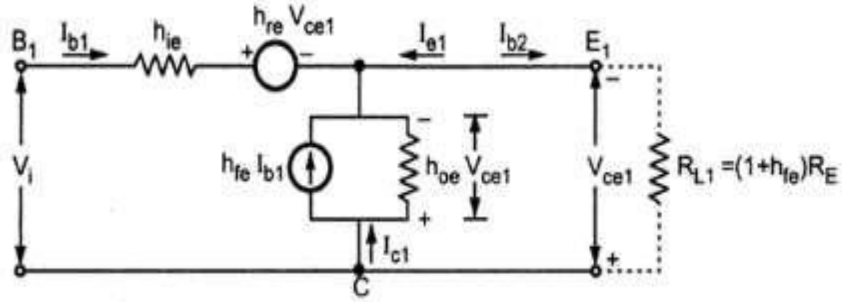


Fig. 2.63

a) Current Gain (A_{i1}) :

$$A_{i1} = \frac{I_{b2}}{I_{b1}}$$

$$A_{i1} = \frac{I_{e1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{c1}) \qquad \ldots (4)$$

and $$I_{c1} = h_{fe}I_{b1} + h_{oe} V_{ce1} = h_{fe}I_{b1} + h_{oe} (-I_{b2} R_{L1}) = h_{fe}I_{b1} + h_{oe} I_{e1} R_{L1}$$

Substituting value of I_{c1} equation 4 we get,

$$\therefore \quad I_{e1} = -(I_{b1} + h_{fe}I_{b1} + h_{oe} I_{e2} R_{L1}) = -I_{b1} - h_{fe}I_{b1} - h_{oe} I_{e1}R_{L1}$$

$$\therefore \quad I_{e1} + h_{oe} R_{L1} I_{e1} = -I_{b1} (1 + h_{fe})$$

$$-\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe} R_{L1}}$$

We know that, $R_{L1} = (1 + h_{fe}) R_E$

$$\therefore \quad \boxed{A_{i1} = -\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe}) R_E}} \qquad \ldots (5)$$

$$= \frac{1+h_{fe}}{1+h_{oe} h_{fe} R_E} \quad \because h_{fe} >> 1$$

b) Input Resistance (R_i) : $$R_{i1} = \frac{V_i}{I_{b1}}$$

Applying KVL to output loop we get,

$$V_i - I_{b1} h_{ie} - h_{re}V_{ce1} + V_{ce1} = 0$$

$$\therefore V_i = I_{b1}h_{ie} + h_{re} V_{ce1} - V_{ce1}$$

The terms $h_{re} V_{ce1}$ is negligible since h_{re} is in the order of 2.5×10^{-4}

$$= I_{b1}h_{ie} - (-I_{b2}R_{L1}) = I_{b1}h_{ie} + I_{b2}R_{L1}$$

$$\therefore R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{I_{b2}}{I_{b1}} R_{L1} = h_{ie} + A_{i1}R_{L1}$$

$$\therefore \quad \boxed{R_{i1} = h_{ie} + A_{i1}(1 + h_{fe}) R_E} \quad \text{... (6)}$$

Substituting value of A_{i1} we get,

$$R_{i1} = \frac{V_i}{I_{b1}} = h_{ie} + \frac{(1+h_{fe})(1+h_{fe})R_E}{1+h_{oe}h_{fe}R_E}$$

$$\therefore \quad \boxed{R_{i1} = h_{ie} + \frac{(1+h_{fe})^2 R_E}{1+h_{oe}h_{fe}R_E}} \quad \text{... (7)}$$

$$\therefore \quad \boxed{R_{i1} \approx \frac{(1+h_{fe})^2 R_E}{1+h_{oe}h_{fe}R_E}} \quad \because h_{ie} << \frac{(1+h_{fe})^2 R_E}{1+h_{oe}h_{fe}R_E} \quad \text{... (8)}$$

Overall Current Gain (A_i)

$$A_i = A_{i1} \times A_{i2} \quad \text{... (9)}$$

$$= \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_E} \times (1 + h_{fe})$$

$$\therefore \quad \boxed{A_i = \frac{(1+h_{fe})^2}{1+h_{oe}(1+h_{fe})R_E}} \quad \text{... (10)}$$

Parameter	Single stage	Darlington
Input resistance	$R_i = (1 + h_{fe}) R_E = 168.3\ k\Omega$	$R_i = \frac{(1+h_{fe})^2 R_E}{1+h_{oe}(1+h_{fe})R_E} = 1.65\ M\Omega$
Current gain	$A_i = 1 + h_{fe} = 51$	$A_i = \frac{(1+h_{fe})^2}{1+h_{oe}(1+h_{fe})R_E} = 500$

Table 2.5

Table 2.5 shows the comparison of input impedance and current gain provided by the single stage amplifier and Darlington connection. It is assumed that $R_E = 3.3$ K and h-parameters are as follows :

$$h_{ie} = 1100,\ h_{re} = 2.5 \times 10^{-4},\ h_{fe} = 50 \text{ and } h_{oe} = 25\ \mu A/V$$

Look at figure in Table 2.5 we can say that Darlington connection improves input impedance as well as current gain of the circuit.

Overall Voltage Gain :

We know that, $A_v = \frac{A_i R_L}{R_i}$

By subtracting 1 on both sides we get

$$1 - A_v = 1 - \frac{A_i R_L}{R_i}$$

$$\therefore \quad 1 - A_v = \frac{R_i - A_i R_L}{R_i} = \frac{h_{ic} + h_{rc} A_i R_i - A_i R_L}{R_i}$$

$$= \frac{h_{ie}}{R_i} \text{ since } h_{ic} = h_{ie} \text{ and } h_{rc} = 1 - h_{re} \approx 1$$

$$\therefore \quad A_v = 1 - \frac{h_{ie}}{R_i} \qquad \text{... (11)}$$

We know that the overall voltage gain in multistage amplifier is a product of individual voltage gain.

$$\therefore \quad A_v = A_{v1} A_{v2} = \left(1 - \frac{h_{ie}}{R_{i1}}\right)\left(1 - \frac{h_{ie}}{R_{i2}}\right)$$

$$\therefore \quad \boxed{A_v = 1 - \frac{h_{ie}}{R_{i2}} - \frac{h_{ie}}{R_{i1}} + \frac{h_{ie}^2}{R_{i1} R_{i2}}}$$

As we know, input resistance $R_{i1} >> R_{i2}$ we can neglect term 3 and term 4 in the above equation.

$$\therefore \quad \boxed{A_v \approx 1 - \frac{h_{ie}}{R_{i2}}} \qquad \text{... (12)}$$

Output Impedance (R_{o2}) :

$$R_o = \frac{1}{\text{Output admittance}} = \frac{1}{Y_o}$$

From equation, Y_o of the transistor is given as

$$Y_o = Y_{o1} = h_{oc} - \frac{h_{fc} . h_{rc}}{h_{ic} + R_s} = h_{oe} - \frac{-(1 + h_{fe})}{h_{ie} + R_s}$$

Since $\quad h_{oc} = h_{oe},$

$$h_{fc} = -(1 + h_{fe})$$

and $\quad h_{ic} = h_{ie}$

$$Y_{o1} = h_{oe} + \frac{(1 + h_{fe})}{h_{ie} + R_s}$$

$$Y_{o1} = \frac{1 + h_{fe}}{h_{ic} + R_s} \qquad \text{... (13)}$$

$\because \qquad h_{oe} << \frac{(1+h_{fe})}{h_{ic}+R_s}$

$\therefore \qquad R_{o1} = \frac{1}{Y_{o1}}$

$$\therefore \qquad \boxed{R_{o1} = \frac{h_{ie1}+R_s}{1+h_{fe}}} \qquad \ldots (14)$$

Looking at Fig. 2.60 we can see that the R_{o1} of the first stage is the source resistance for second stage, i.e. $R_{s2} = R_{o1}$

$$\therefore \qquad R_{o2} = \frac{R_{s2}+h_{ie2}}{1+h_{fe}} = \frac{\left(\frac{h_{ie1}+R_s}{1+h_{fe}}\right)+h_{ie2}}{1+h_{fe}}$$

$$\therefore \qquad \boxed{R_{o2} = \frac{h_{ie1}+R_s}{(1-\ h_{fe})^2}+\frac{h_{ie2}}{1+h_{fe}}} \qquad \ldots (15)$$

Since the current in T_2 is $1+h_{fe}$ times the current in T_1, $h_{ie1} \approx (1+h_{fe})h_{ie2}$ substituting this value of h_{ie1} in equation 15 we get,

$$R_{o2} = \frac{(1+h_{fe})h_{ie2}+R_s}{(1+h_{fe})^2}+\frac{h_{ie2}}{1+h_{fe}} = \frac{h_{ie2}}{1+h_{fe}}+\frac{R_s}{(1+h_{fe})^2}+\frac{h_{ie2}}{1+h_{fe}}$$

$$\therefore \qquad \boxed{R_{o2} = \frac{R_s}{(1+h_{fe})^2}+\frac{2h_{ie2}}{(1+h_{fe})}}$$

Key Point:

1. *In above analysis we have assumed that the h-parameter of T_1 and T_2 are identical.*
2. *From the above analysis we have seen that Darlington connection of two transistor improves current gain and input resistance of the circuit.*

One might think that by connection of one more stage there will be further improvement in the input impedance and current gain. But unfortunately this is not possible because of the following two reasons :

1. In Darlington connection of two transistors, emitter of the first transistor is directly connected to the base of the second transistor. Because of direct coupling d.c. output current of the first stage is $(1 + h_{fe})\ I_{b1}$. If Darlington connection for n transistor is considered, then due to direct coupling the d.c. output current for last stage is $(1+h_{fe})^n$ times I_{b1}. Due to very large amplification factor even two stage Darlington connection has large output current and output stage may have to be a power stage. As power amplifiers are not used in the amplifier circuits it is not possible to use more than two transistors in the Darlington connection.

2. In Darlington transistor connection, the leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high, which is not desired.

Example 2.8 : *For circuit shown in Fig. 2.64.*
Calculate R_i, A_i, A_v and R_o

h_{ie} = 1.1 K , h_{fe} = 50, $h_{re} = 2.5 \times 10^{-4}$, h_{oe} = 25 µA/V

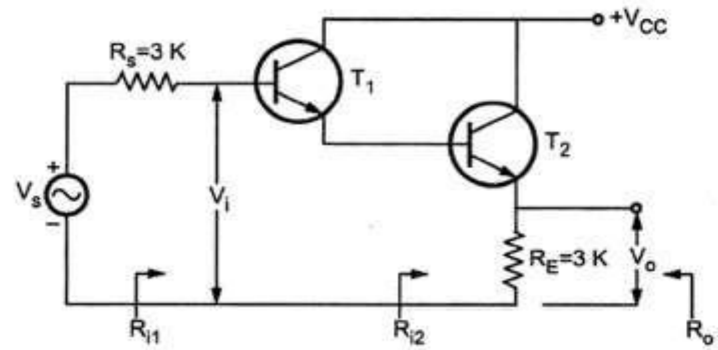


Fig. 2.64

Solution : We can use approximate analysis method because

$$h_{oe} R_L = 25\times10^{-6}\times3\times10^3 < 0.1.$$

Analysis for second stage

a) Current gain (A_{i2}) : $A_{i2} = 1 + h_{fe} = 1 + 50 = 51$

b) Input resistance (R_{i2}) : $R_{i2} = h_{ie} + (1 + h_{fe}) R_E = 1.1 \times 10^3 + (1 + 50)\, 3 \times 10^3$

$$= 154.1 \text{ k}\Omega$$

c) Voltage gain (A_{v2}) : $A_{v2} = 1 - \dfrac{h_{ie}}{R_{i2}} = 1 - \dfrac{1.1\times10^3}{154.1\times10^3} = 0.9928$

Analysis for first stage :

Here, we cannot use approximate analysis because

$h_{oe} R_L = h_{oe} R_E = h_{oe} R_{i2} = 25 \times 10^{-6} \times 154.1 \times 10^3 = 3.8525$ which is not less than 0.1. Hence use exact analysis.

a) Current gain (A_{i1}) : Here $R_E = R_{i2} = 154.1$ K

$$A_{i1} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_{i2}} = \frac{1+50}{1+25\times10^{-6}(1+50)\times154.1\text{K}}$$

$$= 0.258$$

b) Input resistance (R_{i1}) : $R_{i1} = h_{ie}+A_{i1}(1 + h_{fe}) R_E = 1.1 \times 10^3 + 0.258\,(1 + 50) \times 154.1$ K

$$= 2.02 \text{ M}\Omega$$

c) Voltage gain (A_{v1}): $A_{v1} = 1 - \dfrac{h_{ie}}{R_{i1}} = 1 - \dfrac{1.1\times10^3}{2.02\times10^6} = 0.999$

Overall voltage gain (A_v)

$$A_v = A_{v1} A_{v2} = 0.999 \times 0.9928 = 0.9918$$

Output resistance (R_o)

$$R_{o1} = \frac{h_{ie} + R_s}{1 + h_{fe}} = \frac{1.1 \times 10^3 + 3 \times 10^3}{1 + 50} = 80.39\ \Omega$$

$$R_{o2} = \frac{h_{ie} + R_{s2}}{1 + h_{fe}} = \frac{h_{ie} + R_{o1}}{(1 + h_{fe})^2} \qquad \because R_{s2} = R_{o1}$$

$$= \frac{1.1 \times 10^3 + 80.39}{(1 + 50)} = 23.145\ \Omega$$

$$R_o = R_{o2} \parallel R_L = 23.145 \parallel \times 10^3 = 22.96\ \Omega$$

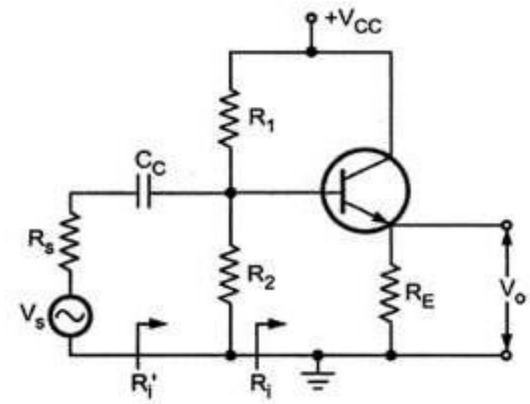


Fig. 2.65 Typical emitter follower amplifier with biasing arrangement

In above discussion of Darlington transistors, we have emphasized its value in providing high input impedance. However, we have simplified the problem by disregarding the effect of the biasing arrangements used in the circuit. Fig. 2.65 shows the typical biasing circuit. The biasing network consists of R_1 and R_2 which appear parallel with the input impedance of the amplifier. Therefore, effective input impedance $R_i' = R_1 \parallel R_2 \parallel R_i$ of the amplifier is very much decreased and the advantage of high input impedance is reduced.

We know that, biasing resistances cannot be avoided. But by modifying the circuit their shunting effect can be avoided. In the following section we still study the circuit called bootstrap, used to overcome the decrease in the input resistance due to the biasing network.

2.12.3 Bootstrap Emitter Follower

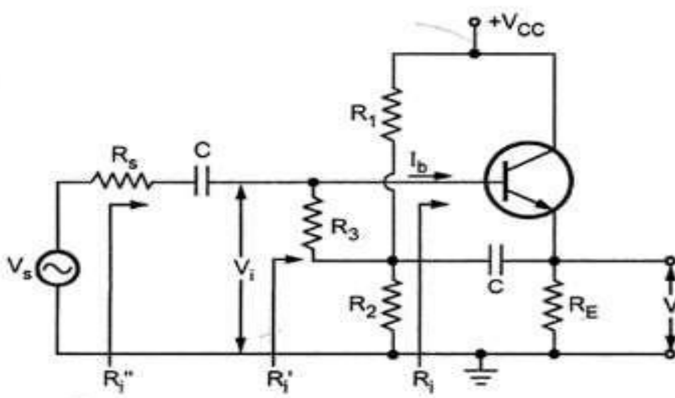


Fig. 2.68 Bootstrap emitter follower

We have seen that, in emitter follower, the input resistance of the amplifier is reduced because of the shunting effect of the biasing resistors. To overcome this problem the emitter follower circuit is modified, as shown in the Fig. 2.68.

Here, two additional components are used, resistance R_3 and capacitor C. The capacitor, is connected between the emitter and the junction of R_1, R_2 and R_3.

For d.c. signal, capacitor C acts as a open circuit and therefore resistance R_1, R_2 and R_3 provides necessary biasing to keep transistor in the active region.

For a.c. signal, the capacitor acts as a short circuit. Its value is chosen such that it provides very low reactance nearly short circuit at lowest operating frequency. Hence, for a.c., the bottom of R_3 is effectively connected to the output (the emitter), whereas the top of R_3 is at the input (the base). In other words, R_3 is connected between input node and output node. For such connection effective input resistance is given by the Miller's theorem. Refer section (2.9.1). The theorem says that the impedance between the two nodes can be resolved into two components, one from each node to ground. The two components are :

$$\frac{Z}{1-K} \quad \text{and} \quad \frac{Z \cdot K}{K-1}$$

In our case R_3 is the impedance between output voltage and input voltage and K is the voltage gain $V_o / V_i = A_v$

Fig. 2.69 shows the bootstrap circuit with two resolved components of R_3 using Miller's theorem. (See Fig. 2.69 on next page.)

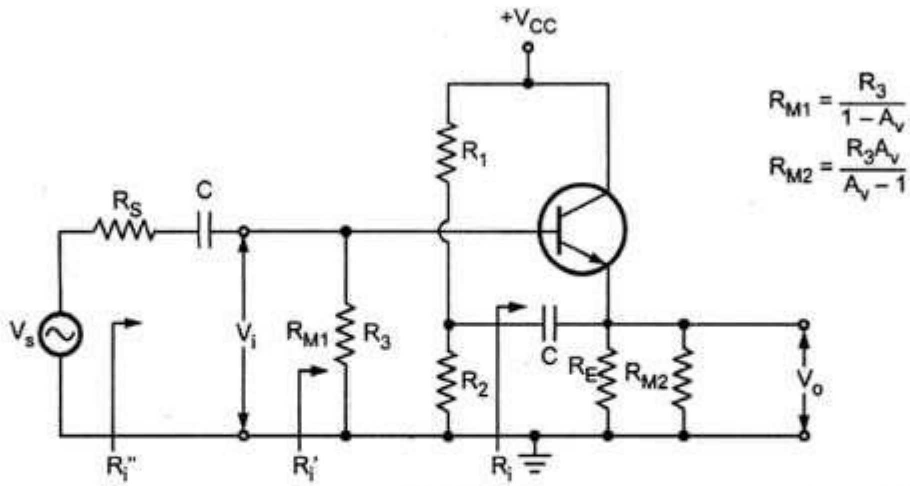


Fig. 2.69

These are

$$R_{M1} = \frac{R_3}{1-A_v} \quad \text{and} \quad R_{M2} = \frac{R_3 A_v}{A_v - 1}$$

Since, for an emitter follower, A_v approaches unity, then R_{M2} becomes extremely large. For example, with $A_v = 0.99$ and $R_3 = 200$ K, we find $R_{M2} = 20$ M.
The R_i' for the circuit shown in Fig. 2.70 can be given as

$$R_i' = R_i \parallel R_M$$

where $R_i = h_{ie} + (1 + h_{fe}) R_E$ for emitter follower.

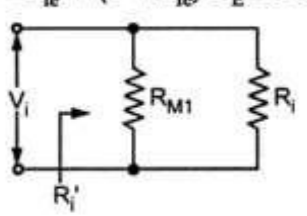


Fig. 2.70

The above effect, when $A_v \to 1$, is called **bootstrapping**. The name arises from the fact that, if one end of the resistor R_3 changes in voltage, the other end of R_3 moves through the same potential difference; it is as if R_3 is pulling itself up by its bootstraps.

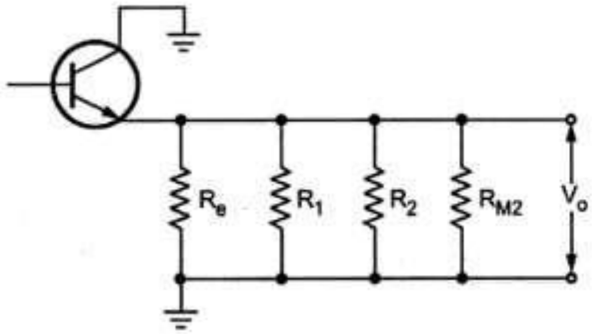


Fig. 2.71

The effective load on the emitter follower can be given as

$$R_{L\,eff} = R_E \parallel R_1 \parallel R_2 \parallel R_{M2}$$

Because of the capacitor, biasing resistances R_1 and R_2 come on output side shunting effective load resistance. The resistance R_{M2} is very large and hence it is often neglected.

$$\therefore \quad R_{L\,eff} = R_E \parallel R_1 \parallel R_2$$

Example 2.9 : *For the circuit shown in Fig. 2.72 calculated $R_{L\,eff}$, R_i and R_i'*

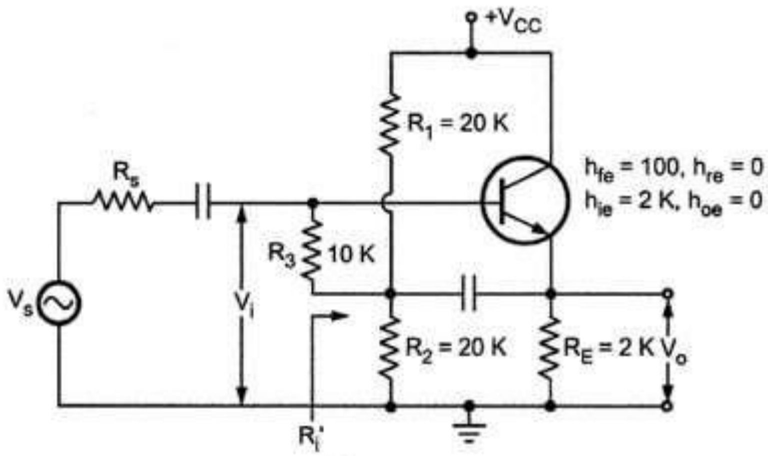


Fig. 2.72

Solution : Here, $R_{Leff} = R_1 \parallel R_2 \parallel R_E = 20\text{ K} \parallel 20\text{ K} \parallel 2\text{ K} = 1.67\text{ k}\Omega$

$$R_i = h_{ie} + (1 + h_{fe})\, R_{L\,eff} = 2 \times 10^3 + (1 + 100) \times 1.67 \times 10^3 = 170.67\text{ k}\Omega$$

$$R_i' = R_i \parallel \frac{R_3}{1 - A_v}$$

where $$A_v = 1 - \frac{h_{ie}}{R_i} = 1 - \frac{2 \times 10^3}{170.67 \times 10^3} = 0.988$$

$$\therefore \quad R_i' = 170.67 \times 10^3 \parallel \frac{10 \times 10^3}{1 - 0.988} = 170.67 \times 10^3 \parallel 833.33 \times 10^3 = 141.66\text{ k}\Omega$$

11.10 FREQUENCY RESPONSE OF MULTISTAGE AMPLIFIERS

For a second transistor stage connected directly to the output of the first stage, there will be significant change in the overall frequency response. There will be additional low frequency cut-off levels due to the second stage that will further reduce the overall gain of the system in this region. For each additional stage, the upper cut-off frequency will be determined primarily by the stage having the lowest high frequency cut-off frequency. The low frequency cut-off is primarily determined by that stage having the highest low frequency cut-off frequency. Hence one poorly designed stage can off set an otherwise well designed cascaded system.

The effect of increasing the number of identical stages, having the same lower and upper cut-off frequencies, can be clearly demonstrated by considering Fig. 11.32.

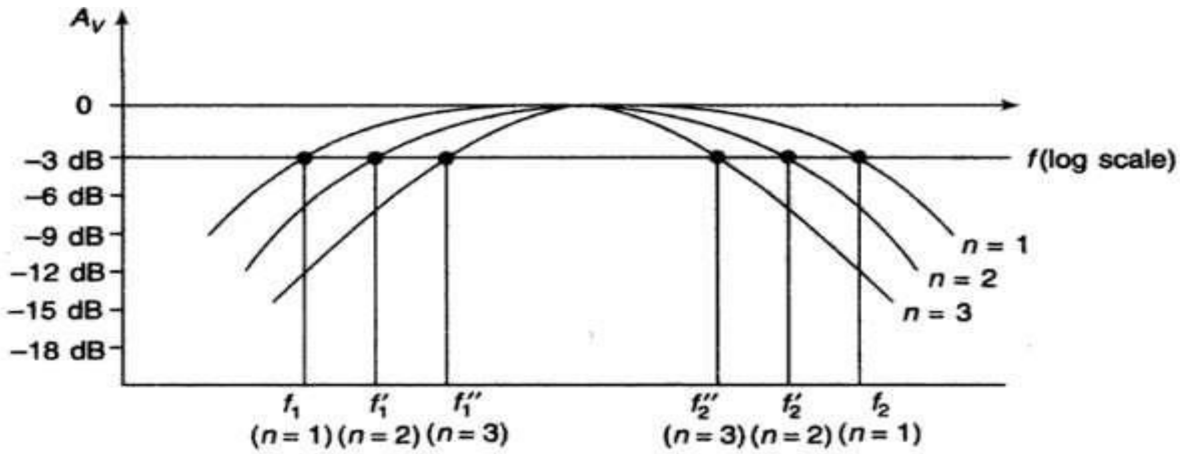


Fig. 11.32 Effect of an increased number of stages on the cut-off frequencies and bandwidth

For a single stage the cut-off frequencies are f_1 and f_2 as indicated. For two identical stages in cascade, the drop off rate in the low and high frequency regions has increased to −12 dB/octave or −40 dB per decade At f_1 and f_2, therefore, the decibel drop is now −6 dB, rather than the defined band frequency gain level of −3 dB. The −3 dB point has shifted to f_1' and f_2' as indicated, with a resulting drop in the bandwidth. A −18 dB/octave or −60 dB/decade slope will result for a three stage system of identical stages with indicated reduction in bandwidth (f_1'' and f_2'').

Assuming identical stages, an equation for each band frequency as a function of the number of the stages (n) can be determined in the following manner.
For the low frequency region,

$$A_{v\text{low(overall)}} = A_{v1\text{ low}}\, A_{v2\text{ low}}\, A_{v3\text{ low}} \cdots A_{vn\text{ low}}$$

As each stage is identical,

$$A_{v1\text{ low}} = A_{v2\text{ low}} = \ldots = A_{vn\text{ low}}$$

Therefore, $A_{v\text{ low(overall)}} = (A_{v\text{ low}})^n$

$$A_{v\text{ low}}/A_{V\text{ mid}}\text{ (overall)} = (A_{V\text{ low}}/A_{V\text{ mid}})^n$$
$$= 1/[1 - j(f_1/f)]^n$$

Setting the magnitude of the result equal to $1/\sqrt{2}$ (−3 dB level) results in

$$1/\sqrt{[1 + (f_1/f_1')^2]^n} = 1/\sqrt{2}$$

UNIT II
HIGH FREQUENCY RESPONSE OF A TRANSISTOR

Transistor at High frequencies:

The **low frequency small signal model** of bipolar junction transistor crudely holds for frequencies below 1 MHz. For frequencies greater than 1 MHz the response of the transistor will be limited by internal and parasitic capacitance's of the bipolar junction transistor. Hence at high frequencies the **low frequency small signal model of transistor** has to be modified to include the effects of internal and parasitic capacitance's of bipolar junction transistor. These capacitance's limit the usage of BJT at higher frequencies. Thus in order to estimate the gain and switching on and off times of BJT at higher frequencies the **high frequency model of BJT** has to be used to get reasonably accurate estimates. The **high frequency hybrid pi model** is also called as Giacoletto model named after **L.J.Giacoletto** who introduced it in 1969.

High frequency effects on BJT:

- The gain decreases at high frequencies due to internal feedback capacitance's. The highest frequency of operation of BJT will be limited by internal capacitance's of BJT.
- The on and off switching times of BJT will be high and speed will be limited due to internal charge storage effects.

High frequency model of BJT:

The high frequency parameters of BJT may vary with operating point but the variation is negligible for small signal variations around the operating point. Following is the high frequency model of a transistor.

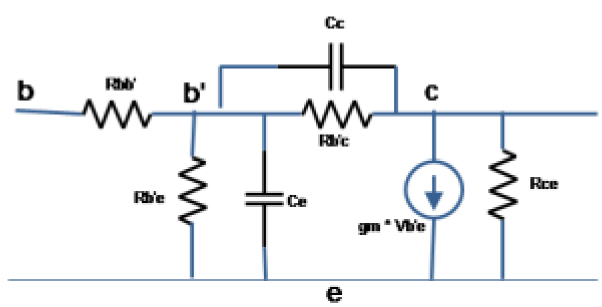


Fig: High Frequency Model of BJT

Where

B' = internal node in base

$R_{bb'}$ = Base spreading resistance

$R_{b'e}$ = Internal base node to emitter resistance

R_{ce} = collector to emitter resistance

C_e = Diffusion capacitance of emitter base junction

$R_{b'c}$ = Feedback resistance from internal base node to collector node

g_m = Transconductance

C_C= transition or space charge capacitance of base collector junction.

Transistors at High Frequencies

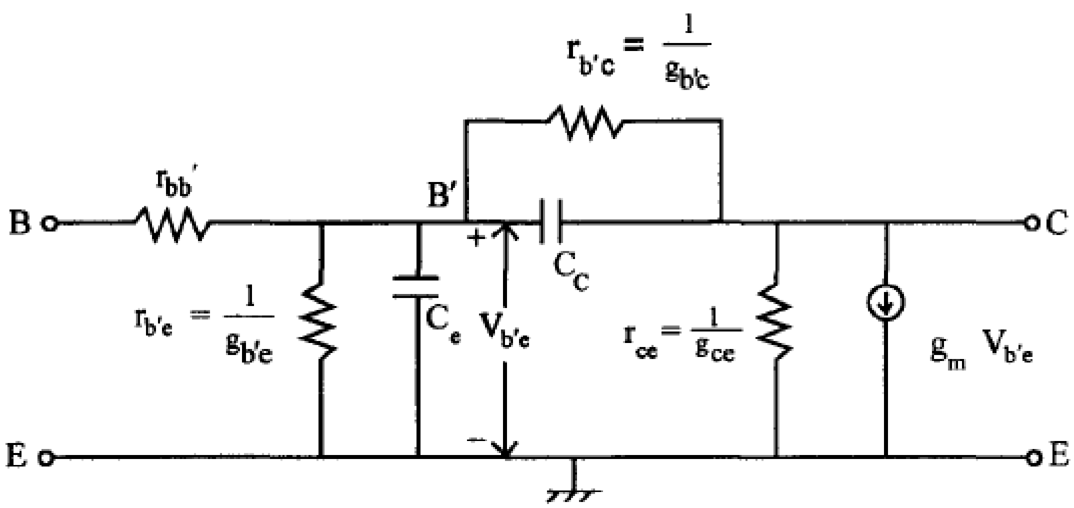
At low frequencies it is assumed that transistor responds instantaneously to changes in the input voltage or current i.e., if you give AC signal between the base and emitter of a Transistor amplifier in Common Emitter configuraii6n and if the input signal frequency is low, the output at the collector will exactly follow the change in the input (amplitude etc.,). If '1' of the input is high (MHz) and the amplitude of the input signal is changing the Transistor amplifier will not be able to respond.

It is because; the carriers from the emitter side will have to be injected into the collector side. These take definite amount of time to travel from Emitter to Base, however small it may be. But if the input signal is varying at much higher speed than the actual time taken by the carries to respond, then the Transistor amplifier will not respond instantaneously. Thus, the junction capacitances of the transistor, puts a limit to the highest frequency signal which the transistor can handle. Thus depending upon doping area of the junction etc, we have transistors which can respond in AF range and also RF range.

To study and analyze the behavior of the transistor to high frequency signals an equivalent model based upon transmission line equations will be accurate. But this model will be very complicated to analyze. So some approximations are made and the equivalent circuit is simplified. If the circuit is simplified to a great extent, it will be easy to analyze, but the results will not be accurate. If no approximations are made, the results will be accurate, but it will be difficult to analyze. The desirable features of an equivalent circuit for analysis are simplicity and accuracy. Such a circuit which is fairly simple and reasonably accurate is the Hybrid-pi or Hybrid-π model, so called because the circuit is in the form of π.

Hybrid - π Common Emitter Transconductance Model

For Transconductance amplifier circuits Common Emitter configuration is preferred. Why? Because for Common Collector (hrc< 1). For Common Collector Configuration, voltage gain Av < 1. So even by cascading you can't increase voltage gain. For Common Base, current gain is hib< 1. Overall voltage gain is less than 1. For Common Emitter, hre>>1. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used. The Hybrid-x or Giacoletto Model for the Common Emitter amplifier circuit (single stage) is as shown below



Analysis of this circuit gives satisfactory results at all frequencies not only at high frequencies but also at low frequencies. All the parameters are assumed to be independent of frequency.

Where B' = internal node in base

$r_{bb'}$ = Base spreading resistance

$r_{b'e}$ = Internal base node to emitter resistance

r_{ce} = collector to emitter resistance

C_e = Diffusion capacitance of emitter base junction

$r_{b'c}$ = Feedback resistance from internal base node to collector node

g_m = Transconductance
C_C= transition or space charge capacitance of base collector junction

Circuit Components

B' is the internal node of base of the Transconductance amplifier. It is not physically accessible. The base spreading resistance rbb is represented as a lumped parameter between base B and internal node B'. $g_{mVb'e}$ is a current generator. Vb'e is the input voltage across the emitter junction. If Vb'e increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is proportional to Vb'e. This results in small signal current since we are taking into account changes in Vb'e. This effect is represented by the current generator g_mVb'e. This represents the current that results because of the changes in Vb'e' when C is shorted to E.

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by gb'e. As recombination increases, base current increases. Minority carrier storage in the base is represented by C_e the diffusion capacitance.

According to Early Effect, the change in voltage between Collector and Emitter changes the base width. Base width will be modulated according to the voltage variations between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. I_E changes and I_C changes. This feedback effect [IE on input side, I_C on output side] is taken into account by connecting gb'e between B', and C. The conductance between Collector and Base is g_{ce}.C_c represents the collector junction barrier capacitance.

Hybrid - *n* Parameter Values

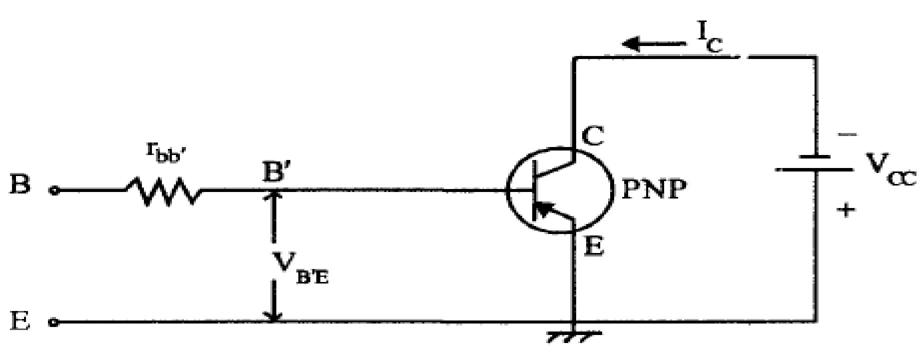
Typical values of the hybrid-n parameter at I_C = 1.3 rnA are as follows:

g_m= 50 mA/v
rbb' = 100 Ω
rb'e = 1 kΩ
ree = 80 kΩ
Cc = 3 pf
Ce = 100 pf
rb'c = 4 MΩ

These values depend upon:
1. Temperature 2. Value of I_C

Determination of Hybrid-x Conductances

1. Transconductance or Mutual Conductance (g_m)



The above figure shows PNP transistor amplifier in Common Emitter configuration for AC purpose, Collector is shorted to Emitter.

$$I_C = I_{C0} - \alpha_0 \cdot I_E$$

I_{CO} opposes I_E. I_E is negative. Hence $I_C = I_{CO} - \alpha_0 IE$ α_0 is the normal value of α at roomtemperature.

In the hybrid - π equivalent circuit, the short circuit current = $g_m Vb'$ e

Here only transistor is considered, and other circuit elements like resistors, capacitors etc,are not considered.

$$g_m = \left. \frac{\partial I_C}{\partial V_{b'e}} \right|_{V_{CE} = K}$$

Differentiate (l) with respect to Vb'e partially. I_{CO} is constant

$$g_m = 0 - \alpha_0 \frac{\partial I_E}{\partial V_{b'e}}$$

For a PNP transistor, Vb'e = $-V_E$Since, for PNP transistor, base is n-type. So negative voltage is given

$$g_m = \alpha_0 \frac{\partial I_E}{\partial V_E}$$

If the emitter diode resistance is r_e then

$$r_e = \frac{\partial V_E}{\partial I_E}$$

$$g_m = \frac{\alpha_0}{r_e}$$

$$r = \frac{\eta . V_T}{I} \quad \eta = 1, \qquad I = I_E \qquad r = \frac{V_T}{I_E}$$

$$g_m = \frac{\alpha_0 . I_E}{V_T} \qquad \alpha_0 \simeq 1, \qquad I_E \simeq I_C$$

$$I_E = I_{C0} - I_C$$

$$g_m = \frac{I_{C0} - I_C}{V_T}$$

Neglect I_{C0}

$$g_m = \frac{|I_C|}{V_T}$$

g_m is directly proportiortal to I_C is also inversely proportiortal to T. For PNP transistor, I_C is negative

$$\boxed{g_m = \frac{-I_C}{V_T}}$$

At room temperature i.e. $T=300^0K$

$$g_m = \frac{|I_C|}{26}, \; I_C \text{ is in mA.}$$

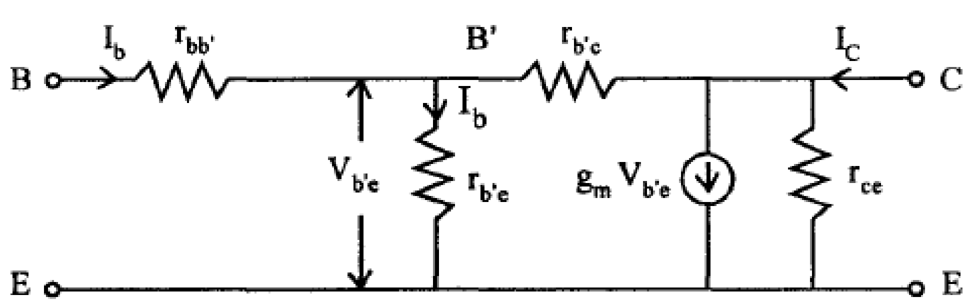
If $\qquad I_C = 1.3$ mA, $g_m = 0.05$ A/V

If $\qquad I_C = 10$ mA, $g_m = 400$ mA/V

Input Conductance (gb'e):

At low frequencies, capacitive reactance will be very large and can be considered as Open circuit. Soin the hybrid-π equivalent circuit which is valid at low frequencies, all the capacitances can be neglected.

The equivalent circuit is as shown in Fig.



The value of rb'c» rb'e (Since Collector Base junction is Reverse Biased)So I_b flows into rb'e only. [This is lb' (IE - I_b)will go to collector junction]

$$V_{b'e} \simeq I_b . r_{b'e}$$

The short circuit collector current,

$$I_C = g_m \cdot V_{b'e}; \qquad V_{b'e} = I_b \cdot r_{b'e}$$

$$I_C = g_m \cdot I_b \cdot r_{b'e}$$

$$h_{fe} = \left.\frac{I_C}{I_B}\right|_{V_{CE}} = g_m \cdot r_{b'e}$$

$$\boxed{r_{b'e} = \frac{h_{fe}}{g_m}}$$

$$g_m = \frac{|I_C|}{V_T}$$

$$r_{b'e} = \frac{h_{fe} \cdot V_T}{|I_C|}$$

$$g_{b'e} = \boxed{\frac{|I_C|}{h_{fe} V_T}} \text{ or } \boxed{\frac{g_m}{h_{fe}}}$$

Feedback Conductance ($g_{b'c}$)

hre = reverse voltage gain, with input open or $I_b = 0$

hre =Vb'e/Vce = Input voltage/Output voltage

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

[With input open, i.e., $I_b - 0$, V_{ce} is output. So it will get divided between $r_{b'e}$ and $r_{b'c}$ only]

or $\quad h_{re}(r_{b'e} + r_{b'c}) = r_{b'e}$

$\quad r_{b'e}[1 - h_{re}] = h_{re} r_{b'c}$

But $\quad h_{re} << 1$

$\therefore \quad r_{b'e} = h_{re} \; r_{b'c}; \quad r_{b'c} = \frac{r_{b'e}}{h_{re}}$

or $\quad \boxed{g_{b'c} = h_{re} \; g_{b'e}} \quad \frac{1}{r_{b'c}} = g_{b'c} = \frac{h_{re}}{r_{b'e}}$

$\quad h_{re} = 10^{-4}$

$\therefore \quad r_{b'c} >> r_{b'e}$

Base Spreading Resistance (r bb')

The input resistance with the output shorted is hie. If output is shorted, i.e., Collector and Emitter arejoined; $r_{b'e}$ is in parallel with $r_{b'c}$.

$$h_{ie} = r_{bb'} + r_{b'e}$$

$$\boxed{r_{bb'} = h_{ie} - r_{b'e}}$$

$$h_{ie} = r_{bb'} + r_{b'e}$$

$$r_{b'e} = \frac{h_{fe}.V_T}{|I_C|}$$

$$h_{ie} = r_{bb'} + \frac{h_{fe}.V_T}{|I_C|}$$

Output Conductance (g_{ce})

This is the conductance with input open circuited. In h-parameters it is represented as hoe. For I_b= 0, we have,

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m \ V_{b'e}$$

$$h_{re} = \frac{V_{b'e}}{V_{ce}} \qquad \therefore \qquad V_{b'e} = h_{re}.\ V_{ce}$$

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m.\ h_{re}.V_{ce}$$

$$h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m \cdot h_{re}$$

$$= g_{ce} + g_{b'c} + g_m\, h_{re}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$g_m = g_{b'e} \cdot h_{fe}$$

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \approx \frac{r_{b'e}}{r_{b'c}} = \frac{g_{b'c}}{g_{b'e}}$$

$$h_{oe} = g_{ce} + g_{b'c} + g_{b'e}\, h_{fe} \cdot \frac{g_{b'c}}{g_{b'e}}$$

$$g_{ce} = h_{oe} - (1 + h_{fe}) \cdot g_{b'c}$$

$$h_{fe} >> 1, \quad 1 + h_{fe} \approx h_{fe}$$

$$\boxed{g_{ce} = h_{oe} - h_{fe} \cdot g_{b'c}}$$

$$g_{b'c} = h_{re} \cdot g_{b'e}$$

$$g_{ce} = h_{oe} - h_{fe} \cdot h_{re} \cdot g_{b'e}$$

Hybrid - π Capacitances

In the hybrid - **π** equivalent circuit, there are two capacitances, the capacitance between the Collector Base junction is the C_c or $C_{b'e}$'. This is measured with input open i.e., $I_E = 0$, and is specified by the manufacturers as C_{Ob}. 0 indicates that input is open. Collector junction is reverse biased.

$$C_C \,\alpha\, \frac{1}{(V_{CE})^n}$$

$$n = \frac{1}{2} \quad \text{for abrupt junction}$$

$$= 1/3 \quad \text{for graded junction.}$$

C_e = Emitter diffusion capacitance C_{De} + Emitter junction capacitance C_{Te}

C_T = Transition capacitance.

C_D = Diffusion capacitance.

$C_{De} >> C_{Te}$

$C_e \simeq C_{De}$

$C_{De}\ \alpha\ I_E$ and is independent of Temperature T.

Validity of hybrid-π model

The high frequency hybrid Pi or Giacoletto model of BJT is valid for frequencies less than the unit gain frequency.

High frequency model parameters of a BJT in terms of low frequency hybrid parameters

The main advantage of high frequency model is that this model can be simplified to obtain low frequency model of BJT. This is done by eliminating capacitance's from the high frequency model so that the BJT responds without any significant delay (instantaneously) to the input signal. In practice there will be some delay between the input signal and output signal of BJT which will be very small compared to signal period (1/frequency of input signal) and hence can be neglected. The high frequency model of BJT is simplified at low frequencies and redrawn as shown in the figure below along with the small signal low frequency hybrid model of BJT.

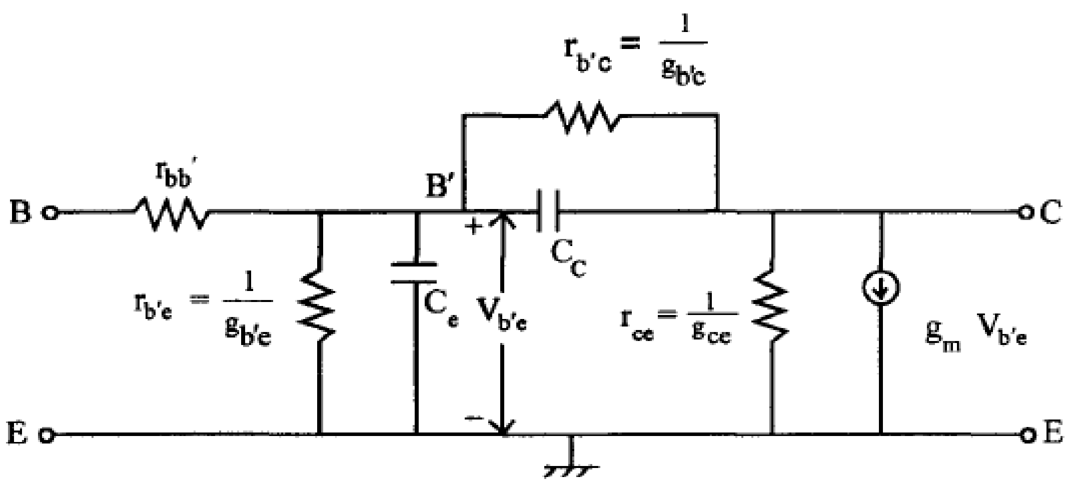


Fig. high frequency model of BJT at low frequencies

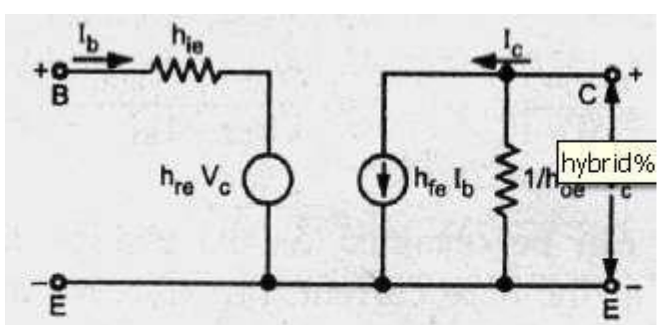


Fig hybrid model of BJT at low frequencies

The High frequency model parameters of a BJT in terms of low frequency hybrid parameters are given below:

Transconductance $g_m = I_c/V_t$

Internal Base node to emitter resistance $r_{b'e} = h_{fe}/ g_m = (h_{fe}* V_t)/ I_c$

Internal Base node to collector resistance $r_{b'e} = (h_{re}* r_{b'c}) / (1- h_{re})$ assuming $h_{re} << 1$ it reduces to $r_{b'e} = (h_{re}* r_{b'c})$

Base spreading resistance $r_{bb'} = h_{ie} – r_{b'e} = h_{ie} – (h_{fe}* V_t)/ I_c$

Collector to emitter resistance $r_{ce} = 1 / (h_{oe} – (1+ h_{fe})/r_{b'c})$

Collector Emitter Short Circuit Current Gain

Consider a single stage Common Emitter transistor amplifier circuit. The hybrid-1t equivalent circuit is as shown:

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

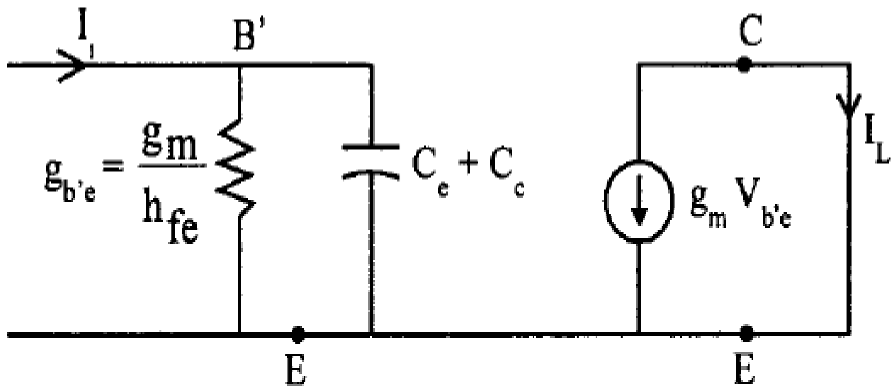
But $$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\,2\pi . g_m . f}{2\pi f_T}}$$

$$\therefore \quad A_i = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

If the output is shorted i.e. $R_L = 0$, what will be the flow response of this circuit? When$R_L = 0$, $V_o = 0$. Hence $A_v = 0$. So the gain that we consider here is the current gain I_L/Ic. The simplified equivalent circuit with output shorted is,



A current source gives sinusoidal current Ic. Output current or load current is IL· $g_{b'c}$ isneglected since $g_{b'c} \ll g_{b'e}$, g_{ce} is in shunt with short circuit R = 0. Therefore g_{ce} disappears. The current is delivered to the output directly through Ce and $g_{b'c}$ is also neglected since this will be very small.

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_I under short circuit condition is,

$$A_I = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But $$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\,2\pi.g_m.f}{2\pi f_T}}$$

∴ $$A_I = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

$$= \frac{-h_{fe}}{1 + j\, h_{fe}\left(\frac{f}{f_T}\right)}$$

$$A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_\beta}\right)}$$

$$\frac{f_T}{h_{fe}} = f_\beta$$

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

Where $$f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_C)}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$\therefore$ $$f_\beta = \frac{g_m}{h_{fe}\, 2\pi(Ce + C_c)}$$

At $f = f_\beta$, $A_i = \frac{1}{\sqrt{2}}$ $= 0.707$ of h_{fe}.

Current Gain with Resistance Load:

$$f_T = f_\beta \,.\, h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

Considering the load resistance R_L

$V_{b'e}$ is the input voltage and is equal to V_1

V_{ce} is the output voltage and is equal to V_2

$$K_2 = \frac{V_{ce}}{V_{b'e}}$$

This circuit is still complicated for analysis. Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

K = Voltage gain. It will be >> 1

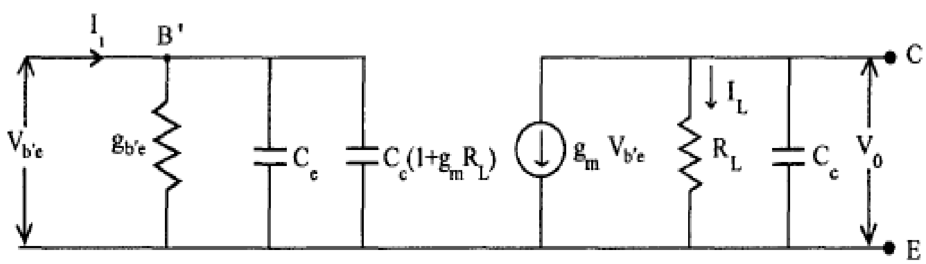
$$g_{b'c}\left(\frac{K-1}{K}\right) \simeq g_{b'c}$$

$$g_{b'c} < g_{ce} \quad \because \quad r_{b'c} \simeq 4\ M\Omega, \qquad r_{ce} = 80\ K \text{ (typical values)}$$

So $g_{b'c}$ can be neglected in the equivalent circuit. In a wide band amplifier RL will not exceed 2KΩ. If R_L is small f_H is large.

$$f_H = \frac{1}{2\pi C_S (R_C \parallel R_L)}$$

Thereforeg_{ce} can be neglected compared with R_L. Therefore the output circuit consists of current generator gm V $_{b'e}$ feeding the load R_L so the Circuit simplifies as shown in Fig.



$$K = \frac{V_{ce}}{V_{b'e}} = -g_m R_L; \quad g_m = 50\ mA\backslash V, \quad R_L = 2K\Omega \text{ (typical values)}$$

$$K = -100$$

Miller's Theorem

It states that if an impedance Z is connected between the input and output terminals, of a network, between which there is voltage gain, K, the same effect can be had by removing Z and connecting an impedance Z_i at the input =Z/(1-K) and Zo across the output = ZK/(K-1)

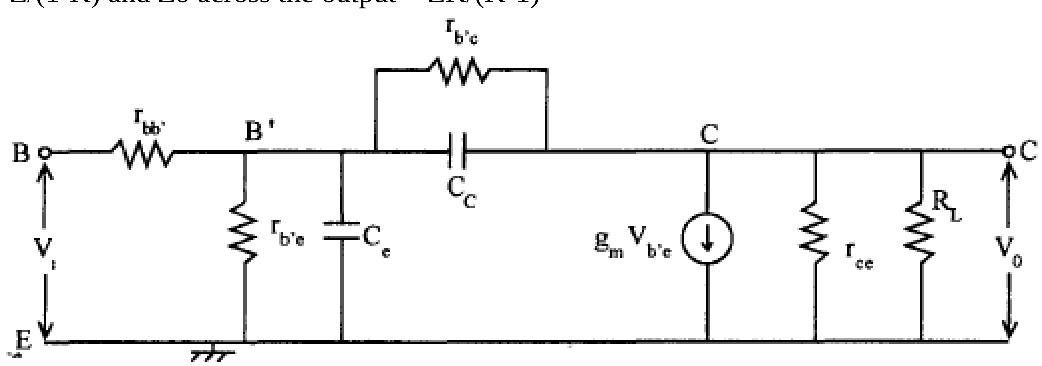


Fig. High frequency equivalent circuit with resistive load R_L

Therefore high frequency equivalent circuit using Miller's theorem reduces to

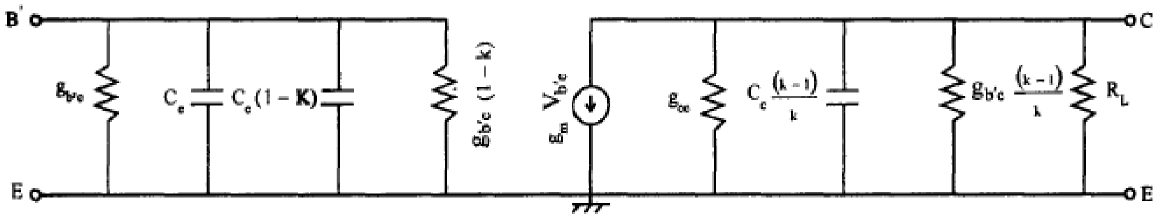


Fig. Circuit after applying Millers' Theorem

$$K = \frac{V_{ce}}{V_{b'e}}$$

$$V_{ce} = - I_c \cdot R_L$$

$$K = \frac{-I_C \cdot R_L}{V_{b'e}}$$

$$\frac{I_C}{V_{b'e}} = g_m$$

$$K = -g_m \cdot R_L$$

The Parameters f*T*

f_T is the frequency at which the short circuit Common Emitter current gain becomes unity.

The Parameters f*β*

$$A_i = 1, \quad \text{or} \quad \frac{h_{fe}}{\sqrt{1+\left(\frac{f_T}{f_\beta}\right)^2}} = 1$$

$$f = f_T, \quad A_i = 1$$

$$h_{fe} = \sqrt{1+\left(\frac{f_T}{f_\beta}\right)^2}$$

$$(h_{fe})^2 = 1 + \left(\frac{f_T}{f_\beta}\right)^2 \cong \left(\frac{f_T}{f_\beta}\right)^2$$

$$h_{fe} \simeq \frac{f_T}{f_\beta} \quad \text{when } Ai = 1$$

$$\boxed{f_T \simeq h_{fe} \cdot f_\beta}$$

$$f_\beta = \frac{g_m}{h_{fe}\{C_e + C_c\}}$$

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

$$C_e >> C_c$$

$$\boxed{f_T \simeq \frac{g_m}{2\pi C_e}}$$

$$A_i = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

Dividing by $g_{b'e}$, Numerator and Denominator,

$$A_i = \frac{-g_m / g_{b'e}}{1 + \frac{j2\pi f(C_e + C_c)}{g_{b'e}}}$$

we know that $g_{b'e} = \frac{g_m}{h_{fe}}$

$\therefore \quad \frac{g_m}{g_{b'e}} = h_{fe}$

$$A_i = \frac{-h_{fe}}{1 + jf\left[\frac{2\pi(C_e + C_C)}{g_{b'e}}\right]}$$

But we know that $A_i = \frac{-h_{fe}}{1 + j\frac{f}{f_\beta}}$

Comparing, $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe}.2\pi(C_e + C_c)} \quad \because \quad g_{b'e} = \frac{g_m}{h_{fe}}$

$$\therefore \quad \boxed{f_\beta = \frac{g_m}{h_{fe}.2\pi(C_e + C_c)}}$$

$$\boxed{f_T = \frac{g_m}{2\pi(C_e + C_c)}}$$

Gain - Bandwidth (B.W) Product

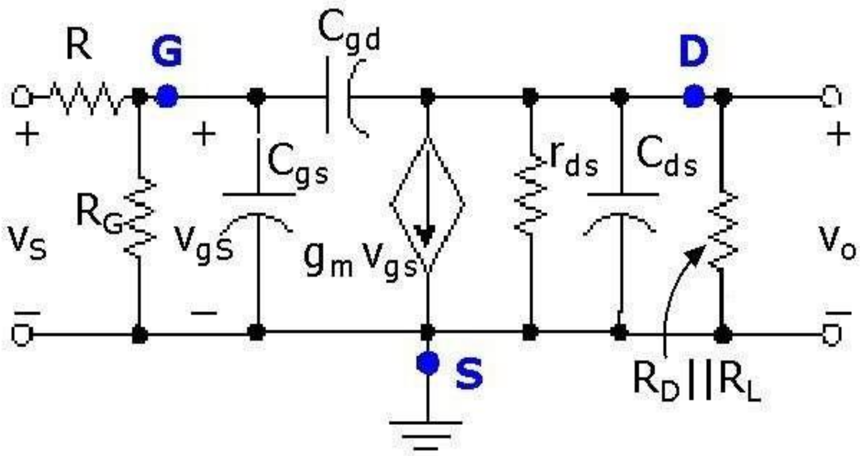
This is a measure to denote the performance of an amplifier circuit. Gain - B. W product is also referred as Figure of Merit of an amplifier. Any amplifier circuit must have large gain and large bandwidth. For certain amplifier circuits, the midband gain Am maybe large, but not Band width or Vice - Versa. Different amplifier circuits can be compared with thus parameter.

FET: Analysis of common Source and common drain Amplifier circuits at high frequencies.

Just like for the BJT, we could use the original small signal model for low frequency analysis–the only difference was that external capacitances had to be kept in the circuit. Also just like the BJT, for high frequency operation, the internal capacitances between each of the device’s terminals can no longer be ignored and the small signal model must be modified. Recall that for high frequency operation, we’re stating that external capacitances are so large (in relation to the internal capacitances) that they may be considered short circuits.

High frequency response of Common source amplifier

The JFET implementation of the common-source amplifier is given to the left below, and the small signal circuit in corporating the high frequency FET model is given to the right below. As stated above, the external coupling and bypass capacitors are large enough that we can model them as short circuits for high frequencies.



We may simplify the small signal circuit by making the following approximations and observations:

1. R_{ds} is usually larger than $R_D||R_L$, so that the parallel combination is dominated by $R_D||R_L$ and r_{ds} may be neglected. If this is not the case, a single equivalent resistance, $r_{ds}||R_D||R_L$ may be defined.
2. The Miller effect transforms C_{gd} into separate capacitances seen in the input and output circuits as

$$C_{M1} = C_{gd}(1 - A_v) \quad (input\ circuit)$$
$$C_{M2} = C_{gd}\left(1 - \frac{1}{A_v}\right) \quad (output\ circuit).$$

3. C_{ds} is very small, so the impedance contribution of this capacitance may be considered to be an open circuit and may be ignored.

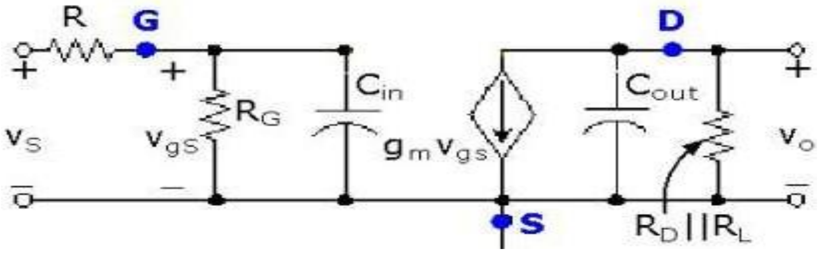
$$C_{in} = C_{gs} + C_{M1} = C_{gs} + C_{gd}(1 - A_v).$$

4. The parallel capacitances in the input circuit, C_{gs} and C_{M1}, may be combined to a single equivalent capacitance of value $C_{in} = C_{gs} + C_{M1} = C_{gs} + C_{gd}(1 - A_v)$.
5. Similarly, the parallel capacitances in the output circuit, C_{ds} and C_{M2}, may be combined to a single equivalent capacitance of value

$$C_{out} = C_{ds} + C_{M2} = C_{ds} + C_{gd}\left(1 - \frac{1}{A_v}\right),$$

Where $A_v = -g_m(R_D||R_L)$ for a common-source amplifier.

Setting the input source, v_S, equal to zero allows us to define the equivalent resistances seen by C_{in} and C_{out} (the Method of Open Circuit Time Constants). Note that, with $v_S=0$, the dependent current source also goes to zero (opens) and the input and output circuits are separated.



$$R_{Cin} = R \,||\, R_G \,.$$

$$R_{Cout} = R_D \,||\, R_L \,.$$

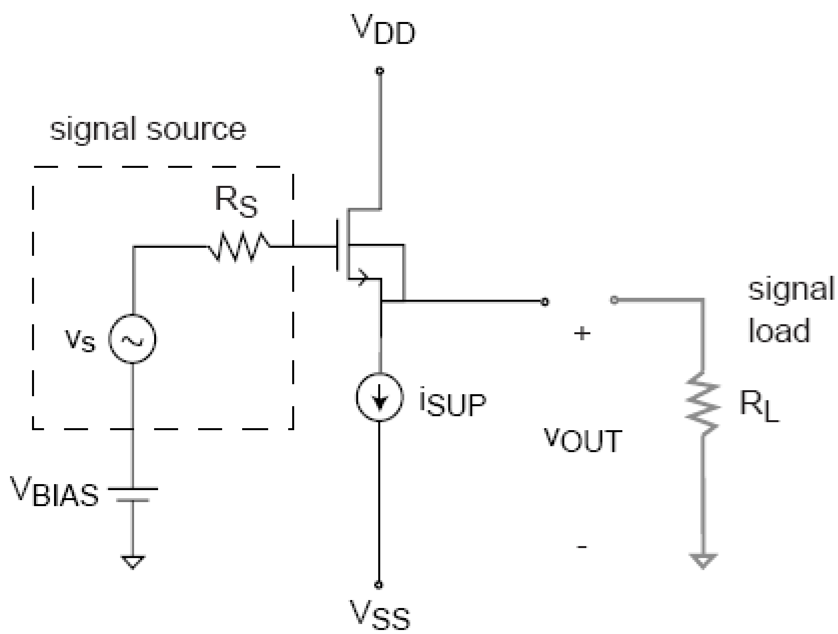
$$\tau_{Cin} = C_{in} R_{Cin}\,; \qquad \tau_{Cout} = C_{out} R_{Cout}\,,$$

$$\omega_H = \frac{1}{\dfrac{1}{\omega_{Cin}} + \dfrac{1}{\omega_{Cout}}} = \frac{1}{\tau_{Cin} + \tau_{Cout}} = \frac{1}{C_{in}R_{Cin} + C_{out}R_{Cout}} = \frac{1}{C_{in}(R\,||\,R_G) + C_{out}(R_D\,||\,R_L)}$$

Generally, the input is going to provide the dominant pole, so the high frequency cut off is given by

$$\omega_H = \frac{1}{C_{in}(R\,||\,R_G)}\,; \qquad f_H = \frac{\omega_H}{2\pi} = \frac{1}{2\pi C_{in}(R\,||\,R_G)}\,.$$

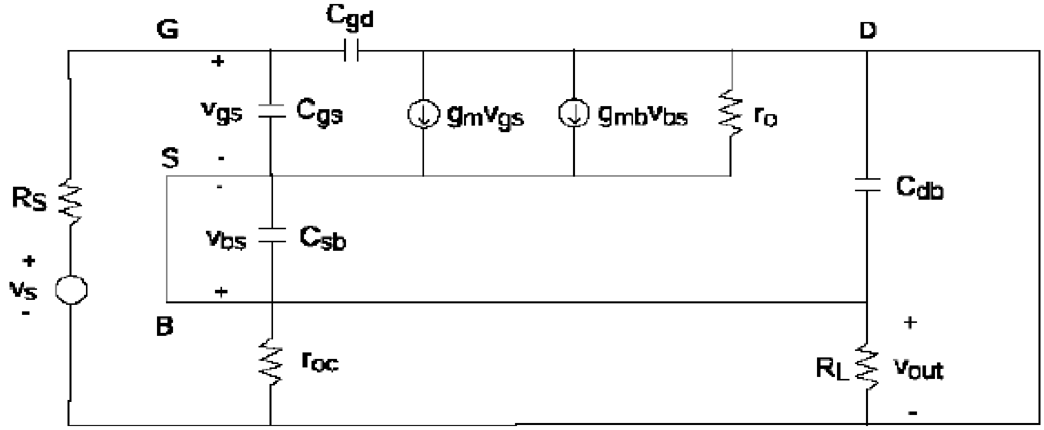
High frequency response of Common source amplifier



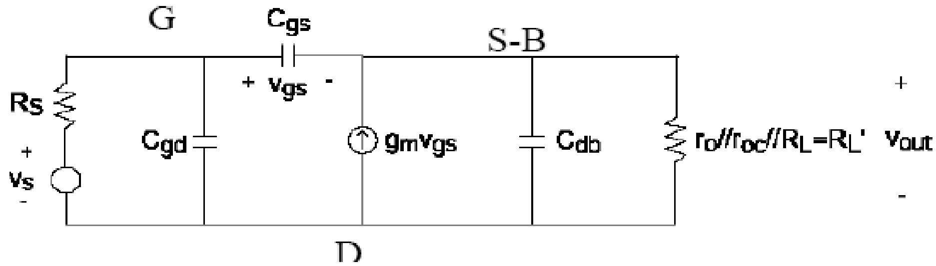
Characteristics ofCDAmplifier:

- Voltagegain ≈1
- Highinputresistance
- Lowoutputresistance
- Goodvoltage buffer

High frequency small signal model



$v_{bs}=0$



$$A_{vC_{gs}} = \frac{R_L}{R_{out} + R_L} = \frac{g_m R_L}{1 + g_m R_L}$$

$$C_M = C_{gs}\left(1 - A_{vC_{gs}}\right) = C_{gs}\left(1 - \frac{g_m R_L}{1 + g_m R_L}\right) = \frac{C_{gs}}{1 + g_m R_L}$$

$$C_T = C_{gs}\left(1 - \frac{g_m R_L}{1 + g_m R_L}\right) + C_{gd}$$

$$R_T = R_S \parallel R_{in} = R_S$$

$$R_{C_{db}} = R_{out} \| R_L = \frac{R_{out} R_L}{R_{out} + R_L} = \frac{R_L}{1 + g_m R_L}$$

$$\omega_{3dB} \approx \frac{1}{R_S\left(\frac{C_{gs}}{1 + g_m R_L} + C_{gd}\right) + C_{db}\frac{R_L}{1 + g_m R_L}}$$

If R_S is not too high, bandwidth can be rather high and approach ω_T

UNIT III
FEEDBACK AMPLIFIERS AND OSCILLATORS

FEEDBACK AMPLIFIERS:

1.1 Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal, and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are in out of phase, the feedback is called **negative feedback**. Use of positive feedback results in oscillations and hence not used in amplifiers.

In this chapter, we introduce the concept of feedback and show how to modify the characteristics of an amplifier by combining a portion or part of the output signal with the input signal. We also study the analysis of various feedback amplifiers.

1.2 Classification of Amplifiers

Before proceeding with the concepts of feedback, it is useful to understand the classification of amplifiers based on the magnitudes of the input and output impedances of an amplifier relative to the source and load impedances, respectively. The amplifiers can be classified into four broad categories : voltage, current, transconductance and transresistance amplifiers.

1.2.1 Voltage Amplifier

Fig. 1.1 shows a Thevenin's equivalent circuit of an amplifier.

If the amplifier input resistance R_i is large compared with the source resistance R_s then $V_i \approx V_s$. If the external load resistance R_L is large compared with the output resistance R_o of the amplifier, then $V_o \approx A_v V_i \approx A_v V_s$. Such amplifier circuit provides a voltage output proportional to the voltage input, and the proportionality factor does not depend on the magnitudes of the source and load resistances. Hence, this amplifier is called **voltage amplifier**. An ideal voltage amplifier must have infinite input resistance R_i and

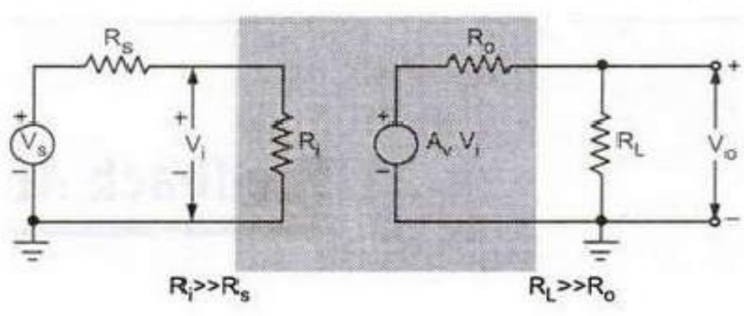


Fig. 1.1 Thevenin's equivalent circuits of a voltage amplifier

zero output resistance R_o. For practical voltage amplifier we must have $R_i >> R_s$ and $R_L >> R_o$.

1.2.2 Current Amplifier

Fig. 1.2 shows Norton's equivalent circuit of a current amplifier. If amplifier input resistance $R_i \to 0$, then $I_i \approx I_s$. If amplifier output resistance $R_o \to \infty$, then $I_L = A_i I_i$. Such amplifier provides a current output proportional to the signal current, and the proportionality factor is independent of source and load resistances. This amplifier is called **current amplifier**. An ideal current amplifier must have zero input resistance R_i and infinite output resistance R_o. For practical current amplifier we must have $R_i << R_s$ and $R_o >> R_L$.

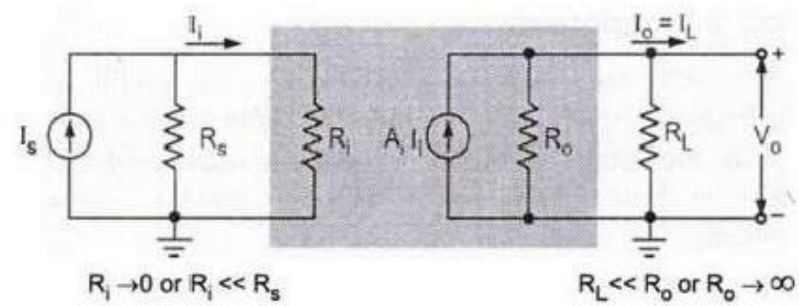


Fig. 1.2 Norton's equivalent circuits of a current amplifier

1.2.3 Transconductance Amplifier

Fig. 1.3 shows a transconductance amplifier with a Thevenin's equivalent in its input circuit and Norton's equivalent in its output circuit. In this amplifier, an output current is proportional to the input signal voltage and the proportionality factor is independent of the magnitudes of the source and load resistances. Ideally, this amplifier must have an infinite input resistance R_i and infinite output resistance R_o. For practical transconductance amplifier we must have $R_i >> R_s$ and $R_o >> R_L$.

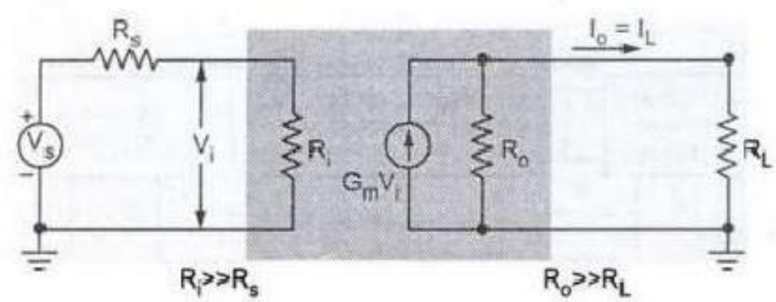


Fig. 1.3 Transconductance amplifier

1.2.4 Transresistance Amplifier

Fig. 1.4 shows a transresistance amplifier with a Norton's equivalent in its input circuit and a Thevenin's equivalent in its output circuit. In this amplifier an output voltage is proportional to the input signal current and the proportionality factor is independent on the source and load resistances. Ideally, this amplifier must have zero input resistance R_i and zero output resistance R_o. For practical transresistance amplifier we must have $R_i << R_s$ and $R_o << R_L$.

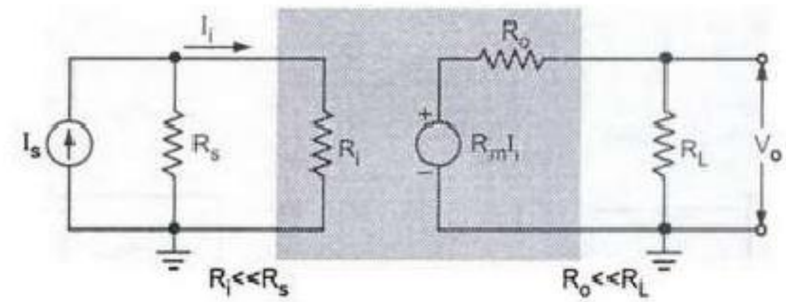


Fig. 1.4

1.3 Block Diagram

In the previous section we have seen four basic amplifier types and their ideal characteristics. In each one of these circuits we can sample the output voltage or current by means of a suitable sampling network and apply this signal to the input through a feedback two port network, as shown in the Fig. 1.5. At the input the feedback signal is combined with the input signal through a mixer network and is fed into the amplifier.

As shown in the Fig. 1.5 feedback connection has three networks :

- Sampling Network
- Feedback Network
- Mixer Network

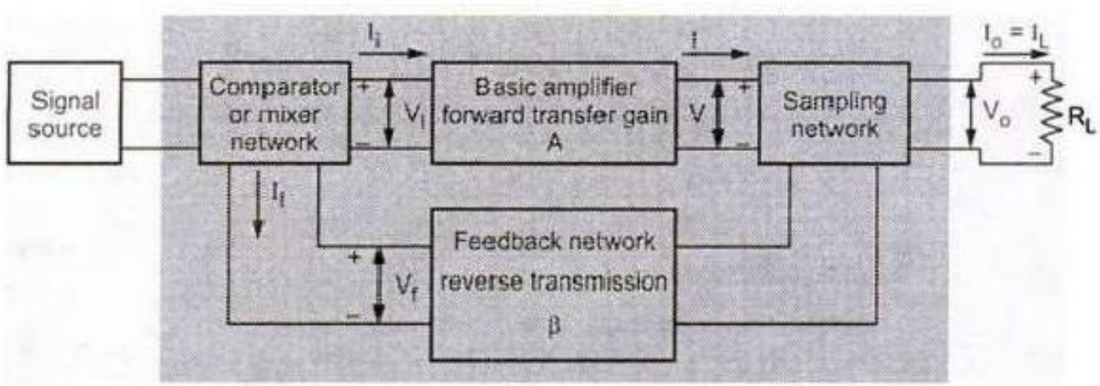
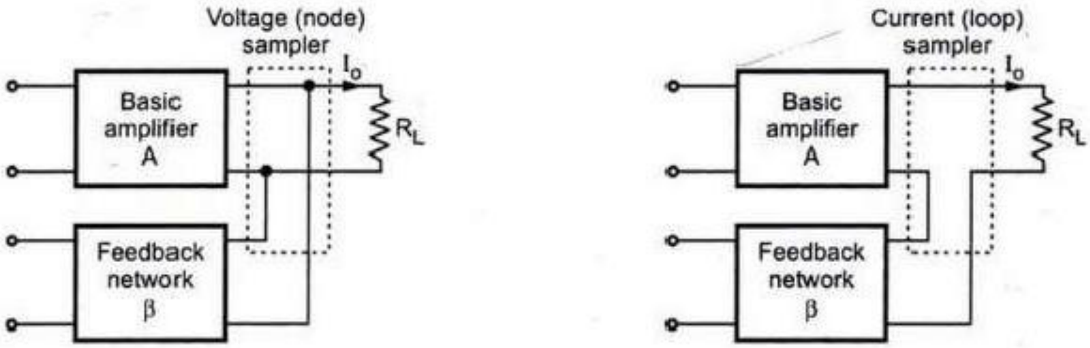


Fig. 1.5 Block diagram of amplifier with feedback

1.3.1 Sampling Network

There are two ways to sample the output, according to the sampling parameter, either voltage or current. The output voltage is sampled by connecting the feedback network in shunt across the output, as shown in the Fig. 1.6 (a). This type of connection is referred to as voltage, or node, sampling. The output current is sampled by connecting the feedback network in series with the output as shown in the Fig. 1.6 (b). This type of connection is referred to as current, or loop, sampling.



(a) Voltage or node sampling

(b) Current or loop sampling

Fig. 1.6

1.3.2 Feedback Network

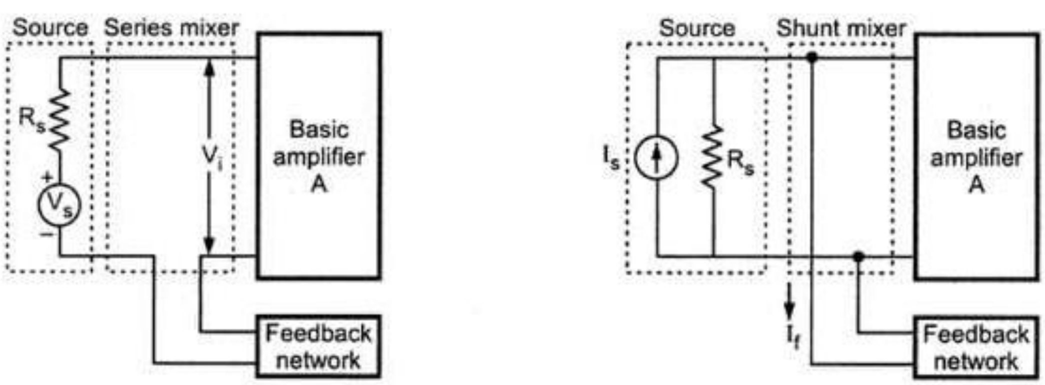
It may consists of resistors, capacitors, and inductors. Most often it is simply a resistive configuration. It provides reduced portion of the output as feedback signal to the input mixer network. It is given as

$$V_f = \beta V_o$$

where β is a **feedback factor** or **feedback ratio**. The symbol β used in feedback circuits represents feedback factor which always lies between 0 and 1. It is totally different from β symbol used to represent current gain in common emitter amplifier, which is greater than 1.

1.3.3 Mixer Network

Like sampling, there are two ways of mixing feedback signal with the input signal. These are : series input connection and shunt input connection. The Fig. 1.7 (a) and (b) show the simple and very common **series (loop)** input and **shunt (node)** input connections, respectively.



(a) Series mixing

(b) Shunt mixing

1.3.4 Transfer Ratio or Gain

In Fig. 1.5, the ratio of the output signal to the input signal of the basic amplifier is represented by the symbol A. The suffix of A given next, represents the different transfer ratios.

$$\frac{V}{V_i} = A_v = \text{Voltage gain} \quad \dots (1)$$

$$\frac{I}{I_i} = A_i = \text{Current gain} \quad \dots (2)$$

$$\frac{I}{V_i} = G_m = \text{Transconductance} \quad \dots (3)$$

$$\frac{V}{I_i} = R_m = \text{Transresistance} \quad \dots (4)$$

The four quantities A_v, A_i, G_m and R_m are referred to as a transfer gain of the basic amplifier without feedback and use of only symbol A represent any one of these quantities.

The transfer gain with feedback is represented by the symbol A_f. It is defined as the ratio of the output signal to the input signal of the amplifier configuration shown in Fig. 1.5. Hence A_f is used to represent any one of the following four ratios :

$$\frac{V_o}{V_s} = A_{Vf} = \text{Voltage gain with feedback} \quad \dots (5)$$

$$\frac{I_o}{I_s} = A_{If} = \text{Current gain with feedback} \quad \dots (6)$$

$$\frac{I_o}{V_s} = G_{Mf} = \text{Transconductance with feedback} \quad \dots (7)$$

$$\frac{V_o}{I_s} = R_{Mf} = \text{Transresistance with feedback} \quad \dots (8)$$

Fig. 1.8 shows the schematic representation of a feedback connection around a basic amplifier. Recall that, when part of output signal and input signal are in out of phase the feedback is called **negative feedback**. The schematic diagram shown in Fig. 1.8 represents negative feedback because the feedback signal is fed back to the input of the amplifier out of phase with input signal of the amplifier.

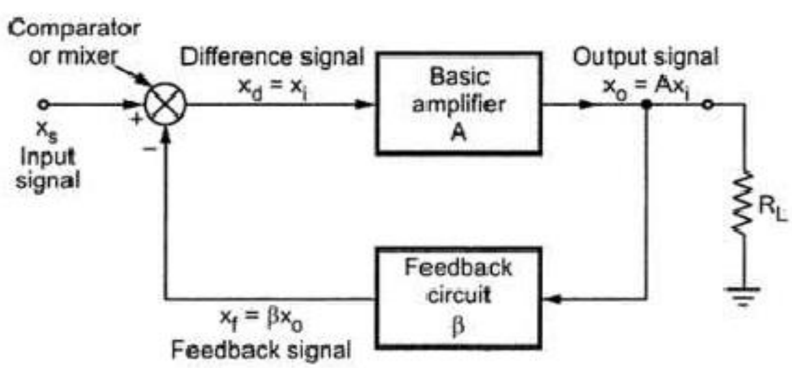


Fig. 1.8 Schematic representation of negative feedback amplifier

1.4 Advantages of Negative Feedback

It is possible to improve important characteristics of four basic amplifier types discussed in section 1.2 by the proper use of negative feedback.

- Normally high input resistance of a voltage amplifier can be made higher.
- Normally low output resistance of a voltage amplifier can be lowered.
- The transfer gain A_f of the amplifier with feedback can be stablized against variations of the h or hybrid-π parameters of the transistor or the parameters of the other active devices used in the amplifier.
- The proper use of negative feedback improves frequency response of the amplifier.
- There is a significant improvement in the linearity of operation of the feedback amplifier compared with that of the amplifier without feedback.

Key Point : *All the advantages mentioned above are obtained at the expense of the gain A_f with feedback, which is lowered in comparison with the transfer gain A of an amplifier without feedback.*

1.5 The Four Basic Feedback Topologies

The basic amplifier shown in Fig. 1.8 may be a voltage, current, transconductance, or transresistance amplifier. These can be connected in a feedback configuration as shown in the Fig. 1.9.

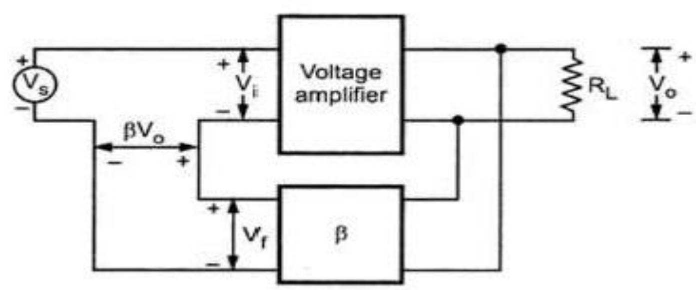


Fig. 1.9 (a) Voltage amplifier with voltage series feedback

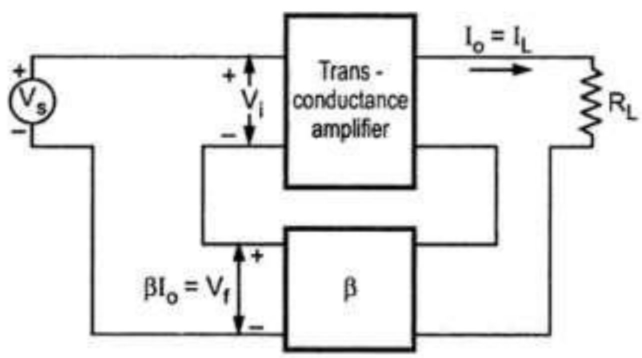


Fig. 1.9 (b) Transconductance amplifier with current series feedback

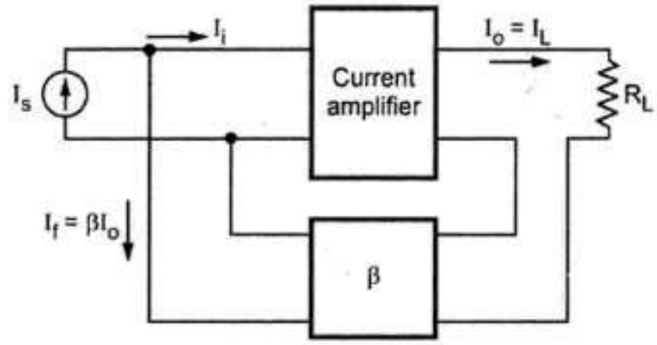


Fig. 1.9 (c) Current amplifier with current-shunt feedback

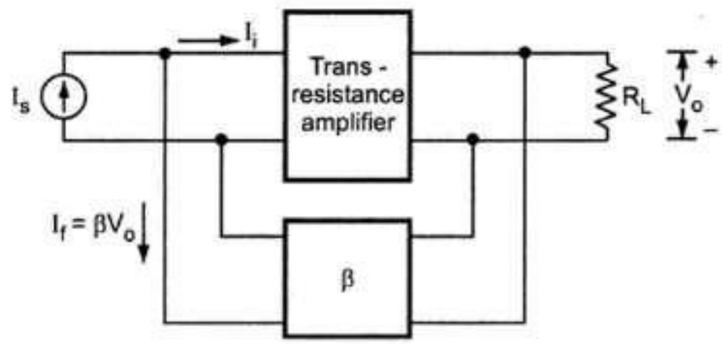


Fig. 1.9 (d) Transresistance amplifier with voltage shunt feedback

1.6 Gain with Feedback

We have seen, the symbol A is used to represent transfer gain of the basic amplifier without feedback and symbol A_f is used to represent transfer gain of the basic amplifier with feedback. These are given as

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

where

X_o = Output voltage or output current

X_i = Input voltage or input current

X_s = Source voltage or source current

As it is a negative feedback the relation between X_i and X_s is given as

$$X_i = X_s + (-X_f)$$

where X_f = Feedback voltage or feedback current

$$\therefore \quad A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

Dividing by X_i to numerator and denominator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f)/X_i}$$

$$= \frac{A}{1 + X_f / X_i} \quad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \quad A_f = \frac{A}{1 + \beta A} \quad \because \beta = \frac{X_f}{X_o} \quad \dots (1)$$

where β is a feedback factor

Looking at equation we can say that gain without feedback (A) is always greater than gain with feedback $(A/(1 + \beta A))$ and it decreases with increase in β i.e. increase in feedback factor.

For voltage amplifier, gain with negative feedback is given as

$$\boxed{A_{vf} = \frac{A_v}{1 + A_v \beta}} \quad \dots (2)$$

where A_v = Open loop gain i.e. gain without feedback

β = Feedback factor

1.6.1 Loop Gain

The diference signal, X_d in Fig. 1.8 is multiplied by A in passing through the amplifier, is multiplied by β in transmission through the feedabck network, and is multiplied by -1 in the mixing or difference network. A path of a signal from input terminals through basic amplifier, through the feedback network and back to the input terminals forms a loop. The gain of this loop is the product $-A\beta$. This gain is known as **loop gain** or **return ratio**.

1.6.2 Desensitivity of Gain

The transfer gain of the amplifier is not constant as it depends on the factors such as operating point, temperature, etc. This lack of stability in amplifiers can be reduced by introducing negative feedback.

We know that,

$$A_f = \frac{A}{1 + \beta A}$$

Differentiating both sides with respect to A we get,

$$\frac{dA_f}{dA} = \frac{(1 + \beta A) 1 - \beta A}{(1 + \beta A)^2}$$

$$= \frac{1}{(1 + \beta A)^2}$$

$$\therefore \quad dA_f = \frac{dA}{(1 + \beta A)^2}$$

Dividing both sides by A_f we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+\beta A)^2} \times \frac{1}{A_f}$$

$$= \frac{dA}{(1+\beta A)^2} \times \frac{(1+\beta A)}{A_f} \qquad \text{since } A_f = \frac{A}{1+\beta A}$$

$$\left|\frac{dA_f}{A_f}\right| = \left|\frac{dA}{A}\right| \frac{1}{|(1+\beta A)|} \qquad \ldots (3)$$

where

$\frac{dA_f}{A_f}$ = Fractional change in amplification with feedback

$\frac{dA}{A}$ = Fractional change in amplification without feedback

Looking at equation (3) we can say that change in the gain with feedback is less than the change in gain without feedback by factor $(1+\beta A)$. The fractional change in amplification with feedback divided by the fractional change without feedback is called the **sensitivity of the transfer gain**. Hence the sensitivity is $\frac{1}{(1+\beta A)}$. The reciprocal of the sensitivity is called the **desensitivity D**. It is given as

$$D = 1 + \beta A$$

Therefore, stability of the amplifier increases with increase in desensitivity.

If $\beta A >> 1$, then

$$A_f = \frac{A}{1+\beta A} = \frac{A}{\beta A}$$

$$= \frac{1}{\beta} \qquad \ldots (4)$$

and the gain is dependent only on the feedback network.

Since A represents either A_v, G_M, A_I or R_M and A_f represents the corresponding transfer gains with feedback either A_{vf}, G_{Mf}, A_{If} or R_{Mf} the equation signifies that :

- For voltage series feedback

$$A_{vf} = \frac{1}{\beta} \quad \text{voltage gain is stabilized} \qquad \ldots (5)$$

- For current series feed back

$$G_{Mf} = \frac{1}{\beta} \quad \text{transconductance gain is stabilized} \qquad \ldots (6)$$

- For voltage shunt feedback

$$R_{Mf} = \frac{1}{\beta} \quad \text{transresistance gain is stabilized} \qquad \ldots (7)$$

- For current shunt feedback

$$A_{If} = \frac{1}{\beta} \quad \text{Current gain is stabilized} \qquad \ldots (8)$$

1.7 Cut Off Frequencies With Feedback

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Using this equation we can write,

$$A_{f\,mid} = \frac{A_{mid}}{1+\beta A_{mid}} \quad \dots (1)$$

$$A_{f\,low} = \frac{A_{low}}{1+\beta A_{low}} \quad \dots (2)$$

and

$$A_{f\,high} = \frac{A_{high}}{1+\beta A_{high}} \quad \dots (3)$$

Now we analyse the effect of negative feedback on lower cutoff and upper cutoff frequency of the amplifier.

Lower cutoff frequency

We know that, the relation between gain at low frequency and gain at mid frequency, is given as,

$$\frac{A_{low}}{A_{mid}} = \frac{1}{1-j\left(\frac{f_L}{f}\right)} \quad \therefore A_{low} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)} \quad \dots (4)$$

Substituting value of A_{low} in equation (1) we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}\right)}$$

$$= \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)+A_{mid}\beta}$$

$$= \frac{A_{mid}}{(1+A_{mid}\beta)-j\left(\frac{f_L}{f}\right)}$$

Dividing numerator and denominator by $(1+A_{mid}\beta)$ we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1+A_{mid}\beta}}{1-j\left[\dfrac{\frac{f_L}{1+A_{mid}\beta}}{f}\right]}$$

$$= \frac{A_{f\,mid}}{1-j\left[\left(\dfrac{\frac{f_L}{1+A_{mid}\beta}}{f}\right)\right]} \quad \because A_f\,mid = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$\therefore \quad \frac{A_{f\,low}}{A_{f\,mid}} = \frac{1}{1-j\left(\frac{f_{Lf}}{f}\right)} \quad \ldots(5)$$

where

$$\boxed{\text{Lower cutoff frequency with feedback} = f_{Lf} = \frac{f_L}{1+A_{mid}\,\beta}} \quad \ldots (6)$$

From equation (6), we can say that lower cutoff frequency with feedback is less than lower cutoff frequency without feedback by factor $(1+A_{mid}\,\beta)$. Therefore, by introducing negative feedback low frequency response of the amplifier is improved.

Upper Cutoff Frequency

We know that, the relation between gain at high frequency and gain at mid frequency is given as,

$$\frac{A_{high}}{A_{mid}} = \frac{1}{1-j\left(\frac{f}{f_H}\right)}$$

$$\therefore \quad A_{high} = \frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)} \quad \ldots (7)$$

Substituting value of A_{high} in equation (11) we get,

$$Af\ high = \frac{\dfrac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)}\right)} = \frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)+A_{mid}\beta}$$

Dividing numerator and denominator by $(1+A_{mid}\,\beta)$ we get,

$$A_{f\,high} = \frac{\dfrac{A_{mid}}{1+A_{mid}\,\beta}}{1-j\left[\dfrac{f}{(1+A_{mid}\beta)\,f_H}\right]}$$

$$A_{f\,high} = \frac{A_{f\,mid}}{1-j\left[\dfrac{f}{(1+A_{mid}\beta)\,f_H}\right]} \quad \because\ A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$= \frac{A_{f\,mid}}{1-j\left(\frac{f}{f_{Hf}}\right)}$$

where upper cutoff frequency with feedback is given as

$$\boxed{f_{Hf} = (1+A_{mid}\,\beta)\,f_H} \quad \ldots (8)$$

From equation (8), we can say that upper cutoff frequency with feedback is greater than upper cutoff frequency without feedback by factor $(1+A_{mid}\,\beta)$. Therefore, by introducing negative feedback high frequency response of the amplifier is improved.

Bandwidth

The bandwidth of the amplifier is given as

$$BW = \text{Upper cutoff frequency} - \text{lower cutoff frequency}$$

$\therefore$ Bandwidth of the amplifier with feedback is given as

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\,\beta)\, f_H - \frac{f_L}{(1 + A_{mid}\,\beta)} \quad \ldots (9)$$

It is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 1.10.

It is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 1.10.

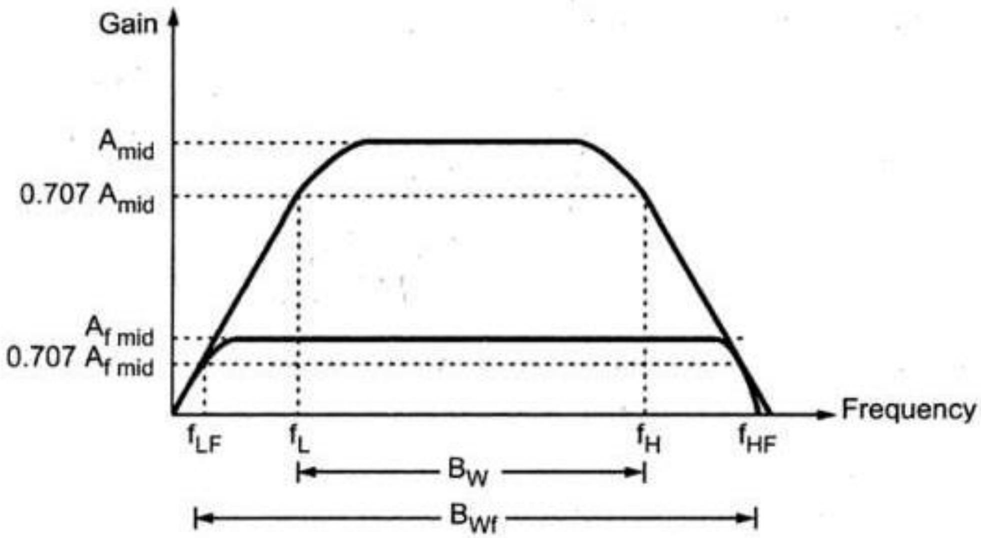


Fig. 1.10 Effect of negative feedback on gain and bandwidth

Key Point: *Since bandwidth with negative feedback increases by factor (1 + Aβ) and gain decreases by same factor, the gain-bandwidth product of an amplifier does not altered, when negative feedback is introduced.*

1.8 Distortion with Feedback

1.8.1 Frequency Distortion

From equation (8) of previous section 1.8 we can say that if the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under such conditions frequency and phase distortion is substantially reduced.

If β is made up of reactive components, the reactances of these components will change with frequency, changing the β. As a result, gain will also change with frequency. This fact is used in tuned amplifiers. In tuned amplifiers, feedback network is designed such that at tuned frequency $\beta \rightarrow 0$ and at other frequencies $\beta \rightarrow \infty$. As a result, amplifier provides high gain for signal at tuned frequency and relatively reject all other frequencies.

1.8.2 Noise and Nonlinear Distortion

Signal feedback reduces the amount of noise signal and non linear distortion. The factor $(1+\beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. Thus, noise and non linear distortion also reduced by same factor as the gain.

1.9 Input and Output Resistances

1.9.1 Input resistance

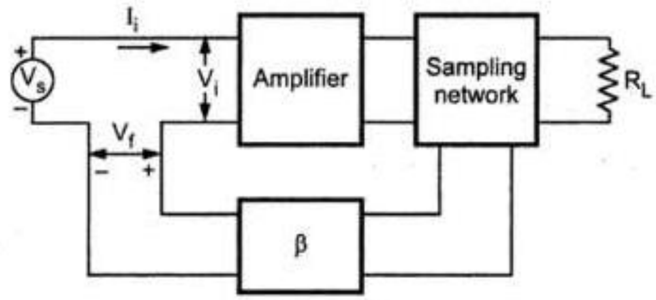


Fig. 1.11

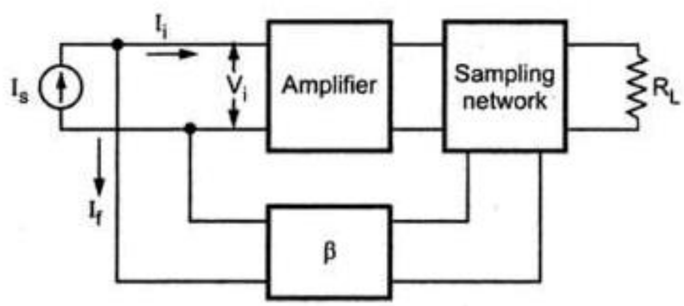


Fig. 1.12

If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), it increases the input resistance. Since the feedback voltage V_f opposes V_s, the input current I_i is less than it would be if V_f were absent, as shown in the Fig. 1.11.

Hence, the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback, for the circuit shown in Fig. 1.11.

On the otherhand, if the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current), it decreases the input resistance. Since $I_s = I_i + I_f$, the current I_s drawn from the signal source is increased over what it would be if there were no feedback current, as shown in the Fig. 1.12.

Hence, the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in Fig. 1.12. Now we see the effect of negative feedback on input resistance in different topologies (ways) of introducing negative feedback and obtain R_{if} quantitatively.

Voltage series feedback

The voltage series feedback topology shown in Fig. 1.13 with amplifier is replaced by Thevenin's model. Here, A_v represents the open-circuit voltage gain taking R_s into account. since throughout the discussion of feedback amplifiers we will consider R_s to be part of the amplifier and we will drop the subscript on the transfer gain and input resistance (A_v instead of A_{vs} and R_{if} instead of R_{ifs}).

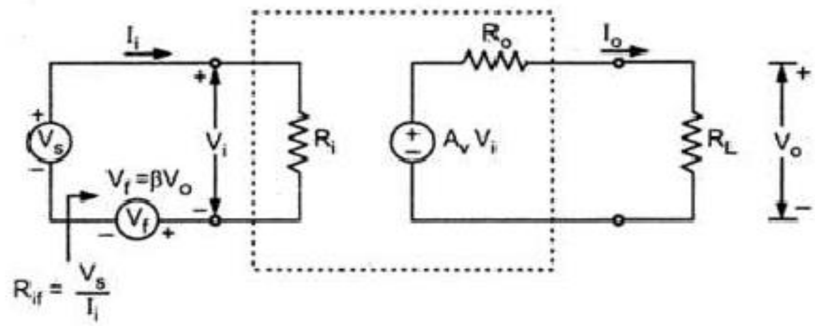


Fig. 1.13

Look at Fig. 1.13 the input resistance with feedback is given as

$$R_{if} = \frac{V_s}{I_i} \quad \ldots (1)$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f$$

$$= I_i R_i + \beta V_o \quad \ldots (2)$$

The output voltage V_o is given as

$$V_o = \frac{A_v V_i R_L}{R_o + R_L}$$

$$= A_V I_i R_i = Av V_i \quad \ldots (3)$$

where

$$Av = \frac{V_o}{V_i}$$

$$= \frac{A_v R_L}{R_o + R_L}$$

Key Point: A_v *represents the open circuit voltage gain without feedback and* A_V *is the voltage gain without feedback taking the load* R_L *into account).*

Key Point: A_v *represents the open circuit voltage gain without feedback and* A_V *is the voltage gain without feedback taking the load* R_L *into account).*

Substituting value of V_o from equation (3) in equation (2) we get,

$$V_s = I_i R_i + \beta A_V I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i + \beta A_V R_i$$

$$\therefore \quad \boxed{R_{if} = R_i (1 + \beta A_V)} \quad \ldots (4)$$

Current series feedback

The current series feedback topology is shown in Fig. 1.14 with amplifier input circuit is represented by Thevenin's equivalent circuit and output circuit by Norton's equivalent circuit.

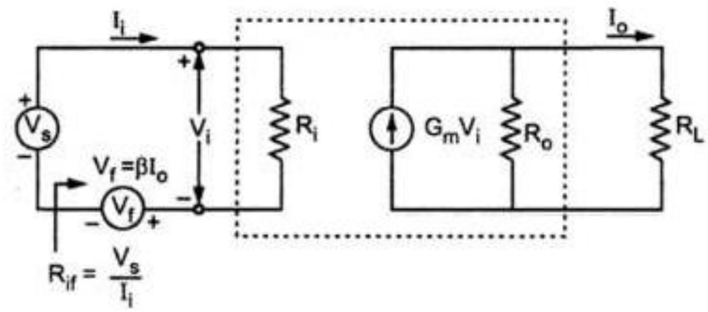


Fig. 1.14

Looking at Fig. 1.14 the input resistance with feedback is given as

$$R_{if} = \frac{V_s}{I_i}$$

Applying KVL to the input side we get,

$$V_s - I_i\ R_i - V_f = 0$$

$$\therefore \quad V_s = I_i\ R_i + V_f$$

$$= I_i\ R_i + \beta\ I_o \qquad \dots (5)$$

The output current I_o is given as

$$I_o = \frac{G_m\ V_i R_o}{R_o + R_L} = G_M\ V_i \qquad \dots (6)$$

where

$$G_M = \frac{G_m R_o}{R_o + R_L}$$

Key Point: *G_M represents the open circuit transconductance without feedback and G_M is the transconductance without feedback taking the load R_L into account.*

Substituting value of I_o from equation (6) into equation (5) we get,

$$V_s = I_i\ R_i + \beta\ G_M\ V_i$$

$$= I_i\ R_i + \beta\ G_M\ I_i\ R_i \qquad \because\ V_i = I_i\ R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i\ (1 + \beta G_M)$$

$$\therefore \quad \boxed{R_{if} = \frac{V_s}{I_i} = R_i\ (1 + \beta G_M)} \qquad \dots (7)$$

Current shunt feedback

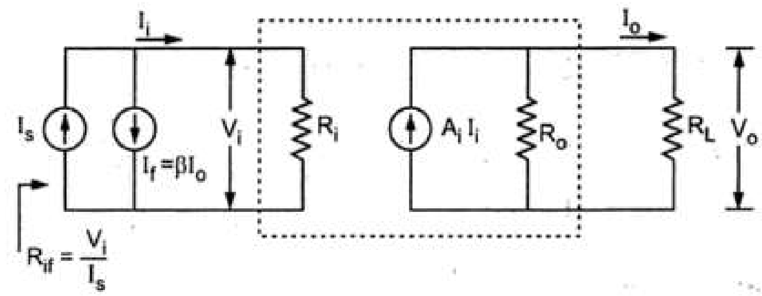


Fig. 1.15

The current shunt feedback topology is shown in Fig. 1.15 with amplifier input and output circuit replaced by Norton's equivalent circuit

Applying KCL to the input node we get

$$I_s = I_i + I_f$$

$$= I_i + \beta I_o \quad \dots (8)$$

The output current I_o is given as

$$I_o = \frac{A_i \; I_i R_o}{R_o + R_L}$$

$$= A_I \; I_i \quad \dots (9)$$

where $$A_I = \frac{A_i R_o}{R_o + R_L}$$

Key Point: A_i *represents the open circuit current gain without feedback and* A_I *is the current gain without feedback taking the load* R_L *into account.*

Substituting value of I_o from equation (9) into equation (8) we get,

$$I_s = I_i + \beta A_I I_i$$

$$= I_i \; (1 + \beta A_I)$$

The input resistance with feedback is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i \; (1 + \beta \; A_I)}$$

$$\therefore \quad R_{if} = \frac{R_i}{(1 + \beta A_I)} \quad \because R_i = \frac{V_i}{I_i} \quad \dots (10)$$

Voltage shunt feedback

The voltage shunt feedback topology is shown in Fig. 1.16 with amplifier input circuit is represented by Norton's equivalent circuit and output circuit represented by Thevenin's equivalent.

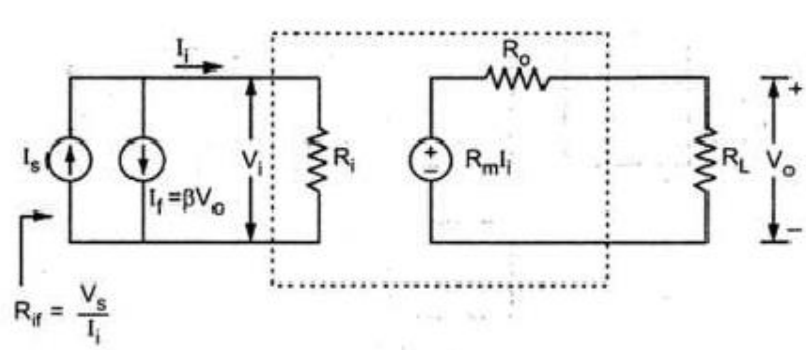


Fig. 1.16

Applying KCL at input node we get,

$$I_s = I_i + I_f$$

$$= I_i + \beta V_o \qquad \dots (11)$$

The output voltage V_o is given as

$$V_o = \frac{R_m I_i R_o}{R_o + R_L}$$

$$= R_M I_i \qquad \dots (12)$$

where $$R_M = \frac{R_m R_o}{R_o + R_L}$$

Key Point: *R_m represents the open circuit transresistance without feedback and R_M is the transresistance without feedback taking the load R_L into account*

Substituting value of V_o from equation (12) into equation (11) we get,

$$I_s = I_i + \beta R_M I_i$$

$$= I_i (1 + \beta R_M)$$

The input resistance with feedback R_{if} is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i (1 + \beta R_M)}$$

$$\therefore \quad \boxed{R_{if} = \frac{R_i}{(1 + \beta R_M)}} \qquad \because R_i = \frac{V_i}{I_i} \qquad \dots (13)$$

1.9.2 Output resistance

The negative feedback which samples the output voltage, regardless of how this output signal is returned to the input, tends to decrease the output resistance, as shown in the Fig. 1.17.

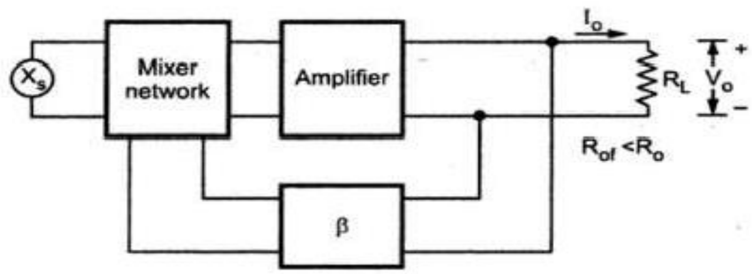


Fig. 1.17

On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 1.18.

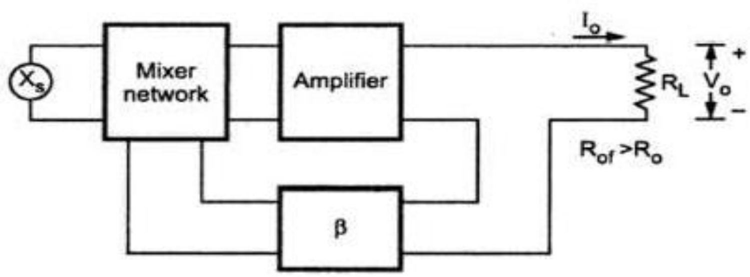


Fig. 1.18

Now, we see the effect of negative feedback on output resistance in different topologies (ways) of introducing negative feedback and obtain R_{of} quantitatively.

Voltage series feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 1.19.

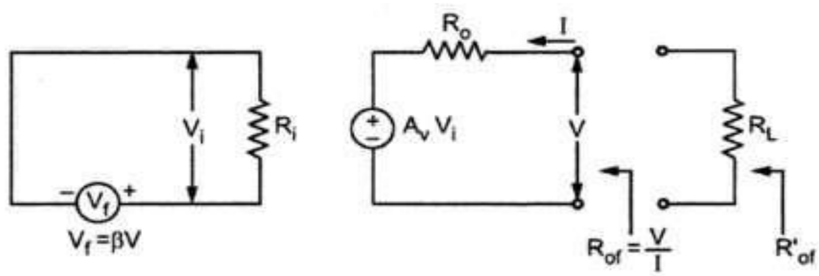


Fig. 1.19

Applying KVL to the output side we get,

$$A_v V_i + IR_o - V = 0$$

$$\therefore \qquad I = \frac{V - A_v V_i}{R_o} \qquad \dots (14)$$

The input voltage is given as

$$V_i = -V_f = -\beta V \qquad \because V_s = 0 \qquad \dots (15)$$

Substituting the V_i from equation (32) in equation (31) we get,

$$I = \frac{V + A_v \beta V}{R_o} = \frac{V(1 + \beta A_v)}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I}$$

$$\therefore \quad \boxed{R_{of} = \frac{R_o}{(1+\beta A_v)}} \quad \text{... (16)}$$

Key Point: *Here A_v is the open loop voltage gain without taking R_L in account,*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L} = \frac{\left(\frac{R_o}{1+\beta A_v}\right) \times R_L}{\frac{R_o}{(1+\beta A_v)} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L(1+\beta A_v)} = \frac{R_o R_L}{R_o + R_L + \beta A_v R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}}$$

$$\therefore \quad \boxed{R'_{of} = \frac{R'_L}{1+\beta A_V}} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_V = \frac{A_v R_L}{R_o + R_L} \quad \text{... (17)}$$

Key Point: *Here A_V is the open loop voltage gain taking R_L into account.*

Voltage shunt feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 1.20.

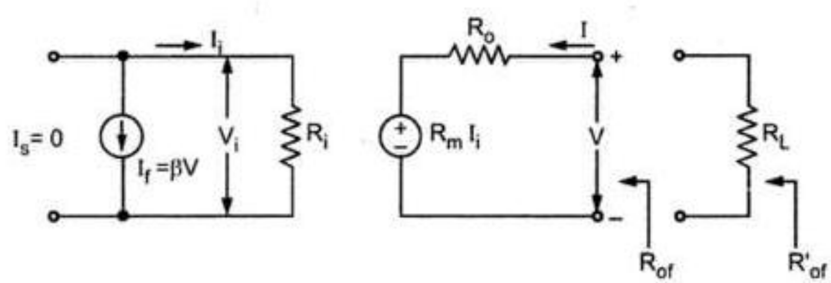


Fig. 1.20

Applying KVL to the output side we get,

$$R_m I_i + I R_o - V = 0$$

$$\therefore \quad I = \frac{V - R_m I_i}{R_o} \quad \text{... (18)}$$

The input current is given as

$$I_i = -I_f = -\beta V. \quad \text{... (19)}$$

Substituting I_i from equation (19) in equation (18) we get,

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

$$\therefore \qquad R_{of} = \frac{V}{I}$$

$$\therefore \qquad \boxed{R_{of} = \frac{R_o}{1 + R_m \beta}} \qquad \ldots [20 (a)]$$

Key Point: *Here,* R_m *is the open loop transresistance without taking* R_L *in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{\dfrac{R_o \times R_L}{1 + R_m \beta}}{\dfrac{R_o}{1 + R_m \beta} + R_L} = \frac{R_o R_L}{R_o + R_L (1 + R_m \beta)}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_o R_L}{R_o + R_L}}{1 + \dfrac{\beta R_m R_L}{R_o + R_L}}$$

$$\boxed{R'_{of} = \frac{R'_o}{1 + \beta R_m}} \qquad \ldots (38)$$

Key Point: *Here,* R_m *is the open loop transresistance taking* R_L *in account.*

Current shunt feedback

In this topology, the output resistance can be measured by open circuiting the input source $I_s = 0$ and looking into the output terminals, with R_L disconnected, as shown in the Fig. 1.21.

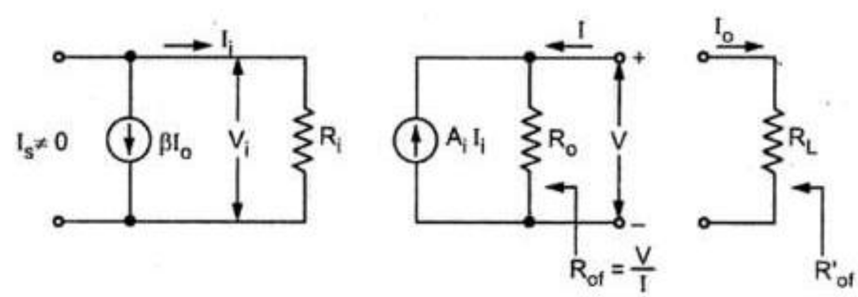


Fig. 1.21

Applying the KCL to the output node we get,

$$I = \frac{V}{R_o} - A_i \ I_i \quad \dots (21)$$

The input current is given as

$$I_i = -I_f = -\beta I_o \quad \because I_s = 0$$

$$= \beta I \quad \because I = -I_o \quad \dots (22)$$

Substituting value of I_i from equation (22) in equation (21) we get,

$$I = \frac{V}{R_o} - A_i \beta I$$

$$\therefore \quad I(1 + A_i \beta) = \frac{V}{R_o}$$

$$\therefore \quad \boxed{R_{of} = \frac{V}{I} = R_o (1 + \beta A_i)} \quad \dots (23)$$

Key Point: *Here, A_i is the open loop current gain without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o (1 + \beta A_i) R_L}{R_o (1 + \beta A_i) + R_L} = \frac{R_o R_L (1 + \beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\frac{R_o R_L (1 + \beta A_i)}{R_o + R_L}}{1 + \frac{\beta A_i R_o}{R_o + R_L}}$$

$$\therefore \quad \boxed{R'_{of} = \frac{R'_o (1 + \beta A_i)}{(1 + \beta A_I)}}$$

$$\because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_I = \frac{A_i R_o}{R_o + R_L} \quad \dots (24)$$

Key Point: *Here, A_I is the open loop current gain taking R_L in account.*

Current series feedback

In this topology the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 1.22.

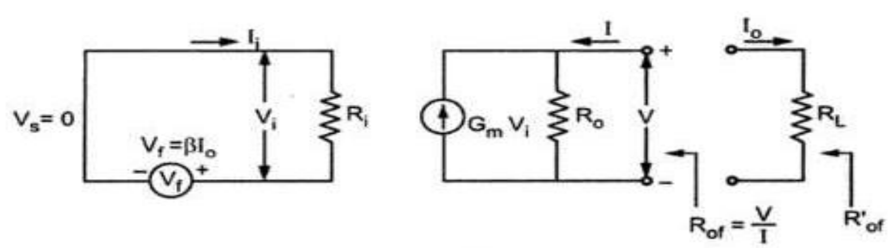


Fig. 1.22

Applying KCL to the output node we get,

$$I = \frac{V}{R_o} - G_m V_i \quad \dots (25)$$

The input voltage is given as $V_i = -V_f = -\beta I_o$

$$= \beta I \qquad \because I_o = -I \quad \dots (26)$$

Substituting value of V_i from equation (26) in equation (25) we get,

$$I = \frac{V}{R_o} - G_m \beta I$$

$$\therefore \quad I(1 + G_m \beta) = \frac{V}{R_o}$$

$$\therefore \quad \boxed{R_{of} = \frac{V}{I} = R_o (1 + G_m \beta)} \quad \dots (27)$$

Key Point: *Here, G_m is the open loop transconductance without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o (1+\beta G_m) R_L}{R_o (1+\beta G_m) + R_L} = \frac{R_o R_L (1+\beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$

we get
$$R'_{of} = \frac{\dfrac{R_L R_o (1+\beta G_m)}{R_o + R_L}}{1 + \dfrac{\beta G_m R_o}{R_o + R_L}}$$

$$\boxed{R'_{of} = \frac{R'_o (1+\beta G_m)}{1+\beta G_M}} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } G_M = \frac{G_m R_o}{R_o + R_L} \quad \dots (28)$$

Key Point: *Note that here, G_M is the open loop current gain taking R_L in account.*

1.10 Summary of Effect of Negative Feedback on Amplifier

Table 1.1 summarizes the effect of negative feedback on amplifier.

Parameter	Voltage series	Current series	Current shunt	Voltage shunt
Gain with feedback	$A_{vf} = \frac{A_v}{1+\beta A_v}$ decreases	$G_{mf} = \frac{G_m}{1+\beta G_m}$ decreases	$A_{if} = \frac{A_i}{1+\beta A_i}$ decreases	$R_{mf} = \frac{R_m}{1+\beta R_{mf}}$ decreases
Stability	Improves	Improves	Improves	Improves
Frequency response	Improves	Improves	Improves	Improves
Frequency distortion	Reduces	Reduces	Reduces	Reduces
Noise and Non linear distortion	Reduces	Reduces	Reduces	Reduces
Input resistance	$R_{if} = R_i(1+\beta A_V)$ increases	$R_{if} = R_i(1+\beta G_M)$ increases	$R_{if} = \frac{R_i}{1+\beta A_I}$ decreases	$R_{if} = \frac{R_i}{1+\beta R_M}$ decreases
Output resistance	$R_{of} = \frac{R_o}{1+\beta A_v}$ decreases	$R_{of} = R_o(1+\beta G_M)$ increases	$R_{of} = R_o(1+\beta A_i)$ increases	$R_{of} = \frac{R_o}{1+\beta R_m}$ decreases

Table 1.1

1.11 Method of Identifying Feedback Topology and Analysis of a Feedback Amplifier

To analyse the feedback amplifier it is necessary to go through the following steps.

Step 1 : Identify Topology (Type of feedback)

a) To find the type of sampling network

1. By shorting the output i.e. V = 0, if feedback signal (x_f) becomes zero then we can say that it is "Voltage Sampling".
2. By opening the output loop i.e. I = 0, if feedback signal (x_f) becomes zero then we can say that it is "Current Sampling".

b) To find the type of mixing network

1. If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop, we can say that it is "series mixing".
2. If the feedback signal is subtracted from the externally applied signal as a current in the input loop, we can say that it is "shunt mixing".

Thus by determining type of sampling network and mixing network, type of feedback amplifier can be determine. For example, if amplifier uses a voltage sampling and series mixing then we can say that it is a voltage series amplifier.

Step 2 : Find the input circuit

1. For voltage sampling make V = 0 by shorting the output
2. For current sampling make I = 0 by opening the output loop.

Step 3 : Find the output circuit.

1. For series mixing make I = 0 by opening the input loop.
2. For shunt mixing make V = 0 by shorting the input

Step 2 and step 3 ensure that the feedback is reduced to zero without altering the loading on the basic amplifier.

Step 4 : Optional. Replace each active device by its h-parameter model at low frequency.

Step 5 : Find the open loop gain (gain without feedback), A of the amplifier.

Step 6 : Indicate X_f and X_o on the circuit and evaluate $\beta = X_f\ X_o$.

Step 7 : From A and β, find D, A_f, R_{if}, R_{of}, and R'_{of}.

Characteristics	Topology			
	Voltage series	Current series	Current shunt	Voltage shunt
Sampling signal X_o	Voltage	Voltage	Current	Current
Mixing signal	Voltage	Current	Current	Voltage
To find input loop, set	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
To find output loop, set	$I_i = 0$	$I_i = 0$	$V_i = 0$	$V_i = 0$
Single source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_V = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1 + \beta A$	$1 + \beta A_V$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_V/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$\frac{R_o}{1+\beta A_v}$	$R_o(1 + \beta G_m)$	$R_o(1 + \beta A_i)$	$\frac{R_o}{1+\beta R_m}$
$R'_{of} = R_{of} \parallel R_L$	$\frac{R'_o}{1+\beta A_v}$	$\frac{R'_o(1+\beta G_m)}{1+\beta G_M}$	$\frac{R'_o(1+\beta A_i)}{1+\beta A_I}$	$\frac{R'_o}{1+\beta R_M}$

Table 1.2

1.12 Analysis of Feedback Amplifiers

1.12.1 Voltage Series Feedback

In this section, we will see two examples of the voltage series amplifier, First we will analyse transistor emitter follower circuit and then source follower using FET.

1.12.1.1 Transistor Emitter Follower

Fig. 1.23 shows the transistor emitter follower circuit. Here feedback voltage is the voltage across R_e and sampled signal is V_o across R_e.

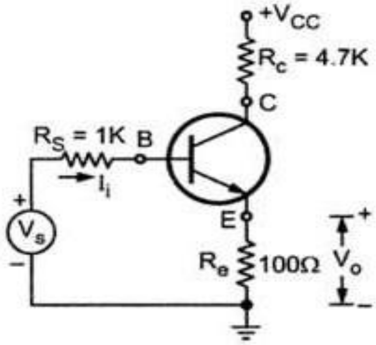


Fig. 1.23

Analysis

Step 1 : Identify Topology

By shorting output voltage ($V_o = 0$), feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 1.23 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

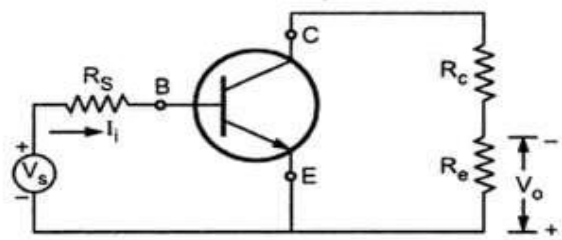


Fig. 1.24

To find the input circuit, set $V_o = 0$, and hence V_s in series with R_s appears between B and E. To find the output circuit, set $I_i = I_b = 0$, and hence R_e appears only in the output loop. With these connections we obtain the circuit as shown in the Fig. 1.24.

Step 4 : Replace transistor by its h-parameter equivalent circuit

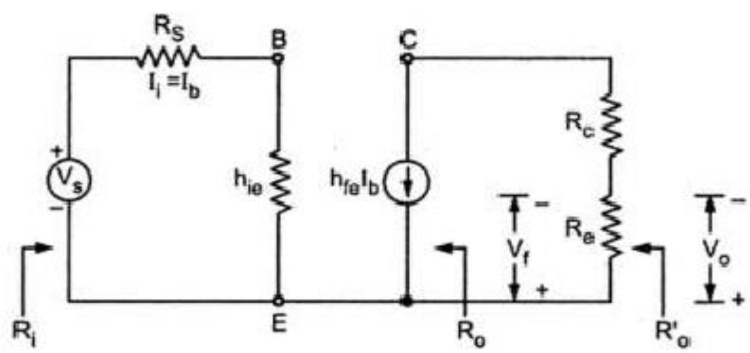


Fig. 1.25 Transistor replaced by its approximate h-parameter equivalent circuit

Step 5 : Find open loop voltage gain

$$A_V = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_e}{V_s}$$

Applying KVL to input loop we get

$$V_s = I_b (R_s + h_{ie})$$

Substituting value of V_s we get

$$A_V = \frac{h_{fe} R_e}{R_s + h_{ie}} = \frac{50 \times 100}{1\,K + 1.1\,K} = 2.38$$

Step 6 : Indicate V_o and V_f and calculate β

We have $\beta = \frac{V_f}{V_o} = 1$ $\because$ both voltage present across R_e

Step 7 : Calculate D, A_{vf}, R_{if}, R_{of} and R'_{of}

$$D = 1 + \beta A_V$$
$$= 1 + 1 \times 2.38$$
$$= \mathbf{2.38}$$
$$A_{Vf} = \frac{A_V}{1+\beta A_V} = \frac{A_V}{D} = \frac{2.38}{3.38}$$
$$= \mathbf{0.7}$$
$$R_i = R_s + h_{ie}$$
$$= 1K + 1.1K = \mathbf{2.1K}$$
$$R_{if} = R_i\ D$$
$$= 2.1k \times 3.38$$
$$= \mathbf{7.098K}$$
$$R_o = \infty$$
$$R_{of} = \infty$$
$$R'_{of} = \frac{R'_o}{D} \quad \text{where } R'_o = R_e$$
$$\therefore \quad R'_{of} = \frac{R_e}{D} = \frac{100}{3.38}$$
$$= \mathbf{29.58\ \Omega}$$

1.12.2 Current Series Feedback

In this section, we will see two examples of the current series feedback amplifier. First we will analyse transistor common emitter circuit with unbypassed emitter resistance and then common source with unbypassed source resistance.

1.12.2.1 Common Emitter Configuration with Unbypassed R_e

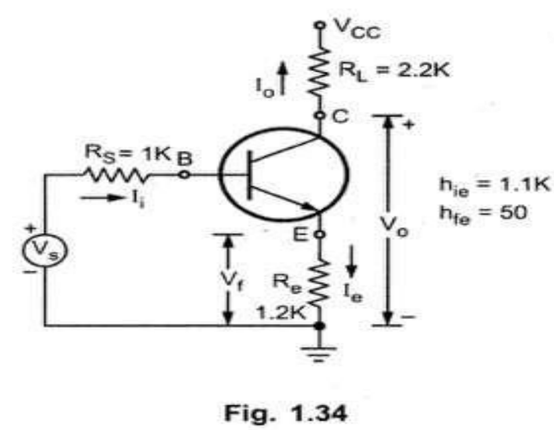


Fig. 1.34

Fig. 1.34 shows the common emitter circuit with unbypassed R_e. The common emitter circuit with unbypassed R_e is an example of current series feedback. In this configuration resistor R_e is common to base to emitter input circuit as well as collector to emitter output circuit and input current I_b as well as output current I_c both flow through it. The voltage drop across R_e, $V_f = (I_b + I_c) = I_e R_e = I_c R_e = - I_o R_e$. This voltage drop shows that the output current I_o is being sampled and it is converted to voltage by feedback network. At input side voltage V_f is subtracted from V_s to produce V_i. Therefore, the feedback applied in series.

Analysis

Step 1 : Identify topology

By opening the output loop, (output current, $I_o = 0$), feedback signal becomes zero and hence it is current sampling. Looking at Fig. 1.34 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a current series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

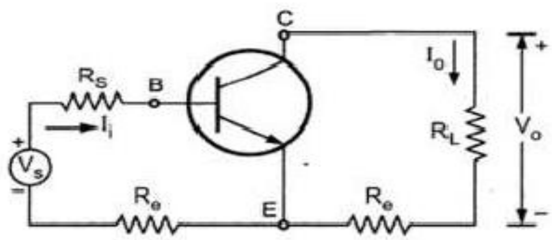


Fig. 1.35

To find input circuit set $I_o = 0$, then R_e appears at the input side. To find output circuit set $I_i = 0$, then R_e appears in the output circuit. The resulting circuit is shown in the Fig. 1.35.

Step 4 : Replace transistor with its approximate h-parameter equivalent circuit

Fig. 1.36 shows the approximate h-parameter equivalent circuit

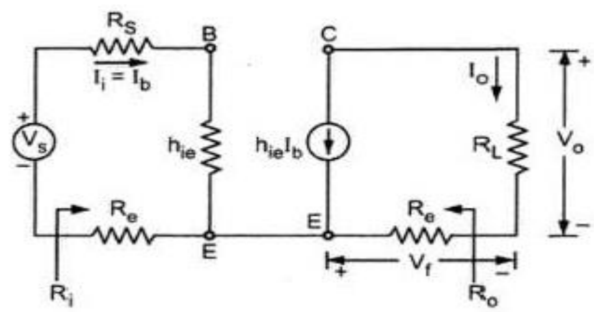


Fig. 1.36 Approximate h-parameter equivalent circuit

Step 5 : Find open loop transfer gain

$$G_M = \frac{I_o}{V_i} = \frac{-h_{fe}I_b}{V_s} \qquad \dots (9)$$

$$= \frac{-h_{fe}I_b}{I_b(R_s + h_{ie} + R_e)}$$

$$= \frac{-h_{fe}}{R_s + h_{ie} + R_e} = \frac{50}{1\,K + 1.1\,K + 1.2\,K}$$

$$= -0.015$$

Step 6 : Indicate $\mathbf{I_o}$ and $\mathbf{V_f}$ and calculate β

$$\beta = \frac{V_f}{I_o} = \frac{I_e R_e}{I_o} \qquad \dots(10)$$

$$= \frac{-I_o R_e}{I_o} = -R_e \qquad \because I_e = -I_o$$

$$= -1.2\ K$$

Step 7 : Calculate D, G_{Mf}, A_{Vf}, R_{if}, R_{of} and R'_{of}

$$D = 1+\beta G_M = 1+(-1.2K)\times(-0.015) \quad \dots (11)$$
$$= \mathbf{19.18}$$
$$G_{Mf} = \frac{G_M}{D} = \frac{-0.015}{19.18} \quad \dots (12)$$
$$= \mathbf{-0.782\times10^{-3}}$$

The voltage gain A_{Vf} is given as

$$A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s} = G_{Mf}\ R_L \quad \because G_{Mf} = \frac{I_o}{V_s} \dots (13)$$
$$= -0.782\times10^{-3}\times 2.2\,K$$
$$= \mathbf{-1.72}$$

Looking at Fig. 1.36 R_i can be given as

$$R_i = R_s + h_{ie} + R_e \quad \dots (14)$$
$$= 1K + 1.1\,K + 1.2\,K = \mathbf{3.3\,K}$$
$$R_{if} = R_i\ D = 3.3K\times19.18 \quad \dots (15)$$
$$= \mathbf{63.294\,K}$$

Looking at Fig. 1.36 R_o is given as

$$R_o = \infty \quad \dots (16)$$
$$\therefore \quad R_{of} = R_o\ D = \infty \quad \dots (17)$$
$$R'_{of} = R_{of} \parallel R_L \quad \dots (18)$$
$$= R_L \quad \because R_{of} = \infty$$
$$= \mathbf{2.2\,K}$$

1.12.3 Current Shunt Feedback

Fig. 1.40 shows two transistors in cascade connection with feedback from second emitter to first base through resistor R′. Here, the feedback network formed by R′ and R_{e2} divides the current I_e. Since $I_e = -I_o$, the feedback network gives current feedback. At input side, we see that $I_i = I_s - I_f$, i.e. I_f is shunt subtracted from I_s to get I_i. Therefore, this configuration is a current shunt feedback.

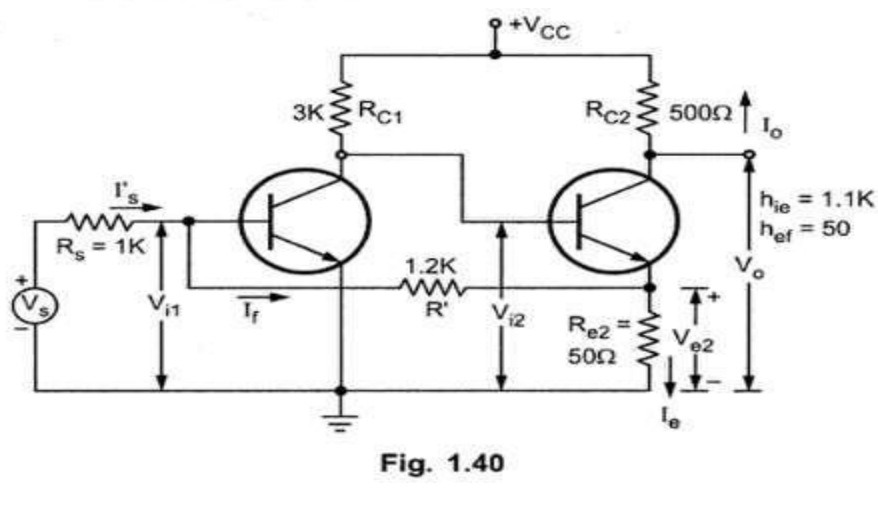


Fig. 1.40

Step 1 : Identify topology

By shorting output voltage ($V_o = 0$), feedback signal does not become zero and hence it is not voltage sampling. By opening the output loop ($I_o = 0$), feedback signal becomes zero and hence it is a current feedback. The feedback signal appears in shunt with input ($I_i = I_s - I_f$), hence the topology is current shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

The input circuit of the amplifier without feedback is obtained by opening the output loop at the emitter of Q_2 ($I_o = 0$). This places R′ in series with R_e from base to emitter of Q_1. The output circuit is found by shorting the input node (the base of Q_1), i.e. making $V_i = 0$. This places R′ in parallel with R_e. The resultant equivalent circuit is shown in Fig. 1.41.

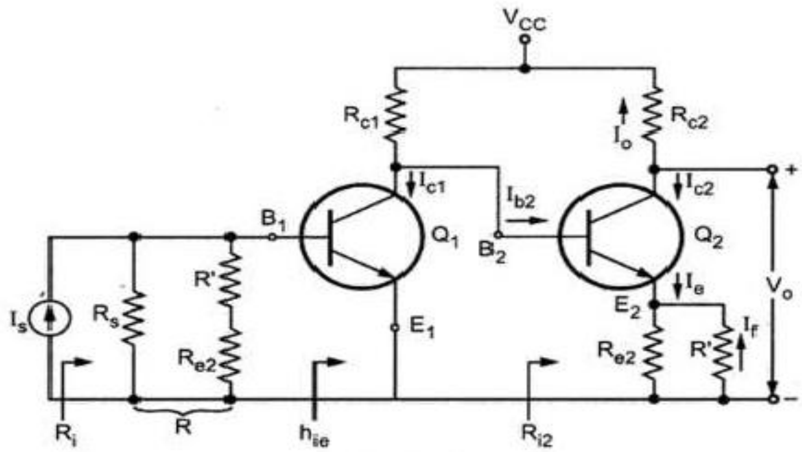


Fig. 1.41

Step 4 : Find open circuit transfer gain

$$A_I = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}}\frac{I_{b2}}{I_{c1}}\frac{I_{c1}}{I_{b1}}\frac{I_{b1}}{I_s} \qquad \dots (31)$$

We know that,

$$\frac{-I_{c2}}{I_{b2}} = A_{i2} = -h_{fe} = -50 \text{ and} \qquad \dots (32)$$

$$\frac{-I_{c1}}{I_{b1}} = A_{i1} = -h_{fe} = -50$$

$$\therefore \quad \frac{I_{c1}}{I_{b1}} = 50 \qquad \dots (33)$$

Looking at Fig. 1.41 we can write

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1}+R_{i2}} \qquad \dots (34)$$

where

$$R_{i2} = h_{ie} + (1 + h_{fe})\,(R_{e2} \parallel R')$$

$$= 1.1 + (51)\left(\frac{50 \times 1.2\text{ K}}{50 + 1.2\text{ K}}\right)$$

$$= \mathbf{3.55\ K}$$

$$\therefore \quad \frac{I_{b2}}{I_{c1}} = \frac{-3\,K}{3\,K + 3.55\,K} = -0.457$$

Looking at Fig. 1.41 we can write

$$\frac{I_{b1}}{I_s} = \frac{R}{R + h_{ie}} \quad \ldots (35)$$

$$\text{where } R = R_s \parallel (R' + R_e) = \frac{1.2\,K \times 1.25\,K}{1.2\,K + 1.25\,K}$$

$$= \mathbf{0.612\ K}$$

$$\therefore \quad \frac{I_{b1}}{I_s} = \frac{0.612\,K}{0.612 + 1.1\,K} = 0.358$$

Substituting the numerial values obtained from equations 32, 33, 34 and 35 in equation 31 we get,

$$A_I = (-50) \times (-0.457) \times (50) \times (0.358)$$

$$= \mathbf{406}$$

Step 5 : Calculate β

Looking at Fig. 1.41 we can write,

$$I_f = \frac{-I_e\,R_{e2}}{R_e + R'}$$

$$= \frac{-I_e\,R_{e2}}{R_e + R'} \qquad \because I_e \cong I_c$$

$$= \frac{I_o\,R_{e2}}{R_{e2} + R'} \qquad \because I_o = -I_c$$

$$\therefore \quad \beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2} + R'} = \frac{50}{50 + 1.2\,K}$$

$$= \mathbf{0.04}$$

Step 6 : Calculate D, R_i, R_{if}, A_{If}, A_{vf}, R_o, R_{of}

$$D = 1 + \beta A_I = 1 + (0.04) \times 406$$

$$= \mathbf{17.2}$$

$$A_{If} = \frac{A_I}{D} = \frac{406}{17.2}$$

$$= \mathbf{23.6}$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{-I_{c2}\,R_{c2}}{I_s\,R_s}$$

$$= \frac{A_{If}\,R_{c2}}{R_s} \qquad \because \frac{-I_{c2}}{I_s} = A_{If}$$

$$= \frac{(23.6)(500)}{1.2\,K}$$

$$= \mathbf{9.83}$$

$$R_i = R \parallel h_{ie} = \frac{0.612\,K \times 1.1K}{0.612\,K + 1.1K}$$

$$= \mathbf{0.394\ K}$$

$$R_{if} = \frac{R_i}{D} = \frac{0.394\text{ K}}{17.2}$$

$$= \mathbf{23\ \Omega}$$

$$R_o = \infty \qquad \because h_{oe} = 0$$

$$\therefore \quad R_{of} = R_o D = \infty$$

$$R'_o = R_o \parallel R_{c2} = \infty \parallel 500 = \mathbf{500\ \Omega}$$

1.12.4 Voltage Shunt Feedback

Fig. 1.42 shows a common emitter amplifier with a resistor R′ connected from the output to the input.

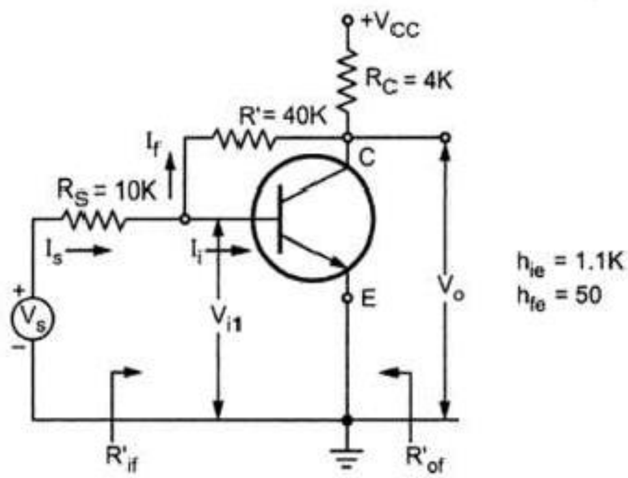


Fig. 1.42

Step 1 : Identify topology

The feedback current I_f is given as

$$I_f = \frac{V_i - V_o}{R'} \qquad \text{But } V_o > \beta V_i$$

$$\therefore \quad I_f \approx \frac{-V_o}{R'}$$

By shorting output voltage ($V_0 = 0$), feedback reduces to zero and hence it is a voltage sampling. As $I_i = I_s - I_f$, the mixing is shunt type and topology is voltage shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$, this places R′ between base and ground. To find output circuit, set $V_i = 0$, this places R′ between collector and ground.

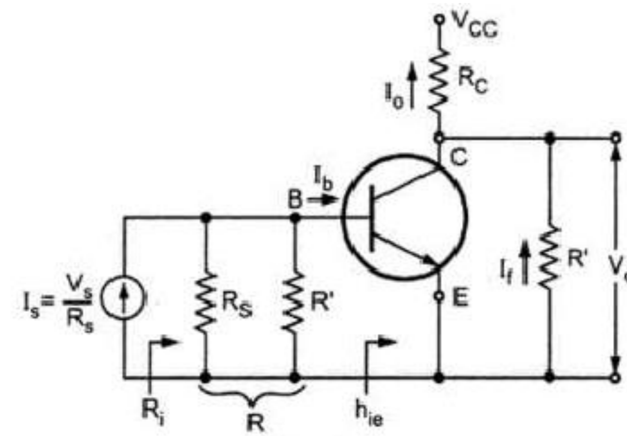


Fig. 1.43

The resultant circuit is shown in Fig. 1.43.

The feedback signal is the current I_f in the resistor R' which is in the output circuit as shown in the Fig. 1.43.

We have seen that

$$I_f = \frac{V_i - V_o}{R'} = \frac{-V_o}{R'} \qquad \because V_o > V_i$$

$$\therefore \qquad \frac{I_f}{V_o} = \beta = \frac{-1}{R'}$$

$$R_{Mf} = \frac{R_M}{1+\beta\ R_M} = \frac{1}{\beta} \qquad \because \beta R_M >> 1$$

$$= -R'$$

$$\therefore \qquad A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s\ R_s}$$

$$\approx \frac{1}{\beta R_s} = \frac{-R'}{R_s}$$

Step 4 : Find the open circuit transresistance

$$R_M = \frac{V_o}{I_s} = \frac{I_o\ R'_c}{I_s} = \frac{-I_c\ R'_c}{I_s} \qquad \text{... (36)}$$

where $\qquad R'_c = R_c \parallel R' = 4\text{ K} \parallel 40\text{ K}$

$$= \mathbf{3.636\ K}$$

and $\qquad \frac{-I_c}{I_s} = \frac{-I_c}{I_b}\frac{I_b}{I_s}$

$$\frac{-I_c}{I_b} = A_i = -h_{fe} = \mathbf{-50} \text{ and} \qquad \text{... (37)}$$

$$\frac{I_b}{I_s} = \frac{R}{R+h_{ie}} \qquad \text{where } R = R_S \parallel R' = 10\text{ K} \parallel 40\text{ K} = 8\text{ K}$$

$$\therefore \qquad \frac{I_b}{I_s} = \frac{8\text{ K}}{8\text{ K}+1.1\text{ K}}$$

$$= \mathbf{0.879} \qquad \text{... (38)}$$

Substituting values of equation 37 and 38 in equation 36 we have

$$R_M = \frac{-I_c R'_c}{I_s} = \frac{-I_c}{I_b}\frac{I_b}{I_s} \times R'_c$$

$$= (-50) \times (0.879) \times 3.636 \text{ K}$$

$$= \mathbf{-159.8 \text{ K}}$$

Step 5 : Calculate β

$$\beta = \frac{-1}{R'} = \frac{-1}{40 \text{ K}}$$

$$= -2.5 \times 10^{-5}$$

Step 6 : Calculate D, R_{MF}, A_{VF}, R_{iF}, R_{of} and R'_{of}

$$D = 1 + \beta R_M$$

$$= 1 + (-2.5 \times 10^{-5})(-159.8 \times 10^3)$$

$$= \mathbf{4.995}$$

$$R_{MF} = \frac{R_M}{D} = \frac{-159.8 \text{ K}}{4.995}$$

$$= \mathbf{-32 \text{ K}}$$

$$A_{VF} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{MF}}{R_s}$$

$$= \frac{-32 \text{ K}}{10 \text{ K}} = \mathbf{-3.2}$$

Looking at Fig. 1.43 we can write

$$R_i = R \parallel h_{ie} = \frac{R\, h_{ie}}{R + h_{ie}}$$

$$= \frac{8 \text{ K} \times 1.1 \text{ K}}{8 \text{ K} + 1.1 \text{ K}} = 0.967 \text{ K}$$

$$R_{if} = \frac{R_i}{D} = \frac{0.967 \text{ K}}{4.995}$$

$$= \mathbf{193.59\ \Omega}$$

$$R_o = \infty \qquad \because h_{oe} = 0$$

$$\therefore \quad R_{of} = \frac{\infty}{D} = \infty$$

$$R'_o = R_o \parallel R'_c = \infty \parallel 3.636 \text{ K}$$

$$= 3.636 \text{ K}$$

$$R'_{of} = \frac{R'_o}{D} = \frac{3.636 \text{ K}}{4.995}$$

$$= 728\ \Omega$$

Example 1.2 : *A feedback amplifier has an open loop gain of 600 and feedback factor $\beta = 0.01$. Find the closed loop gain with negative feedback.* **(Nov./Dec.-2004)**

Solution :

$$A_{vf} = \frac{A}{1+A\beta} = \frac{600}{1+600\times 0.01}$$

$$= \mathbf{85.714}$$

Example 1.3 : *The distortion in an amplifier is found to be 3%, when the feedback ratio of negative feedback amplifier is 0.04. When the feedback is removed, the distortion becomes 15%. Find the open and closed loop gain.* **(April/May-2005)**

Solution : Given : $\beta = 0.04$ Distortion with feedback = 3%, Distortion without feedback = 15 %

$$\therefore \quad D = \frac{15}{3} = 5 \quad \text{where } D = 1 + A\beta = 5$$

$$\therefore \quad 5 = 1 + A\beta = 1 + A \times 0.04$$

$$\therefore \quad A = 100$$

Example 1.4 : *An amplifier has mid-band voltage gain ($A_{v\,mid}$) of 1000 with $f_L = 50$ Hz and $f_H = 50$ kHz, if 5% feedback is applied then calculate gain f_L, and f_H with feedback.*

Solution : Given $\beta = \frac{5}{100} = 0.05$, $f_L = 50$, $f_H = 50$ kHz and $A_{v\,mid} = 1000$

a) Gain with feedback

$$A_{v\,mid\,f} = \frac{A_{v\,mid}}{1+\beta A_{v\,mid}} = \frac{1000}{1+0.05\times 1000}$$

$$= \mathbf{19.6}$$

b)

$$f_{Lf} = \frac{f_L}{1+\beta A_{v\,mid}} = \frac{50}{1+0.05\times 1000}$$

$$= \mathbf{0.98\ Hz}$$

c)

$$f_{Hf} = f_H \times (1+\beta A_{v\,mid}) = 50\times 10^3 \times (1+0.05\times 1000)$$

$$= \mathbf{2.55\ MHz}$$

Example 1.5 : *An amplifier with open loop voltage gain of 1000 delivers 10 W of power output at 10% second harmonic distortion when i/p is 10 mV. If 40 dB negative feedback is applied and output power is to remain at 10W, determine required input signal V_s and second harmonic distortion with feedback.*

Solution : Given $A_v = 1000$, Output power = 10W,

a) β :

$$-40 = 20 \log\left[\frac{1}{1+\beta A}\right]$$

$$\therefore \quad 1+\beta A = 100$$

$$\therefore \quad \beta A = 99$$

$$\therefore \quad \beta = \frac{99}{1000} = \mathbf{0.099}$$

Gain of the amplifier with feedback is given as

$$A_{vf} = \frac{A_v}{1+\beta A_v} = \frac{1000}{100} = \mathbf{10}$$

b) To maintain output power 10W, we should maintain output voltage constant and to maintain output voltage constant with feedback gain required V_s is

$$V_{sf} = V_s \times 100 = 10\text{mV} \times 100$$

$$= \mathbf{1V}$$

c) Second harmonic distortion is reduced by factor $1+\beta A$.

$$\therefore \quad D_{2f} = \frac{D_2}{1+\beta A} = \frac{0.1}{1+\beta A}$$

$$= \frac{0.1}{100} = 0.001$$

$$= \mathbf{0.1\ \%}$$

Example 1.6 : *An amplifier with open loop gain of A = 2000 ± 150 is available. It is necessary to have the amplifier whose voltage gain varies by not more than ± 0.2%. Calculate β and* A_f

Solution : a) We know that

$$\frac{dA_f}{A_f} = \frac{1}{1+\beta A}\ \frac{dA}{A}$$

$$\therefore \quad \frac{0.2}{100} = \frac{1}{1+\beta A} \times \frac{150}{2000}$$

$$\therefore \quad 1+\beta A = 37.5$$

$$\therefore \quad \beta A = 36.5$$

$$\therefore \quad \beta = \frac{36.5}{2000} = 0.01825$$

$$= \mathbf{1.825\%}$$

b) A_F :

$$A_F = \frac{A}{1+\beta A} = \frac{2000}{1+0.01825 \times 2000}$$

$$= \mathbf{53.33}$$

Oscillators:

2.1 Introduction

The operation of the feedback amplifiers in which the negative feedback is used, has been discussed earlier. In this chapter, a device which works on the principle of positive feedback is discussed. The device is called an **Oscillator**.

Key Point *: An oscillator is a circuit which basically acts as a generator, generating the output signal which oscillates with constant amplitude and constant desired frequency.*

An oscillator does not require any input signal. An electrical device, alternator generates a sinusoidal voltage at a desired frequency of 50 Hz in our nation but electronic oscillator can generate a voltage of any desired waveform at any frequency. An oscillator can generate the output waveform of high frequency upto gigahertz.

In short, an oscillator is an amplifier, which uses a positive feedback and without any external input signal, generates an output waveform at a desired frequency. This chapter explains the various types of oscillator circuits.

2.2 Basic Theory of Oscillators

The feedback is a property which allows to feedback the part of the output, to the same circuit as its input. Such a feedback is said to be positive whenever the part of the output that is fed back to the amplifier as its input, is in phase with the original input signal applied to the amplifier. Consider a non-inverting amplifier with the voltage gain A as shown in the Fig. 2.1.

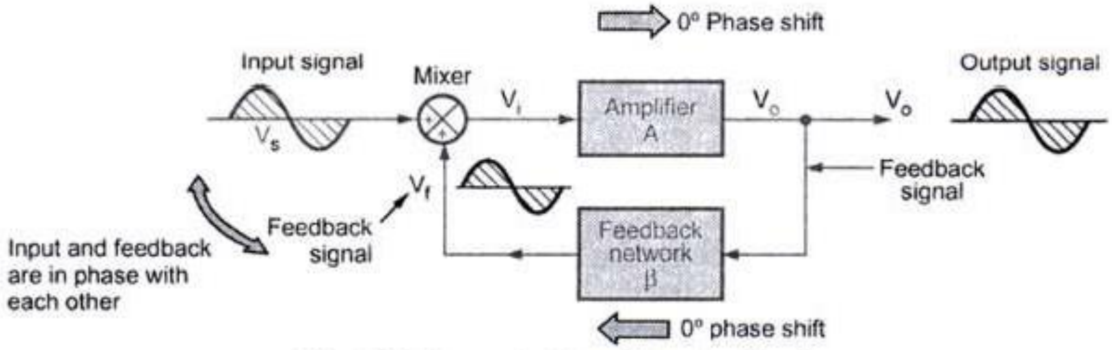


Fig. 2.1 Concept of positive feedback

(2 - 1)

Assume that a sinusoidal input signal (voltage) V_s is applied to the circuit. As amplifier is non-inverting, the output voltage V_o is in phase with the input signal V_s. The part of the output is fed back to the input with the help of a feedback network. How much part of the output is to be fed back, gets decided by the feedback network gain β. No phase change is introduced by the feedback network. Hence the feedback voltage V_f is in phase with the input signal V_s.

Key Point : *As the phase of the feedback signal is same as that of the input applied, the feedback is called* ***positive feedback****.*

The amplifier gain is A i.e. it amplifies its input V_i, A times to produce output V_o.

$$\therefore \qquad \boxed{A = \frac{V_o}{V_i}}$$

This is called **open loop** gain of the amplifier.

For the overall circuit, the input is supply voltage V_s and net output is V_o. The ratio of output V_o to input V_s considering effect of feedback is called **closed loop** gain of the circuit or gain with feedback denoted as A_f.

$$\therefore \qquad \boxed{A_f = \frac{V_o}{V_s}}$$

The feedback is positive and voltage V_f is added to V_s to generate input of amplifier V_i. So referring Fig. 2.1 we can write,

$$V_i = V_s + V_f \qquad \text{...(1)}$$

The feedback voltage V_f depends on the feedback element gain β. So we can write,

$$V_f = \beta V_o \qquad \text{... (2)}$$

Substituting equation (2) in equation (1),

$$V_i = V_s + \beta V_o$$

$$\therefore \qquad V_s = V_i - \beta V_o \qquad \text{... (3)}$$

Substituting in expression for A_f,

$$A_f = \frac{V_o}{V_i - \beta V_o}$$

Dividing both numerator and denominator by V_i,

$$\therefore \qquad A_f = \frac{(V_o / V_i)}{1 - \beta (V_o / V_i)}$$

$$\therefore \qquad \boxed{A_f = \frac{A}{1 - A\beta}} \qquad \text{... as } A = \frac{V_o}{V_i}$$

Now consider the various values of β and the corresponding values of A_f for constant amplifier gain of A = 20.

A	β	A_f
20	0.005	22.22
20	0.04	100
20	0.045	200
20	0.05	∞

Table 2.1

The above result shows that the gain with feedback increases as the amount of positive feedback increases. In the limiting case, the gain becomes infinite. This indicates that circuit can produce output without external input ($V_s = 0$), just by feeding the part of the output as its own input. Similarly, output cannot be infinite but gets driven into the oscillations. In other words, the circuit stops amplifying and starts oscillating.

Key Point : *Thus without an input, the output will continue to oscillate whose frequency depends upon the feedback network or the amplifier or both. Such a circuit is called as an* ***oscillator***.

It must be noted that β the feedback network gain is always a fraction and hence $\beta < 1$. So the feedback network is an attenuation network. To start with the oscillations $A\beta > 1$ but the circuit adjusts itself to get $A\beta = 1$, when it produces sinusoidal oscillations while working as an oscillator.

2.3 Barkhausen Criterion

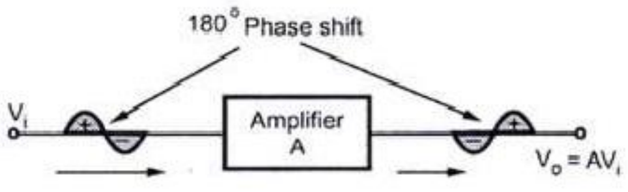


Fig. 2.2 Inverting amplifier

Consider a basic inverting amplifier with an open loop gain A. The feedback network attenuation factor β is less than unity. As basic amplifier is inverting, it produces a phase shift of 180° between input and output as shown in the Fig. 2.2.

Now the input V_i applied to the amplifier is to be derived from its output V_o using feedback network.

But the feedback must be positive i.e. the voltage derived from output using feedback network must be in phase with V_i. Thus the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input. This ensures positive feedback.

The arrangement is shown in the Fig. 2.3.

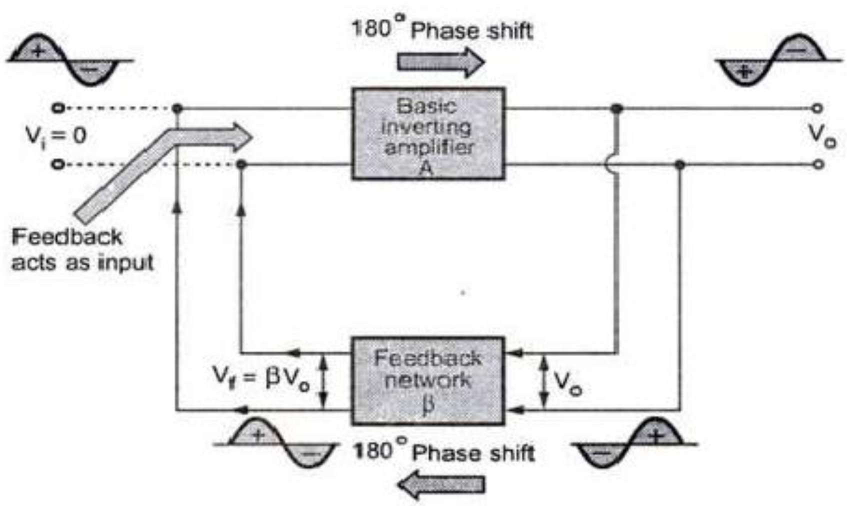


Fig. 2.3 Basic block diagram of oscillator circuit

Consider a fictitious voltage V_i applied at the input of the amplifier. Hence we get,

$$V_o = A V_i \quad \ldots(1)$$

The feedback factor β decides the feedback to be given to input,

$$V_f = -\beta V_o \quad \ldots(2)$$

Negative sign indicates 180° phase shift.

Substituting equation (2) into equation (1) we get,

$$V_f = -A \beta V_i \quad \ldots(3)$$

For the oscillator, we want that feedback should drive the amplifier and hence V_f must act as V_i.

Now if V_f has to be equal to V_i,

$$V_i = -A \beta V_i \quad \ldots(4)$$

This will get satisfied only when,

$$\boxed{-A \beta = 1} \quad \ldots(5)$$

The $-A\beta = 1$ condition is called **Barkhausen criterion.**

$$\therefore \quad A\beta = -1 + j0 \quad \ldots(6)$$

Equating magnitudes of both sides,

$$|A \beta| = |-1 + j0|$$

i.e.

$$\boxed{|A \beta| = 1} \quad \ldots(7)$$

And the phase of V_f must be same as V_i i.e. feedback network should introduce 180° phase shift in addition to 180° phase shift introduced by inverting amplifier. This ensures positive feedback. **So total phase shift around a loop is 360°.**

In this condition, V_f drives the circuit and without external input, circuit works as an oscillator.

The two conditions discussed above, required to work the circuit as an oscillator are called **Barkhausen Criterion** for oscillation.

The **Barkhausen Criterion** states that :

1. The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely 0° or 360°, or ofcourse an integral multiple of 2π radians.
2. The magnitude of the product of the open loop gain of the amplifier (A) and the feedback factor β is unity i.e. $|A\beta| = 1$.

2.3.1 | Aβ | > 1

When the total phase shift around a loop is 0° or 360° and | Aβ | > 1, then the output oscillates but the oscillations are of growing type. The amplitude of oscillations goes on increasing as shown in the Fig. 2.4.

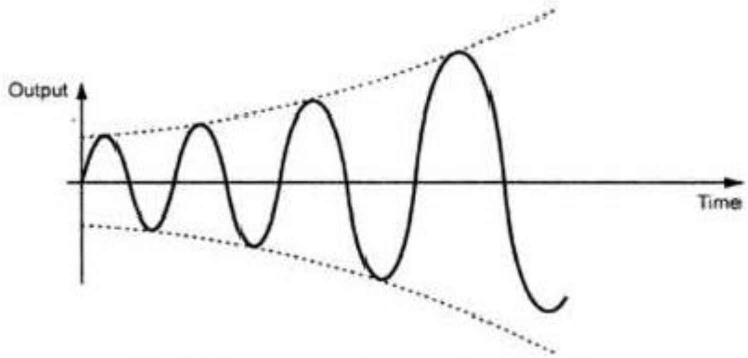


Fig. 2.4 Growing type of oscillations

2.3.2 | Aβ | = 1

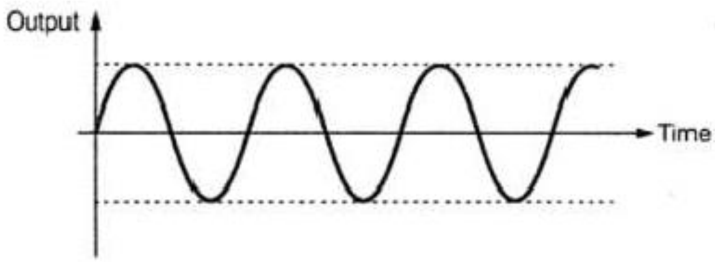


Fig. 2.5 Sustained oscillations

As stated by Barkhausen criterion, when total phase shift around a loop is 0° or 360° ensuring positive feedback and |Aβ| = 1 then the oscillations are with constant frequency and amplitude called **sustained oscillations.** Such oscillations are shown in the Fig. 2.5.

2.3.3 | Aβ | < 1

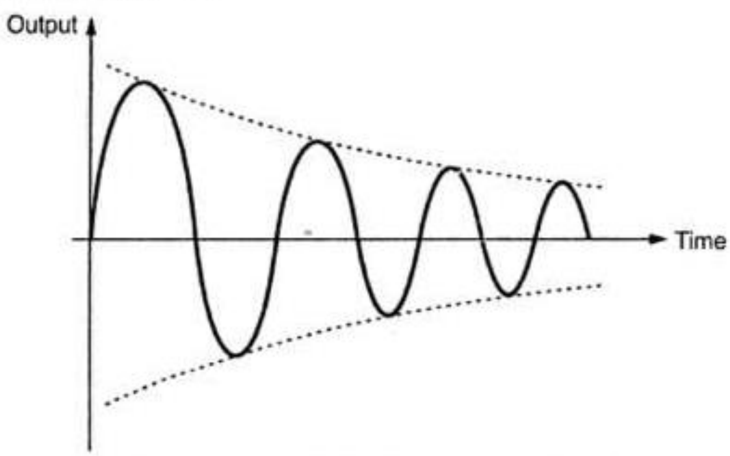


Fig. 2.6 Exponentially decaying oscillations

When total phase shift around a loop is 0° or 360° but |Aβ| < 1 then the oscillations are of decaying type i.e. such oscillation amplitude decreases exponentially and the oscillations finally cease. Thus circuit works as an amplifier without oscillations. The decaying oscillations are shown in the Fig. 2.6.

So to start the oscillations without input, |Aβ| is kept higher than unity and then circuit adjusts itself to get |A β| = 1 to result sustained oscillations.

2.4 Classification of Oscillators

The oscillators are classified based on the nature of the output waveform, the parameters used, the range of frequency etc. The various ways in which oscillators are classified as ;

2.4.1 Based on the Output Waveform

Under this, the oscillators are classified as sinusoidal and nonsinusoidal oscillators. The sinusoidal oscillators generate purely sinusoidal waveform at the output. While nonsinusoidal oscillators generate an output waveform as triangular, square, sawtooth etc. In this chapter, we are going to discuss only sinusoidal oscillators.

2.4.2 Based on the Circuit Components

The oscillators using the components resistance (R) and capacitor (C), are called RC oscillators. While the oscillators using the components inductance (L) and capacitor (C), are called LC oscillators. In some oscillators, crystal is used, which are called crystal oscillators.

2.4.3 Based on the Range of Operating Frequency

If the oscillators are used to generate the oscillations at audio frequency range which is 20 Hz to 100-200 kHz, then the oscillators are classified as low frequency (L.F.) or audio frequency (A.F.) oscillators. While the oscillators used at the frequency range more than 200-300 kHz upto gigahertz (GHz) are classified as high frequency (H.F.) or radio frequency (R.F.) oscillators. The RC oscillators are used at low frequency range while the LC oscillators are used at high frequency range. At low frequencies, the value of inductor required is large. The large inductor is larger in size and occupies lot of space. It increases size and cost of the circuit. Hence **LC oscillators are not used for low frequency ranges.**

2.4.4 Based on : Whether Feedback is Used or Not ?

The oscillators in which the feedback is used, which satisfies the required conditions, are classified as feedback type of oscillators. The oscillators in which the feedback is not used to generate the oscillations, are classified as nonfeedback oscillators. The nonfeedback oscillators use the negative resistance region of the characteristics of the device used. The example of the nonfeedback type of oscillator is the UJT relaxation oscillator.

RC Phase Shift Oscillator:

2.5 R-C Phase Shift Oscillator

RC phase shift oscillator basically consists of an amplifier and a feedback network consisting of resistors and capacitors arranged in ladder fashion. Hence such an oscillator is also called **ladder type RC phase shift oscillator**.

To understand the operation of this oscillator let us study RC circuit first, which is used in the feedback network of this oscillator. The Fig. 2.7 shows the basic RC circuit.

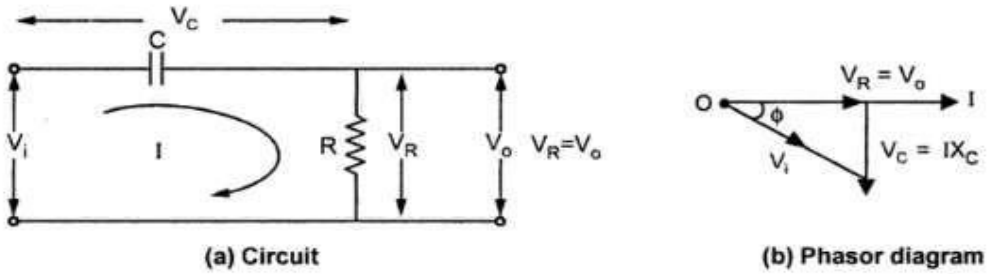


Fig. 2.7

The capacitor C and resistance R are in series. Now X_C is the capacitive reactance in ohms given by,

$$X_C = \frac{1}{2\pi f C} \quad \Omega$$

The total impedance of the circuit is,

$$Z = R - j X_C = R - j\left(\frac{1}{2\pi f C}\right) \quad \Omega$$

$$= |Z| \angle -\phi^\circ \ \Omega$$

The r.m.s. value of the input voltage applied is say V_i volts. Hence the current is given by,

$$I = \frac{V_i \angle 0^\circ}{Z}$$

$$= \frac{V_i \angle 0^\circ}{|Z| \angle -\phi}$$

$$\therefore \quad I = \frac{V_i}{Z} \angle +\phi \quad A$$

where $|Z| = \sqrt{R^2 + (X_C)^2}$

and $\phi = \tan^{-1}\left(\frac{X_C}{R}\right)$

From expression of current it can be seen that current **I leads input voltage V_i by angle ϕ.**

The output voltage V_o is the drop across resistance R given by,

$$V_o = V_R = IR$$

The voltage across the capacitor is,

$$V_C = I X_C$$

The drop V_R is in phase with current I while the drop V_C lags current I by 90° i.e. I leads V_C by 90°. The phasor diagram is shown in the Fig. 2.7 (b).

Key Point : *By using proper values of R and C,* ***the angle ϕ is adjusted in practice equal to 60°.***

2.5.1 RC Feedback Network

As stated earlier, RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. Thus if one RC network produces phase shift of $\phi = 60°$ then to produce phase shift of 180° such three RC networks must be connected in cascade. Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60°, thus total phase shift due to feedback is 180° ($3 \times 60°$). Such a feedback network is shown in the Fig. 2.8.

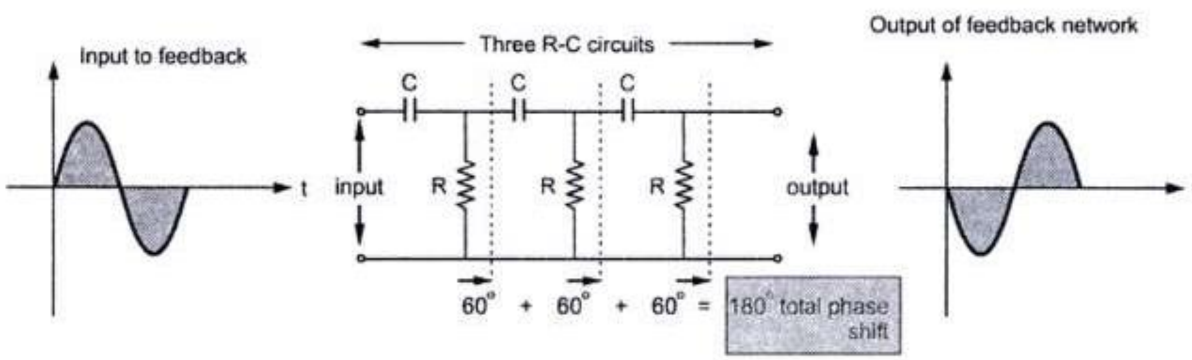


Fig. 2.8 Feedback network in RC phase shift oscillator

The network is also called the **ladder network**. All the resistance values and all the capacitance values are same, so that for a particular frequency, each section of R and C produces a phase shift of 60°.

2.5.2 Transistorised RC Phase Shift Oscillator

In a practical, transistorised RC phase shift oscillator, a transistor is used as an active element of the amplifier stage.

The Fig. 2.9 shows a practical transistorised RC phase shift oscillator which uses a common emitter single stage amplifier and a phase shifting network consisting of three identical RC sections.

The output of the feedback network gets loaded due to the low input impedance (h_{ie}) of a transistor. Hence an emitter follower input stage before the common emitter amplifier stage can be used, to avoid the problem of low input impedance. But if only single stage is to be used then the voltage shunt feedback, denoted by resistance R_3 in the Fig. 2.9 is used, connected in series with the amplifier input resistance.

A phase shifting network is a feedback network, so output of the amplifier is given as an input to the feedback network. While the output of the feedback network is given as an input to the amplifier. Thus amplifier supplies its own input, through the feedback network.

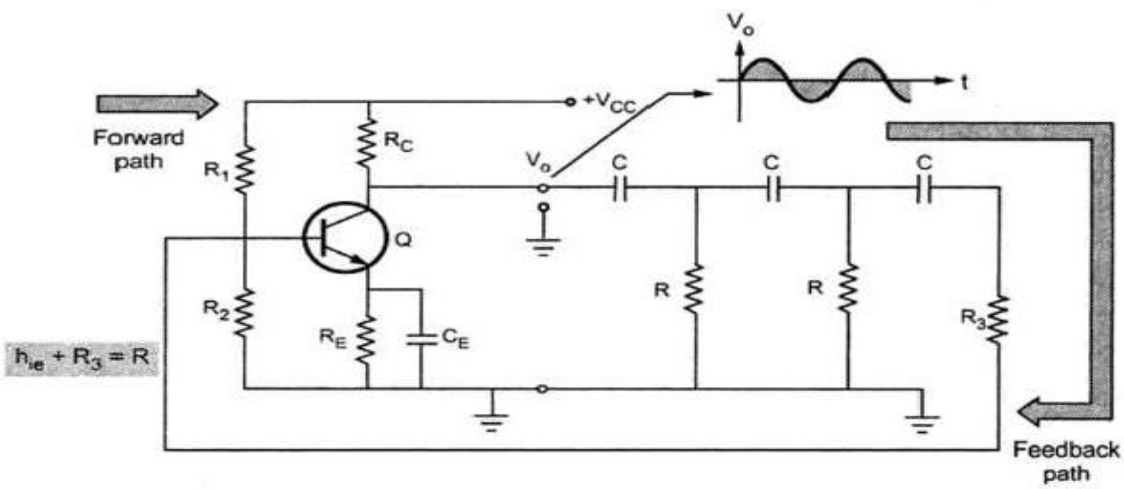


Fig. 2.9 Transistorised RC phase shift oscillator

Neglecting R_1 and R_2, as these are sufficiently large, we can write,

$$h_{ie} = \text{Input impedance of the amplifier stage}$$

Now the resistance R_3 and h_{ie} are in series and the value of R_3 is so selected such that the resultant of the two resistance is R, which is the required value of the resistance, in the last section of RC phase shifting network.

$$\therefore \quad \boxed{h_{ie} + R_3 = R} \quad \dots (1)$$

This ensures that all the three sections of the phase shifting network are identical.

Note : If the resistances R_1 and R_2 are not neglected then the input impedance of the amplifier stage becomes as,

$$\boxed{R_i' = R_1 \,||\, R_2 \,||\, h_{ie}} \quad \dots (1\text{ a})$$

In such a case, the value of R_3 must be so selected that

$$\boxed{R_i' + R_3 = R} \quad \dots (1\text{ b})$$

2.5.3 Derivation for the Frequency of Oscillations

Replacing the transistor by its approximate h-parameter model, we get the equivalent oscillator circuit as shown in the Fig. 2.10.

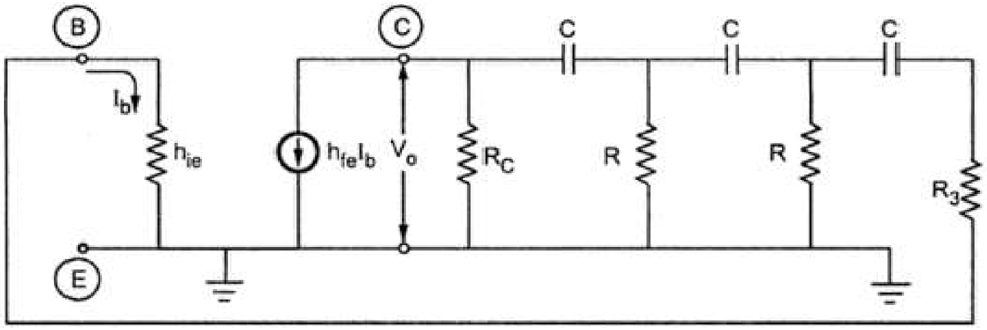


Fig. 2.10 Equivalent circuit using h-parameter model

Now we can replace h_{ie} + R_e as R, from the equation (1). Similarly we can replace, the current source h_{fe} I_b by its equivalent voltage source. And assume the ratio of the resistance R_C to R be k.

$$\therefore \qquad \boxed{k = \frac{R_C}{R}}$$

The modified equivalent circuit is shown in the Fig. 2.11.

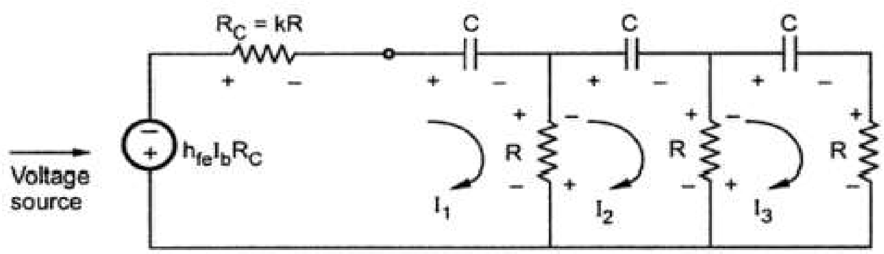


Fig. 2.11 Modified equivalent circuit

Applying KVL for the various loops in the modified equivalent circuit we get,

For Loop 1,

$$-I_1 R_C - \frac{1}{j\omega C} I_1 - I_1 R + I_2 R - h_{fe} I_b R_C = 0$$

Replacing R_C by kR and $j\omega$ by s we get,

$$\therefore \qquad + I_1 \left[(k+1) R + \frac{1}{sC}\right] - I_2 R = -hfe\, I_b\, kR \qquad \text{... (2)}$$

For Loop 2,

$$-\frac{1}{j\omega C} I_2 - I_2 R - I_2 R + I_1 R + I_3 R = 0$$

$$\therefore \qquad -I_1 R + I_2\left[2R + \frac{1}{sC}\right] - I_3 R = 0 \qquad \text{... (3)}$$

For Loop 3,

$$-I_3\frac{1}{j\omega C}-I_3R-I_3R+I_2R = 0$$

$$\therefore \qquad -I_2R+I_3\left[2R+\frac{1}{sC}\right] = 0 \qquad \dots (4)$$

Using Cramer's Rule to solve for I_3,

$$D = \begin{vmatrix} (k+1)R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{vmatrix}$$

$$= \left[(k+1)R+\frac{1}{sC}\right]\left[2R+\frac{1}{sC}\right]^2 - R^2\left[2R+\frac{1}{sC}\right] - R^2\left[(k+1)R+\frac{1}{sC}\right]$$

$$= \frac{[sRC(k+1)+1][2sCR+1]^2}{s^3C^3} - \frac{R^2(2sCR+1)}{sC} - \frac{R^2[(k+1)sRC+1]}{sC}$$

First term can be written as,

$[skRC + sRC + 1][4s^2C^2R^2 + 4sRC + 1]/s^3C^3$

$$= \frac{4s^3kR^3C^3 + 4s^3R^3C^3 + 4s^2C^2R^2 + 4s^2kR^2C^2 + 4s^2R^2C^2 + 4sRC + skRC + sRC + 1}{s^3C^3}$$

Second and the Third term can be combined to get,

$$= \frac{-R^2[ksRC + sRC + 1] - R^2[1+2sRC]}{sC}$$

$$= \frac{-[2R^2 + 3sR^3C + ksR^3C]}{sC}$$

Combining the two terms and taking LCM as s^3C^3 we get,

$$D = \frac{s^3C^3R^3[4k+4] + s^2C^2R^2[4k+8] + sRC[5+K] + 1 - [2R^2 + 3sR^3C + ksR^3C]s^2C^2}{s^3C^3}$$

$$= \frac{s^3C^3R^3[3k+1] + s^2C^2R^2[4k+6] + sRC[5+k] + 1}{s^3C^3} \qquad \dots (5)$$

Now

$$D_3 = \begin{vmatrix} (k+1)R+\frac{1}{sC} & -R & -h_{fe}I_bkR \\ -R & 2R+\frac{1}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= -R^2(h_{fe}I_bkR)$$

$$= -kR^3h_{fe}I_b \qquad \dots (6)$$

$\therefore \quad I_3 = \frac{D_3}{D}$

$$\therefore \quad \boxed{I_3 = \frac{-kR^3\, h_{fe}\, I_b\, s^3\, C^3}{s^3\, C^3\, R^3\,[3k+1] + s^2\, C^2\, R^2\,[4K+6] + sRC\,[5K+1] + 1}} \quad \ldots (7)$$

Now $\quad I_3$ = Output current of the feedback circuit.

I_b = Input current of the amplifier.

$I_c = h_{fe}\, I_b$ = Input current of the feedback circuit.

$$\therefore \quad \beta = \frac{\text{Output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{h_{fe}\, I_b}$$

$$\text{And} \quad A = \frac{\text{Output of amplifier circuit}}{\text{Input to amplifier circuit}} = \frac{I_3}{I_b} = h_{fe}$$

$$\therefore \quad \boxed{A\beta = \frac{I_3}{h_{fe}\, I_b} \times h_{fe} = \frac{I_3}{I_b}} \quad \ldots (8)$$

Using equation (8) we get,

$$A\beta = \frac{-kR^3\, h_{fe}\, s^3\, C^3}{s^3\, C^3\, R^3\,[3k+1] + s^2\, C^2\, R^2\,[4k+6] + sRC\,[5k+1] + 1} \quad \ldots (9)$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = j^3\omega^3 = -j\omega^3$ in the equation (9) we get,

$$A\beta = \frac{-j\omega^3\, kR^3\, C^3\, h_{fe}}{-j\omega^3\, C^3\, R^3\,[3k+1] - \omega^2\, C^2\, R^2\,[4k+6] + j\omega RC\,[5+k] + 1}$$

Separating the real and imaginary parts in the denominator we get,

$$A\beta = \frac{-j\omega^3\, kR^3\, C^3\, h_{fe}}{[1 - 4k\omega^2\, C^2\, R^2 - 6\omega^2\, C^2\, R^2] - j\omega[3k\,\omega^2\, R^3\, C^3 + \omega^2\, R^3\, C^3 - 5RC - kRC]}$$

Dividing numerator and denominator by $j\omega^3\, R^3\, C^3$,

$$A\beta = \frac{k h_{fe}}{\left\{\dfrac{(1 - 4k\omega^2\, C^2\, R^2 - 6\omega^2\, C^2\, R^2)}{-j\omega^3\, R^3\, C^3}\right\} - \left\{\dfrac{j\omega[3k\,\omega^2\, R^3\, C^3 + \omega^2\, R^3\, C^3 - 5RC - kRC]}{-j\omega^3\, R^3\, C^3}\right\}}$$

Replacing $-1/j = j$,

$$= \frac{k h_{fe}}{j\left\{\dfrac{1}{\omega^3\, R^3\, C^3} - \dfrac{4k}{\omega RC} - \dfrac{6}{\omega RC}\right\} + \left\{3k + 1 - \dfrac{5}{\omega^2\, R^2\, C^2} - \dfrac{k}{\omega^2\, R^2\, C^2}\right\}}$$

Replacing $\frac{1}{\omega RC} = \alpha$ for simiplicity

$$\therefore \quad \boxed{A\beta = \frac{k h_{fe}}{[3k + 1 - 5\alpha^2 - k\alpha^2] + j[\alpha^3 - 4k\alpha - 6\alpha]}} \quad \ldots (10)$$

As per the Barkhausen Criterion, $\angle A\beta = 0°$. Now the angle of numerator term kh_{fe} of the equation (10) is 0° hence to have angle of the $A\beta$ term as 0°, the imaginary part of the denominator term must be 0.

$$\therefore \quad \alpha^3 - 4k\alpha - 6\alpha = 0$$

$$\alpha(\alpha^2 - 4k - 6) = 0$$

$$\therefore \quad \alpha^2 = 4k + 6 \text{ neglecting zero value}$$

$$\therefore \quad \boxed{\alpha = \sqrt{4k+6}}$$

$$\therefore \quad \frac{1}{\omega RC} = \sqrt{4k+6}$$

$$\therefore \quad \boxed{\omega = \frac{1}{RC\sqrt{4k+6}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi RC\sqrt{4k+6}}} \qquad \ldots (11)$$

This is the frequency at which $\angle A\beta = 0°$. At the same frequency, $|A\beta| = 1$.

Substituting $\alpha = \sqrt{4k+6}$ in the equation (10) we get,

$$A\beta = \frac{kh_{fe}}{3k+1-(4k+6)[5+k]} = \frac{kh_{fe}}{3k+1-20k-30-4k^2-6k}$$

$$= \frac{kh_{fe}}{-4k^2-23k-29}$$

Now $\quad |A\beta| = 1$

$$\therefore \quad \left|\frac{kh_{fe}}{-4k^2-23k-29}\right| = 1$$

$$\therefore \quad kh_{fe} = 4k^2 + 23k + 29$$

$$\boxed{h_{fe} = 4k + 23 + \frac{29}{k}} \qquad \ldots (12)$$

This must be the value of h_{fe} for the oscillations.

2.5.4 Minimum Value of h_{fe} for the Oscillations

To get minimum value of h_{fe},

$$\frac{d\,h_{fe}}{dk} = 0$$

$$\therefore \quad \frac{d}{dk}\left[4\,k + 23 + \frac{29}{k}\right] = 0$$

$$\therefore \quad \left[4 - \frac{29}{k^2}\right] = 0$$

$$\therefore \quad k^2 = \frac{29}{4}$$

$$\therefore \quad \boxed{k = 2.6925 \text{ for minimum } h_{fe}} \qquad \ldots (13)$$

Substituting in the equation (12),

$$(h_{fe})_{min} = 4\,(2.6925) + 23 + \frac{29}{(2.6925)}$$

$$\therefore \quad \boxed{(h_{fe})_{min} = 44.54} \qquad \ldots (14)$$

> **Key Point** : *Thus for the circuit to oscillate, we must select the transistor whose $(h_{fe})_{min}$ should be greater than 44.54.*

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. **Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.**

Example 2.2 : *Find the capacitor C and h_{fe} for the transistor to provide a resonating frequncy of 10 kHz of a transistorised phase shift oscillator. Assume R_1 = 25 kΩ, R_2 = 57 kΩ, R_C = 20 kΩ, R = 7.1 kΩ and h_{ie} = 1.8 kΩ.*

$$R_i' = R_1 \parallel R_2 \parallel h_{ie} = 25 \text{ k}\Omega \parallel 57 \text{ k}\Omega \parallel 1.8 \text{ k}\Omega$$

$$\frac{1}{R_i'} = \frac{1}{25} + \frac{1}{57} + \frac{1}{1.8}$$

$$\therefore \quad R_i' = 1.631 \text{ k}\Omega$$

Now $\quad R_i' + R_3 = R$

$$\therefore \quad R_3 = R - R_i' = 7.1 - 1.631$$

$$= 5.47 \text{ k}\Omega$$

$$k = \frac{R_C}{R} = \frac{20}{7.1} = 2.816$$

Now $$f = \frac{1}{2\pi RC\sqrt{6+4k}}$$

$\therefore$ $$10\times10^3 = \frac{1}{2\pi\times7.1\times10^3\times C\times\sqrt{6+4\times2.816}}$$

$\therefore$ $$C = \mathbf{539.45\ pF}$$

$$h_{fe} \geq 4k + 23 + \frac{29}{k}$$ refer equation (12) of section 2.5.3

$\therefore$ $$h_{fe} \geq 4\times2.816+23+\frac{29}{2.816}$$

$\therefore$ $$h_{fe} \geq \mathbf{44.562}$$

Wien Bridge Oscillator:

2.6 Wien Bridge Oscillator

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But **Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage.** As total phase shift required is 0° or $2n\pi$ radians, in Wien bridge type no phase shift is necessary through feedback.

Key Point : *Thus the total phase shift around a loop is 0°.*

Let us study the basic version of the Wien bridge oscillator and its analysis.

A basic Wien bridge used in this oscillator and an amplifier stage is shown in the Fig. 2.15.

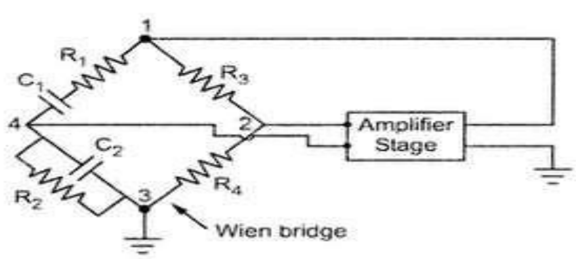


Fig. 2.15 Basic circuit of Wien bridge oscillator

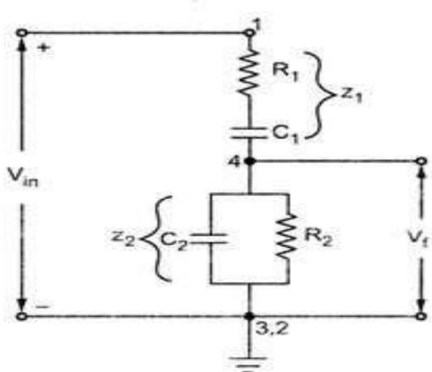


Fig. 2.16 Feedback network of Wien bridge oscillator

The output of the amplifier is applied between the terminals 1 and 3, which is the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own input through the Wien bridge as a feedback network.

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called **frequency sensitive arms**. This is because the components of these two arms decide the frequency of the oscillator. Let us find out the gain of the feedback network. As seen earlier input V_{in} to the feedback network is between is 1 and 3 while output V_f of the feedback network is between 2 and 4. This is shown in the Fig. 2.16. Such a feedback network is called **lead-lag network**. This is because at very low frequencies it acts like a lead while at very high frequencies it acts like lag network.

Now from the Fig. 2.16, as shown,

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}$$

$$Z_2 = R_2 \parallel \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$\therefore$
$$Z_2 = \frac{R_2}{1 + j\omega R_2 C_2} \quad \ldots (1)$$

Replacing $j\omega = s$,

$$Z_1 = \frac{1 + s R_1 C_1}{s C_1}$$

and
$$Z_2 = \frac{R_2}{1 + s R_2 C_2}$$

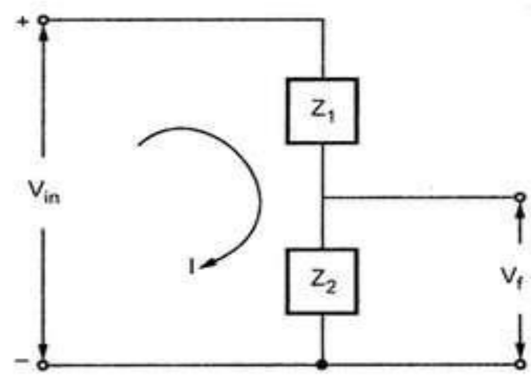


Fig. 2.17 Simplified circuit

$$I = \frac{V_{in}}{Z_1 + Z_2}$$

and
$$V_f = I Z_2$$

$\therefore$
$$V_f = \frac{V_{in} Z_2}{Z_1 + Z_2}$$

$\therefore$
$$\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2} \quad \ldots (2)$$

Substituting the values of $\bar{Z}_1$ and $\bar{Z}_2$,

$$\beta = \frac{\left[\dfrac{R_2}{1+sR_2C_2}\right]}{\left[\dfrac{1+sR_1C_1}{sC_1}\right]+\left[\dfrac{R_2}{1+sR_2C_2}\right]}$$

$$\beta = \frac{s\,C_1\,R_2}{(1+s\,R_1\,C_1)(1+s\,R_2\,C_2)+s\,C_1\,R_2}$$

$$= \frac{s\,C_1\,R_2}{1+s\,(R_1\,C_1+R_2\,C_2)+s^2\,R_1\,R_2\,C_1\,C_2+s\,C_1\,R_2}$$

$$= \frac{s\,C_1\,R_1}{1+s\,(R_1\,C_1+R_2\,C_2+C_1R_2)+s^2\,R_1R_2C_1C_2}$$

Replacing s by $j\omega$, $s^2 = -\omega^2$

$$\therefore \quad \beta = \frac{j\omega C_1\,R_2}{(1-\omega^2\,R_1\,R_2\,C_1\,C_2)+j\omega(R_1\,C_1+R_2\,C_2+C_1R_2)} \qquad \dots (3)$$

Rationalising the expression,

$$\beta = \frac{j\omega C_1R_2\left[(1-\omega^2R_1R_2C_1C_2)-j\omega(R_1C_1+R_2C_2+C_1R_2)\right]}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2(R_1C_1+R_2C_2+C_1R_2)^2}$$

$$\boxed{\beta = \frac{\omega^2\,C_1\,R_2\,(R_1C_1+R_2C_2+C_1R_2)+j\omega C_1R_2(1-\omega^2\,R_1R_2C_1C_2)}{\left(1-\omega^2\,R_1R_2C_1C_2\right)^2+\omega^2\left(R_1C_1+R_2C_2+C_1R_2\right)^2}}$$

$$\dots (4)$$

To have zero phase shift of the feedback network, its imaginary part must be zero.

$$\therefore \quad \omega\,(1-\omega^2\,R_1R_2C_1C_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{R_1\,R_2\,C_1\,C_2} \text{ neglecting zero value.}$$

$$\boxed{\omega = \frac{1}{\sqrt{R_1\,R_2\,C_1\,C_2}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}} \qquad \dots(5)$$

Key Point : *This is the frequency of the oscillator and it shows that the components of the frequency sensitive arms are the deciding factors, for the frequency.*

In practice, $R_1 = R_2 = R$ and $C_1 = C_2 = C$ are selected.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R^2\,C^2}}$$

$$\boxed{f = \frac{1}{2\pi\,RC}} \qquad \dots(6)$$

At $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the gain of the feedback network becomes,

$$\beta = \frac{\omega^2 RC(3RC) + j\omega RC\left(1-\omega^2R^2C^2\right)}{\left(1-\omega^2R^2C^2\right) + \omega^2(3RC)^2}$$

Substituting $f = \frac{1}{2\pi RC}$ i.e. $\omega = \frac{1}{RC}$,

we get the magnitude of the feedback network at the resonating frequency of the oscillator as,

$$\beta = \frac{3}{0 + \frac{1}{R^2C^2} \times (3RC)^2} = \frac{3}{9}$$

$$\therefore \quad \boxed{\beta = \frac{1}{3}} \quad \ldots (7)$$

The positive sign of β indicates that the phase shift by the feedback network is 0°. Now to satisfy the Barkhausen criterion for the sustained oscillations, we can write,

$$|A\beta| \geq 1$$

$$\therefore \quad |A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{3}\right)}$$

$$\therefore \quad \boxed{|A| \geq 3}$$

This is the required gain of the amplifier stage, without any phase shift.

If $R_1 \neq R_2$ and $C_1 \neq C_2$ then

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}}$$

Substituting in the equation (4) we get,

$$\boxed{\beta = \frac{C_1R_2}{(R_1C_1 + R_2C_2 + C_1R_2)}}$$

$$|A\beta| \geq 1$$

$$\therefore \quad \boxed{A \geq \frac{R_1C_1 + R_2C_2 + C_1R_2}{C_1R_2}} \quad \ldots (8)$$

Another important advantage of the Wien bridge oscillator is that by varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be provided.

Let us see the various versions of the Wien bridge oscillator by considering various circuits for the amplifier stage.

2.6.1 Transistorised Wien Bridge Oscillator

In this circuit, **two stage** common emitter transistor amplifier is used. Each stage contributes 180° phase shift hence the total phase shift due to the amplifier stage becomes 360° i.e. 0° which is necessary as per the oscillator conditions.

The practical, transistorised Wien bridge oscillator circuit is shown in the Fig. 2.18.

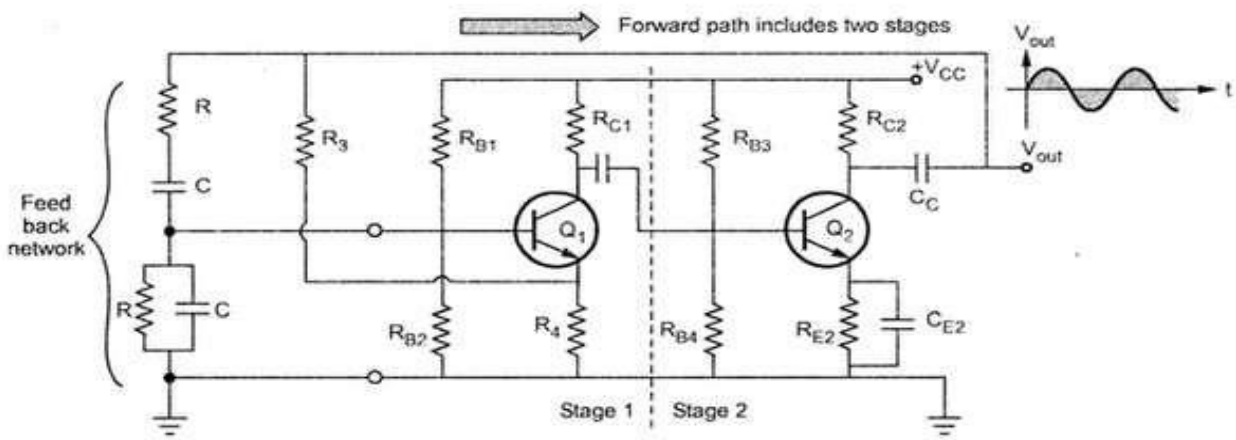


Fig. 2.18 Transistorised Wien bridge oscillator

The bridge consists of R and C in series, R and C in parallel, R_3 and R_4. The feedback is applied from the collector of Q_2 through the coupling capacitor, to the bridge circuit. The resistance R_4 serves the dual purpose of emitter resistance of the transistor Q_1 and also the element of the Wien bridge.

The two stage amplifier provides a gain much more than 3 and it is necessary to reduce it. To reduce the gain, the negative feedback is used without bypassing the resistance R_4. The negative feedback can accomplish the gain stability and can control the output magnitude. The negative feedback also reduces the distortion and therefore output obtained is a pure sinusoidal in nature. The amplitude stability can be improved using a nonlinear resistor for R_4. Due to this, the loop gain depends on the amplitude of the oscillations. Increase in the amplitude of the oscillations, increases the current through nonlinear resistance, which results into an increase in the value of nonlinear resistance R_4. When this value increases, a greater amount of negative feedback is applied. This reduces the loop gain. And hence signal amplitude gets reduced and controlled.

Example : *The frequency sensitive arms of the Wien bridge oscillator uses $C_1 = C_2 = 0.001\,\mu F$ and $R_1 = 10\ k\Omega$ while R_2 is kept variable. The frequency is to be varied from 10 kHz to 50 kHz, by varying R_2. Find the minimum and maximum values of R_2.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

For $f = 10$ kHz,

$$10 \times 10^3 = \frac{1}{2\pi\sqrt{(10 \times 10^3 \times R_2 \times (0.001 \times 10^{-6})^2}}$$

$\therefore$ $R_2 = $ **25.33 kΩ**

For $f = 50$ kHz

$$50 \times 10^3 = \frac{1}{2\pi\sqrt{(10 \times 10^3 \times R_2 \times (0.001 \times 10^{-6})^2}}$$

$\therefore$ $R_2 = $ **1.013 kΩ**

So minimum value of R_2 is 1.013 kΩ while the maximum value of R_2 is 25.33 kΩ.

Oscillators:

2.8 LC Oscillators

The oscillators which use the elements L and C to produce the oscillations are called LC oscillators. The circuit using elements L and C is called **tank circuit** or **oscillatory circuit**, which is an important part of LC oscillators. This circuit is also referred as resonating circuit, or tuned circuit. These oscillators are used for high frequency range from 200 kHz upto few GHz. Due to high frequency range, these oscillators are often used for sources of RF (radio frequency) energy. Let us study the basic action of LC tank circuit first.

2.8.1 Operation of LC Tank Circuit

The LC tank circuit consists of elements L and C connected in parallel as shown in the Fig. 2.24.

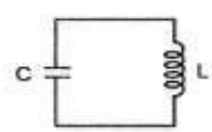


Fig. 2.24 LC tank circuit

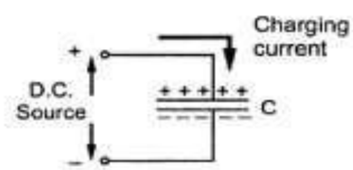


Fig. 2.25 Initial charging

Let capacitor is initially charged from a d.c. source with the polarities as shown in the Fig. 2.25.

When the capacitor gets charged, the energy gets stored in a capacitor called electrostatic energy. When such a charged capacitor is connected across inductor L in a tank circuit, the capacitor starts discharging through L, as shown in the Fig. 2.26. The arrow indicates direction of flow of conventional current. Due to such current flow, the magnetic field gets set up around the inductor L. Thus inductor starts storing the energy. When capacitor is fully discharged, maximum current flows through the circuit. At this instant all the electrostatic energy get stored as a magnetic energy in the inductor L. This is shown in the Fig. 2.27.

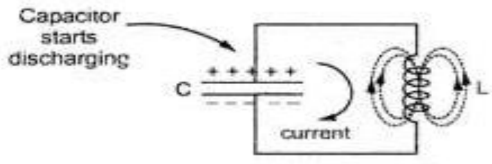


Fig. 2.26

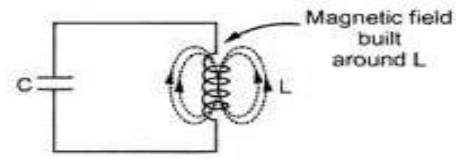


Fig. 2.27

Now the magnetic field around L starts collapsing. As per Lenz's law, this starts charging the capacitor with opposite polarity making lower plate positive and upper plate negative, as shown in the Fig. 2.28.

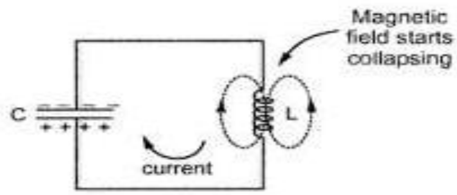


Fig. 2.28

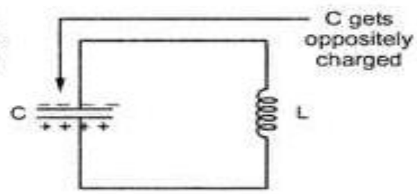


Fig. 2.29

After some time, capacitor gets fully charged with opposite polarities, as compared to its initial polarities. This is shown in the Fig. 2.29. The entire magnetic energy gets converted back to electrostatic energy in capacitor.

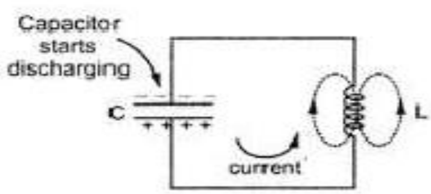


Fig. 2.30

Now capacitor again starts discharging through inductor L. But the direction of current through circuit is now opposite to the direction of current earlier in the circuit. This is shown in the Fig. 2.30. Again electrostatic energy is converted to magnetic energy. When capacitor is fully discharged, the magnetic field starts collapsing, charging the capacitor again in opposite direction.

Key Point : *Thus capacitor charges with alternate polarities and discharges producing alternating current in the tank circuit.*

This is nothing but oscillatory current. But every time when energy is transferred from C to L and L to C, the losses occur due to which amplitude of oscillating current keeps on decreasing everytime when energy transfer takes place. Hence actually we get exponentially decaying oscillations called damped oscillations. These are shown in the Fig. 2.31. Such oscillations stop after sometime.

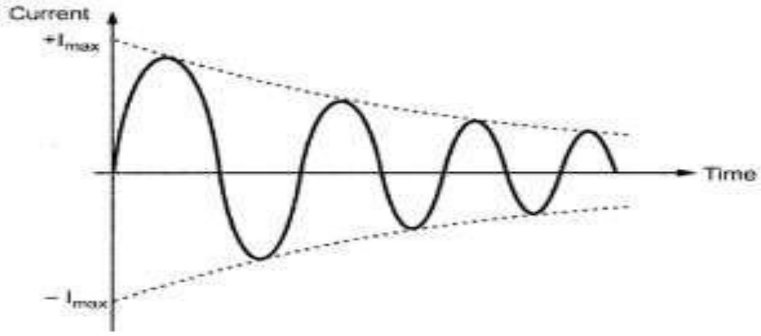


Fig. 2.31 Damped oscillations

Key Point : *In LC oscillator, the transistor amplifier supplies this loss of energy at the proper times.*

The care of proper polarity is taken by the feedback network. Thus LC tank circuit alongwith transistor amplifier can be used to obtain oscillators called LC oscillators. Due to supply of energy which is lost, the oscillations get maintained hence called **sustained oscillations** or **undamped oscillations**.

The frequency of oscillations generated by LC tank circuit depends on the values L and C and is given by,

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \text{Hz}$$

where L is in henries and C is in farads.

2.9 Basic Form of LC Oscillator Circuit

As stated earlier, LC tuned circuit forms the feedback network while an op-amp, FET or bipolar junction transistor can be active device in the amplifier stage. The Fig. 2.32 (a) shows the basic form of LC oscillator circuit with gain of the amplifier as A_v. The amplifier output feeds the network consisting of impedances Z_1, Z_2 and Z_3. Assume an active device with infinite input impedance such as FET or op-amp. Then the basic circuit can be replaced by its linear equivalent circuit as shown in the Fig. 2.32 (b).

Amplifier provides a phase shift of 180°, while the feedback network provides an additional phase shift of 180°, to satisfy the required condition.

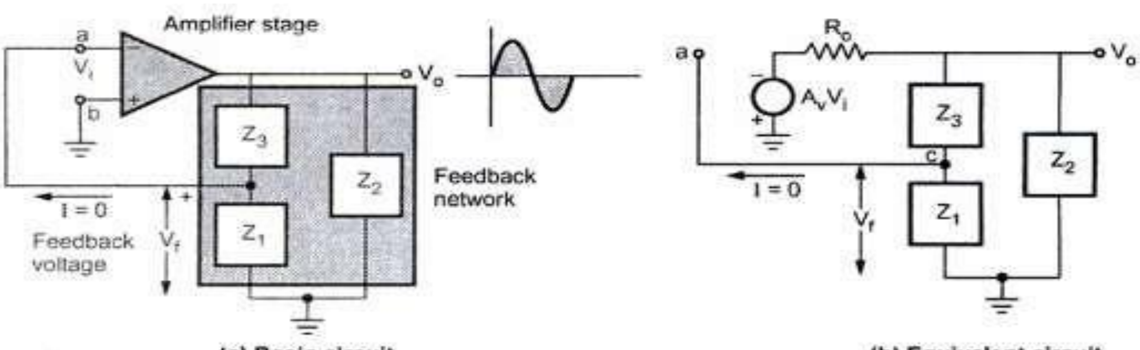


Fig. 2.32

i) Analysis of the amplifier stage

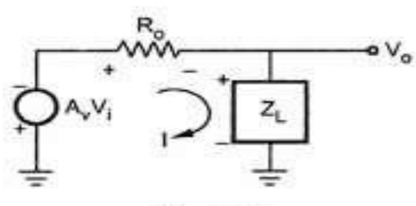


Fig. 2.33

As input impedance of the amplifier is infinite, there is no current flowing towards the input terminals. Let R_o be the output impedance of the amplifier stage.

As I = 0, Z_1, Z_3 appears in series and the combination in parallel with Z_2. The equivalent be Z_L i.e. load impedance. So circuit can be reduced, as shown in the Fig. 2.33.

Key Point : *As $I = 0$, Z_1 and Z_3 are in series and combination is in parallel with Z_2.*

$$\therefore \quad \boxed{I = \frac{-A_V V_i}{R_o + Z_L}} \quad \dots (1)$$

While $$V_o = I Z_L \quad \dots (2)$$

$$\therefore \quad V_o = \frac{-A_V V_i Z_L}{R_o + Z_L}$$

$$\therefore \quad \boxed{\frac{V_o}{V_i} = A = \frac{-A_V Z_L}{R_o + Z_L}} \quad \dots (3)$$

where A is the gain of the amplifier stage.

Key Point: *The negative sign indicates that the amplifier stage introduces 180° phase shift,*

ii) Analysis of the feedback stage

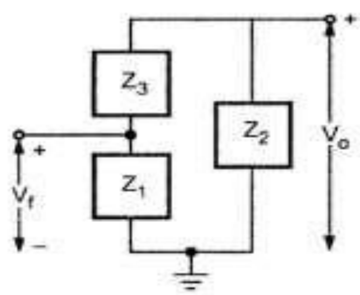


Fig. 2.34

For the feedback factor (β) calculation, consider only the feedback circuit as shown in the Fig. 2.34.

From the voltage division in parallel circuit, we can write,

$$V_f = V_o \left[\frac{Z_1}{Z_1 + Z_3} \right] \quad \dots (4)$$

$$\therefore \frac{V_f}{V_o} = \beta = \frac{Z_1}{Z_1 + Z_3} \quad \dots (5)$$

But as the phase shift of the feedback network is 180°,

$$\boxed{\beta = -\frac{Z_1}{Z_1 + Z_3}} \quad \dots (6)$$

Obtain an expression for $-A\beta$ as basic Barkhausen condition is $-A\beta = 1$. Refer Equation (5) of section 2.3.

$$\therefore \qquad -A\beta = \frac{-A_V Z_1 Z_L}{(R_o + Z_L)\times(Z_1 + Z_3)} \qquad \ldots (7)$$

This is the required loop gain. Now Z_L can be written as $(Z_1 + Z_3) \| Z_2$ i.e.

$$Z_L = \frac{Z_2(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \qquad \ldots (8)$$

$$\therefore \qquad -A\beta = \frac{-A_V Z_1\left[\dfrac{Z_2(Z_1+Z_3)}{Z_1+Z_2+Z_3}\right]}{\left[R_o + \dfrac{Z_2(Z_1+Z_3)}{Z_1+Z_2+Z_3}\right](Z_1+Z_3)}$$

Dividing numerator and denominator by $\frac{(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$,

$$= \frac{-A_V Z_1 Z_2}{\left[\dfrac{R_o(Z_1+Z_2+Z_3)}{(Z_1+Z_3)} + Z_2\right](Z_1+Z_3)}$$

$$\therefore \qquad \boxed{-A\beta = \frac{-A_V Z_1 Z_2}{R_o(Z_1+Z_2+Z_3) + Z_2(Z_1+Z_3)}} \qquad \ldots (9)$$

As Z_1 Z_2 and Z_3 are the pure reactive elements,

$$\boxed{Z_1 = jX_1, \quad Z_2 = jX_2 \quad \text{and } Z_3 = jX_3}$$

where $\qquad X = \omega L \qquad$ for an inductive reactance

and $\qquad X = \frac{-1}{\omega C} \qquad$ for a capacitive reactance.

$$-A\beta = \frac{-A_V (jX_1)(jX_2)}{R_o(jX_1 + jX_2 + jX_3) + jX_2(jX_1 + jX_3)}$$

$$= \frac{A_V X_1 X_2}{-X_2(X_1 + X_3) + jR_o(X_1 + X_2 + X_3)} \qquad \ldots (10)$$

Key Point: *The feedback circuit must introduces 180° phase shift.*

To have 180° phase shift, the imaginary part of the denominator must be zero.

$$\therefore \qquad \boxed{X_1 + X_2 + X_3 = 0} \qquad \ldots (11)$$

Substituting in the equation (10),

$$-A\beta = \frac{-A_V X_1 X_2}{X_2(X_1 + X_3)}$$

But from the equation (11), $X_1 + X_3 = -X_2$

$$\therefore \qquad \boxed{-A\beta = \frac{-A_V X_1}{-X_2} = +A_V\left(\frac{X_1}{X_2}\right)} \qquad \ldots (12)$$

According to the Barkhausen Criterion, $-A\beta$ must be positive and must be greater than or equal to unity. As A_V is positive, the $-A\beta$ will be positive only when X_1 and X_2 will have same sign. **This indicates that X_1 and X_2 must be of same type of reactances either both inductive or capacitive.** While from the equation (11), we can say that $X_3 = -(X_1 + X_2)$ must be inductive if X_1, X_2 are capacitive while X_3 must be capacitive if X_1, X_2 are inductive.

2.9.1 Types of LC Oscillators

Table 2.3 shows the various types of the LC oscillators depending on the design of the reactances X_1, X_2 and X_3.

Oscillator Type	Reactance elements in the tank circuit		
	X_1	X_2	X_3
Hartley Oscillator	L	L	C
Colpitts Oscillator	C	C	L

Table 2.3

2.10 Hartley Oscillator

As seen earlier, a LC oscillator which uses **two inductive reactances** and **one capacitive reactance** in its feedback network is called **Hartley Oscillator**.

2.10.1 Transistorised Hartley Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 2.35.

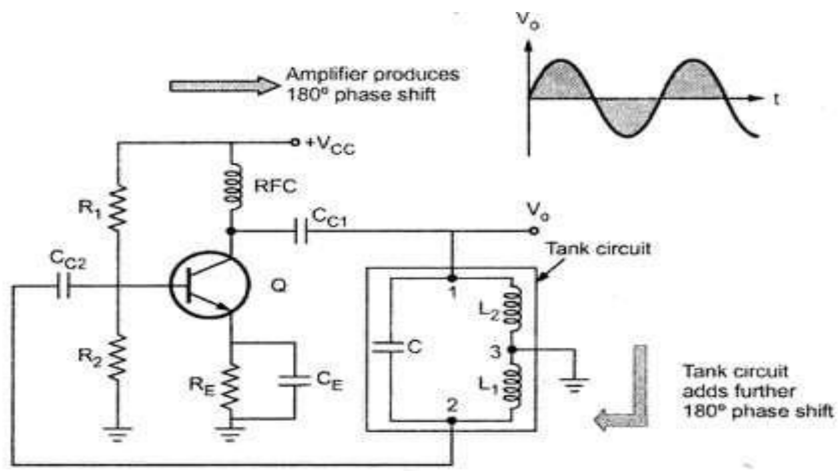


Fig. 2.35 Transistorised Hartley oscillator

The resistances R_1 and R_2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high for high frequencies, hence it can be treated as open circuit. While for d.c. conditions, the reactance is zero hence causes no problem for d.c. capacitors.

Hence due to RFC, the isolation between a.c. and d.c. operation is achieved. R_E is also a biasing circuit resistance and C_E is the emitter bypass capacitor. C_{C1} and C_{C2} are the coupling capacitor.

The common emitter amplifier provides a phase shift of 180°. As emitter is grounded, the base and the collector voltages are out of phase by 180°. As the centre of L_1 and L_2 is grounded, when upper end becomes positive, the lower becomes negative and viceversa. So the LC feedback network gives an additional phase shift of 180°, necessary to satisfy oscillation conditions.

2.10.2 Derivation of Frequency of Oscillations

The output current which is the collector current is $h_{fe}I_b$ where I_b is the base current. Assuming coupling condensers are short, the capacitor C is between base and collector. The inductance L_1 is between base and emitter while the inductance L_2 is between collector and emitter. The equivalent circuit of the feedback network is shown in the Fig. 2.36.

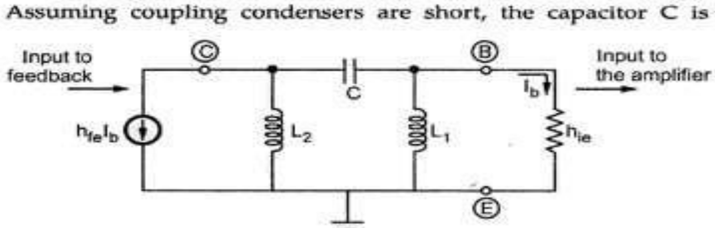


Fig. 2.36 Equivalent circuit

As h_{ie} is the input impedance of the transistor. The output of the feedback is the current I_b which is the input current of the transistor. While input to the feedback network is the output of the transistor which is $I_c = h_{fe}I_b$, converting current source into voltage source we get,

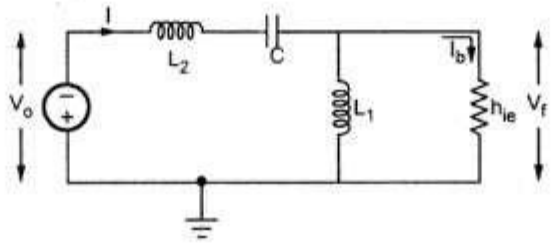


Fig. 2.37 Simplified equivalent circuit

$$V_o = h_{fe}I_b X_{L2} = h_{fe}I_b j\omega L_2 \quad \text{... (1)}$$

Now L_1 and h_{ie} are in parallel, so the total current I drawn from the supply is,

$$I = \frac{-V_o}{[X_{L2}+X_C] + [X_{L1} \| h_{ie}]} \quad \text{... (2)}$$

Key Point : *Negative sign, as current direction shown in opposite to the polarities of* V_o.

Now $\quad X_{L2} + X_C = j\omega L_2 + \frac{1}{j\omega C}$

and $\quad X_{L1} \| h_{ie} = \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}$

Substituting in the equation (2) we get,

$$I = \frac{-h_{fe} I_b j\omega L_2}{\left[j\omega L_2 + \frac{1}{j\omega C}\right] + \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}} \quad \text{... (3)}$$

Replacing $j\omega$ by s,

$$I = \frac{-s h_{fe} I_b L_2}{\left[s L_2 + \frac{1}{sC}\right] + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2}{\frac{[1+s^2 L_2 C]}{sC} + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2 (sC)(s L_1 + h_{ie})}{[1+s^2 L_2 C][s L_1 + h_{ie}] + (sC)(s L_1 h_{ie})}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s L_1 + h_{ie} + s^2 L_2 C h_{ie} + s^2 L_1 C h_{ie}}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s^2 C h_{ie}(L_1 + L_2) + s L_1 + h_{ie}}$$

According to current division in parallel circuit,

$$I_b = I \times \frac{X_{L1}}{XL_1 + h_{ie}}$$

$$= I \times \frac{j\omega L_1}{(j\omega L_1 + h_{ie})}$$

$$\boxed{I_b = I \times \left[\frac{sL_1}{(sL_1 + h_{ie})}\right]} \quad \dots (4)$$

Substituting value of I from equation (3) in equation (4),

$$I_b = \frac{-s^2 h_{fe} I_b L_2 C(sL_1 + h_{ie})}{[s^3(L_1L_2C) + s^2C\,h_{ie}(L_1 + L_2) + sL_1 + h_{ie}]} \times \frac{sL_1}{(sL_1 + h_{ie})}$$

$$= \frac{-s^3 h_{fe} I_b C L_1 L_2}{s^3(L_1L_2C) + s^2Ch_{ie}(L_1 + L_2) + sL_1h_{ie}}$$

$$\therefore \quad 1 = \frac{-s^3 h_{fe} C L_1 L_2}{s^3(L_1L_2C) + s^2Ch_{ie}(L_1 + L_2) + sL_1 + h_{ie}} \quad \dots (5)$$

Substituting $s = j\omega$, $s^2 = -\omega^2$, $s^3 = -j\omega^3$ we get,

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C - \omega^2 C h_{ie}(L_1 + L_2) + j\omega L_1 + h_{ie}}$$

$$= \frac{j\omega^3 h_{ie} C L_1 L_2}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)] + j\omega L_1(1 - \omega^2 L_2 C)} \quad \dots (6)$$

Rationalising the R.H.S of the above equation,

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2 [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2) - j\omega L_1(1 - \omega^2 L_2 C)]}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2}$$

$$= \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C) + j\omega^3 h_{fe} L_1 L_2 C [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_1^2 L_2 C)^2} \quad \dots (7)$$

To satisfy this equation, imaginary part of R. H. S. must be zero.

$$\therefore \quad \boxed{\omega^3 h_{fe} L_1 L_2 C\,[h_{ie} - \omega^2 h_{ie} C (L_1 + L_2)] = 0}$$

$$\therefore \quad \omega^3 h_{fe} h_{ie} L_1 L_2 C\,[1 - \omega^2 C (L_1 + L_2)] = 0$$

$$\therefore \quad 1 - \omega^2 C (L_1 + L_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{C(L_1 + L_2)}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{C(L_1 + L_2)}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}} \quad \dots (8)$$

This is the frequency of the oscillations. At this frequency, the restriction of the value of h_{fe} can be obtained, by equating the magnitudes of the both sides of the equation (7)

$$\therefore \quad 1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C(1-\omega^2 L_2 C)}{0+\omega^2 L_1^2 (1-\omega^2 L_2 C)^2} \text{ at } \omega = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{(1-\omega^2 L_2 C)} \text{ at } \omega = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{\left[1-\frac{L_2 C}{C(L_1+L_2)}\right]} = \frac{h_{fe} L_2}{L_1}$$

$$\therefore \quad \boxed{h_{fe} = \frac{L_1}{L_2}} \quad \text{... (9 a)}$$

This is the value of h_{fe}, required to satisfy the oscillating conditions.

For a mutual inductance of M,

$$\boxed{h_{fe} = \frac{L_1 + M}{L_2 + M}} \quad \text{... (9 b)}$$

Now $L_1 + L_2$ is the equivalent inductance of the two inductances L_1 and L_2, connected in series denoted as

$$\boxed{L_{eq} = L_1 + L_2} \quad \text{... (10)}$$

Hence the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{C L_{eq}}}} \quad \text{... (11)}$$

So if the capacitor C is kept variable, frequency can be varied over a large range as per the requirement.

In practice, L_1 and L_2 may be wound on a single core so that there exists a mutual inductance between them denoted as M.

In such a case, the mutual inductance is considered while determining the equivalent inductance L_{eq}. Hence,

$$\boxed{L_{eq} = L_1 + L_2 + 2M} \quad \text{... (12)}$$

If L_1 and L_2 are assisting each other then sign of 2M is positive while if L_1 and L_2 are in series opposition then sign of 2M is negative.

The expression for the frequency of the oscillations remain same as given by (13).

A practical circuit where the mutual inductance exists between L_1 and L_2, of transistorised Hartley oscillator is shown in the Fig. 2.38.

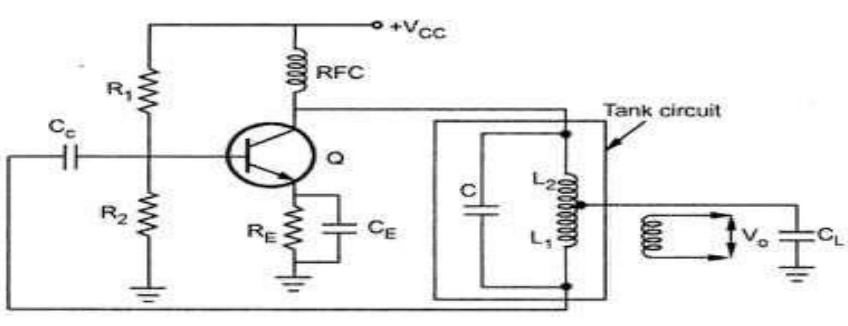


Fig. 2.38 Another form of transistorised Hartley oscillator

Example 2.6 : *In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied.*

Solution : The frequency is given by

$$f = \frac{1}{2\pi\sqrt{C\,(L_{eq})}}$$

Where $L_{eq} = L_1 + L_2 = 2\times10^{-3} + 20\times10^{-6}$

$= 0.00202$ kHz

For $f = f_{max} = 2050$ kHz

$$2050\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}}$$

$\therefore$ $C =$ **2.98 pF**

For $f = f_{min} = 950$ kHz

$$950\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}} \quad C = \mathbf{13.89\ pF}$$

Hence C must be varied from 2.98 pF to 13.89 pF, to get the required frequency variation.

2.11 Colpitts Oscillator

An LC oscillator which uses two capacitive reactances and one inductive reactance in the feedback network i.e. tank circuit, is called **Colpitts oscillator**.

2.11.1 Transistorised Colpitts Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 2.41.

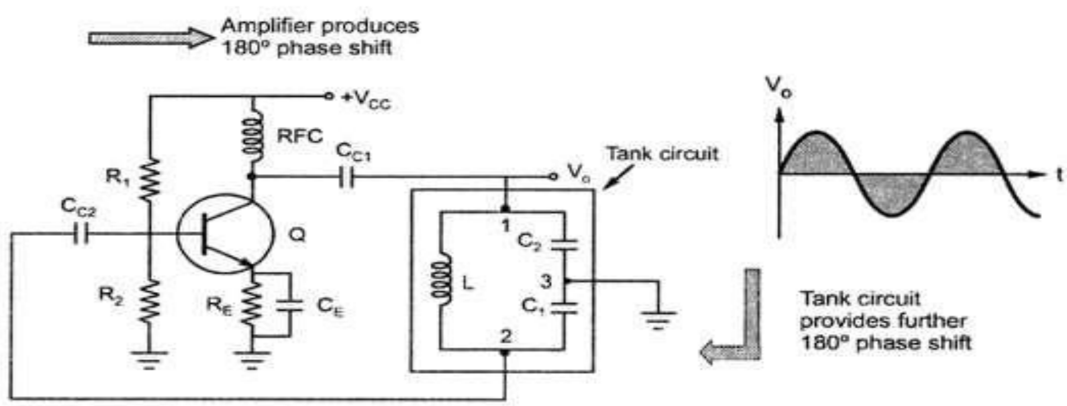


Fig. 2.41 Transistorised Colpitts oscillator

The basic circuit is same as transistorised Hartley oscillator, except the tank circuit. The common emitter amplifier causes a phase shift of 180°, while the tank circuit adds further 180° phase shift, to satisfy the oscillating conditions.

2.11.2 Derivation of frequency of Oscillations

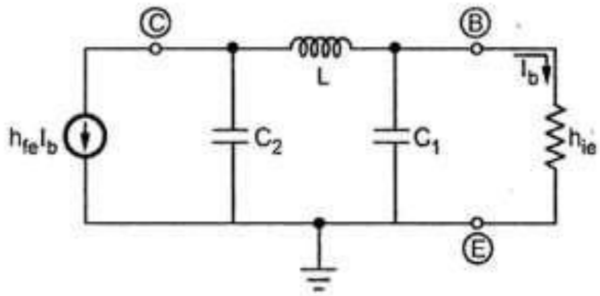


Fig. 2.42 Equivalent circuit

As seen earlier, the output current I_c which is h_{fe} I_b acts as input to the feedback network. While the base current I_b acts as the output current of the tank circuit, flowing through the input impedance of the amplifier h_{ie}. The equivalent circuit of the tank circuit is shown in the Fig. 2.42.

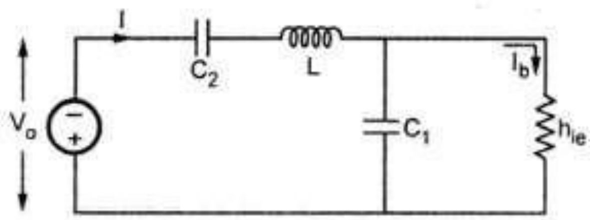


Fig. 2.43 Simplified equivalent circuit

Converting the current source into the voltage source. We get the equivalent circuit as shown in the Fig. 2.43.

$$V_o = h_{fe} I_b X_{C2} = h_{fe} I_b \frac{1}{j\omega C_2} \quad \text{... (1)}$$

The total current I, drawn from the supply is,

$$I = \frac{-V_o}{[X_{C2} + X_L] + [X_{C1} \,||\, h_{ie}]} \quad \text{... (2)}$$

Key Point : *The negative sign is because the current direction is assumed in the opposite direction to that, would be due to the polarities of V_o.*

Now $$X_{C2} + X_L = \frac{1}{j\omega C_2} + j\omega L$$

and $$X_{C1} \,||\, h_{ie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\left[\frac{1}{j\omega C_1} + h_{ie}\right]}$$

Substituting in the equation (2),

$$\therefore \quad I = \frac{-h_{fe} I_b \left(\frac{1}{j\omega C_2}\right)}{\left[\frac{1}{j\omega C_2} + j\omega L\right] + \left[\frac{\frac{h_{ie}}{j\omega C_1}}{h_{ie} + \frac{1}{j\omega C_1}}\right]} \quad \ldots (3)$$

Replacing jω by s,

$$\therefore \quad I = \frac{-h_{fe} I_b \left(\frac{1}{s C_2}\right)}{\left[\frac{1}{s C_2} + s L\right] + \left[\frac{\frac{h_{ie}}{s C_1}}{h_{ie} + \frac{1}{s C_1}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{s C_2}\right)}{\frac{(1 + s^2 L C_2)}{s C_2} + \left[\frac{h_{ie}}{1 + s C_1 h_{ie}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{s C_2}\right)(s C_2)(1 + s C_1 h_{ie})}{(1 + s^2 L C_2)(1 + s C_1 h_{ie}) + s C_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s C_1 h_{ie} + 1 + s C_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1} \quad \ldots (4)$$

According to the current division in the parallel circuit,

$$I_b = I \times \frac{X_{C1}}{(X_{C1} + h_{ie})} = \frac{I \times \frac{1}{j\omega C_1}}{\left(h_{ie} + \frac{1}{j\omega C_1}\right)}$$

$$\therefore \quad \boxed{I_b = \frac{I}{(1 + s h_{ie} C_1)}} \quad \ldots (5)$$

Substituting value of I from the equation (4) in (5) we get,

$$\therefore \quad I_b = \frac{-h_{fe} I_b (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1} \times \frac{1}{(1 + s C_1 h_{ie})}$$

$$= \frac{-h_{fe} I_b}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie}(C_1 + C_2) + 1}$$

$$\therefore \quad \boxed{1 = \frac{-h_{fe}}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie}(C_1 + C_2) + 1}} \quad \ldots (6)$$

Replacing s by $j\omega$, and s^2 by $-\omega^2$ and s^3 by $-j\omega^3$

$$\therefore \quad 1 = \frac{-h_{fe}}{-j\omega^3 L C_1 C_2 h_{ie} - \omega^2 L C_2 + j\omega h_{ie}(C_1 + C_2) + 1}$$

$$= \frac{-h_{fe}}{(1 - \omega^2 L C_2) + j\omega h_{ie}[C_1 + C_2 - \omega^2 L C_1 C_2]} \quad \ldots (7)$$

There is no need to rationalise this as there are no j terms in the numerator, as in the equation (6) of section 2.10.2 a.

It can be seen that, to satisfy the equation, the imaginary part of the denominator of the right hand side must be zero.

$$\therefore \quad \boxed{\omega h_{ie}[C_1 + C_2 - \omega^2 L C_1 C_2] = 0}$$

$$\therefore \quad C_1 + C_2 - \omega^2 L C_1 C_2 = 0 \quad \ldots \text{Neglecting zero value of } \omega$$

$$\therefore \quad \omega^2 = \frac{(C_1 + C_2)}{L C_1 C_2} = \frac{1}{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}}}$$

Now $\frac{C_1 C_2}{C_1 + C_2}$ is nothing but the equivalent of two capacitors C_1 and C_2 in series.

$$\therefore \quad C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L C_{eq}}}} \quad \ldots (8)$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L C_{eq}}}} \quad \ldots (9)$$

This is the frequency of the oscillations in the Colpitts oscillator.

Substituting this frequency in the equation (7) of section 2.11.2 and equating the magnitudes of the both sides, the restriction on the value of h_{fe} can be obtained as,

$$\therefore \qquad \boxed{h_{fe} = \frac{C_2}{C_1}} \qquad \dots (10)$$

Key Point : *Thus the behaviour of Colpitts oscillator is similar to the Hartley oscillator, as basic LC oscillator circuit is same, except the tank circuit.*

Let us see the FET and op-amp versions of the Colpitts oscillator.

Example 2.7 : *Find the frequency of the oscillations of a transistorised Colpitts oscillator having $C_1 = 150$ pF, $C_2 = 1.5$ nF and $L = 50$ μH*

Solution :

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{150\times10^{-12}\times1.5\times10^{-9}}{[150\times10^{-12}+1.5\times10^{-9}]}$$

$$= 136.363 \text{ pF}$$

Now

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{50\times10^{-6}\times136.363\times10^{-12}}}$$

$$= \mathbf{1.927\ MHz}$$

2.16 Frequency Stability of Oscillator

For an oscillator, the frequency of the oscillations must remain constant. The analysis of the dependence of the oscillating frequency on the various factors like stray capacitance, temperature etc. is called as the **frequency stability analysis**.

The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long a time as possible is called **frequency stability** of an oscillator.

In a transistorised Colpitts oscillator or Hartley oscillator, the base-collector junction is reverse biased and there exists an internal capacitance which is dominant at high frequencies. This capacitance affects the value of capacitance in the tank circuit and hence the oscillating frequency.

Similarly the transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. Hence practically the circuits cannot provide stable frequency.

Factors affecting the frequency stability :

In general following are the factors which affect the frequency stability of an oscillator :

1. Due to the changes in temperature, the values of the components of tank circuit get affected. So changes in the values of inductors and capacitors due to the changes in the temperature is the main cause due to which frequency does not remain stable.
2. Due to the changes in temperature, the parameters of the active device used like BJT, FET get affected which inturn affect the frequency.
3. The variation in the power supply is another factor affecting the frequency.

4. The changes in the atmospheric conditions, aging and unstable transistor parameters affect the frequency.
5. The changes in the load connected, affect the effective resistance of the tank circuit.
6. The capacitive effect in transistor and stray capacitances, affect the capacitance of the tank circuit and hence the frequency.

The variation of frequency with temperature is given by the factor denoted as S.

$$S_{\omega,T} = \frac{\Delta\omega / \omega_r}{\Delta T / T_r} \text{ parts per million per °C} \quad \ldots (1)$$

where ω_r = Desired frequency.

T_r = Operating temperature.

$\Delta\omega$ = Change in frequency.

ΔT = Change in temperature.

The frequency stability is defined as,

$$S_\omega = \frac{d\theta}{d\omega} \quad \ldots (2)$$

where $d\theta$ = Phase shift introduced for a small frequency change in desired frequency f_r.

Key Point : *Larger the value of $d\theta/d\omega$, more stable is the oscillator.*

The **frequency stability can be improved** by the following modifications :

1. Enclosing the circuit in a constant temperature chamber.
2. Maintaining constant voltage by using the zener diodes.
3. The load effect is reduced by coupling the oscillator to the load loosely or with the help of a circuit having high input impedance and low output impedance.

2.17 Crystal Oscillators

The crystals are either naturally occurring or synthetically manufactured, exhibiting the **piezoelectric effect**. The piezoelectric effect means under the influence of the mechanical pressure, the voltage gets generated across the opposite faces of the crystal. If the mechanical force is applied in such a way to force the crystal to vibrate, the a.c. voltage gets generated across it. Conversely, if the crystal is subjected to a.c. voltage, it vibrates causing mechanical distortion in the crystal shape. Every crystal has its own resonating frequency depending on its cut. So under the influence of the mechanical vibrations, the crystal generates an electrical signal of very constant frequency. The crystal has a greater stability in holding the constant frequency. A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as its resonant tank circuit. The crystal oscillators are preferred when greater frequency stability is required. Hence the crystals are used in watches, communication transmitters and receivers etc.

The main substances exhibiting the piezoelectric effect are quartz, Rochelle salt and tourmaline. Rochelle salts have the greatest piezoelectric activity. For a given a.c. voltage, they vibrate more than quartz or tourmaline. Hence these are preferred in making microphones associated with portable tape recorders, headsets, loudspeakers etc. Rochelle salt is mechanically weakest of the three and break very easily. Tourmaline shows least piezoelectric effect but mechanically strongest. The tourmaline is most expensive and hence its use is rare in practice Quartz is a compromise between the piezoelectric activity of Rochelle salts and the strength of the tourmaline. **Quartz** is inexpensive and easily available in nature and hence very commonly used in the crystal oscillators.

Key Point : *Quartz is widely used for RF oscillators and the filters.*

2.17.1 Constructional Details

The natural shape of a quartz crystal is a hexagonal prism. But for its practical use, it is cut to the rectangular slab. This slab is then mounted between the two metal plates.

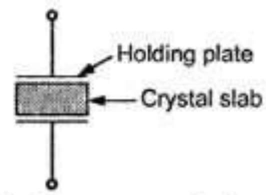


Fig. 2.55 Symbolic representation of a crystal

The symbolic representation of such a practical crystal is shown in the Fig. 2.55. The metal plates are called holding plates, as they hold the crystal slab in between them.

2.17.2 A.C. Equivalent Circuit

When the crystal is not vibrating, it is equivalent to a capacitance due to the mechanical mounting of the crystal. Such a capacitance existing due to the two metal plates separated by a dielectric like crystal slab, is called **mounting capacitance** denoted as C_M or C′.

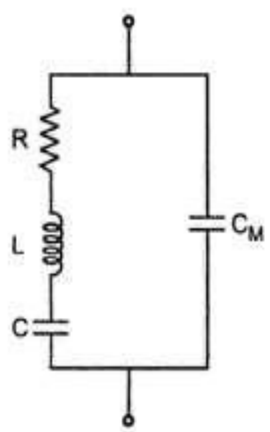


Fig. 2.56 A.C. equivalent circuit of a crystal

When it is vibrating, there are internal frictional losses which are denoted by a resistance R. While the mass of the crystal, which is indication of its inertia is represented by an inductance L. In vibrating condition, it is having some stiffness, which is represented by a capacitor C. The mounting capacitance is a shunt capacitance. And hence the overall equivalent circuit of a crystal can be shown as in the Fig. 2.56.

RLC forms a resonating circuit. The expression for the resonating frequency f_r is,

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}} \qquad ...(1)$$

Where

$$Q = \text{Quality factor of crystal}$$

$$\therefore \quad Q = \frac{\omega L}{R} \quad ...(2)$$

The Q factor of the crystal is very high, typically 20,000. Value of Q upto 10^6 also can be achieved. Hence $\sqrt{\frac{Q^2}{1+Q^2}}$ factor approaches to unity and we get the resonating frequency as,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad ...(3)$$

The crystal frequency is infact inversely proportional to the thickness of the crystal.

$$f \propto \frac{1}{t} \quad \text{where } t = \text{Thickness}$$

So to have very high frequencies, thickness of the crystal should be very small. But it makes the crystal mechanically weak and hence it may get damaged, under the vibrations. Hence practically crystal oscillators are used upto 200 or 300 kHz only.

The crystal has two resonating frequencies, series resonant frequency and parallel resonant frequency.

2.17.3 Series and Parallel Resonance

One resonant condition occurs when the reactances of series RLC leg are equal i.e. $X_L = X_C$. This is nothing but the series resonance. The impedance offered by this branch, under resonant condition is minimum which is resistance R. The series resonance frequency is same as the resonating frequency given by the equation (3).

$$f_s = \frac{1}{2\pi\sqrt{LC}} \quad ... (4)$$

The other resonant condition occurs when the reactances of series resonant leg equals the reactance of the mounting capacitor C_M. This is parallel resonance or antiresonance condition.

Under this condition the impedance offered by the crystal to the external circuit is maximum.

Under parallel resonance, the equivalent capacitance is,

$$C_{eq} = \frac{C_M C}{C_M + C} \quad ... (5)$$

Hence the parallel resonating frequency is given by,

$$\boxed{f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}} \quad \text{... (6)}$$

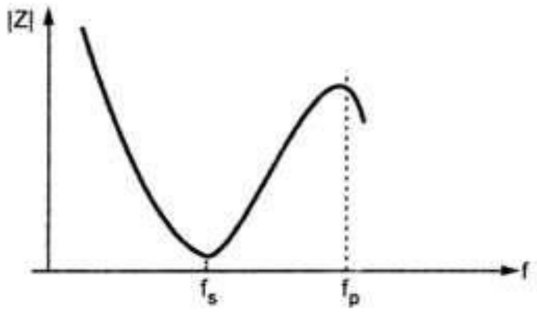


Fig. 2.57 (a) Crystal impedance versus frequency

When the crystal capacitance C is much smaller than C_M, then the Fig. 2.57 shows the behaviour of crystal impedance versus frequency.

Generally values of f_s and f_p are very close to each other and practically it can be said that there exists only one resonating frequency for a crystal.

The higher value of Q is the main advantage of crystal. Due to high Q of a resonant circuit, it provides very good frequency stability.

If we neglect the resistance R, the impedance of the crystal is a reactance jX which depends on the frequency as,

$$jX = -\frac{j}{\omega C_M} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

where ω_s = Series resonant frequency.

ω_p = Parallel resonant frequency.

The sketch of reactance against frequency is shown in the Fig. 2.57 (b).

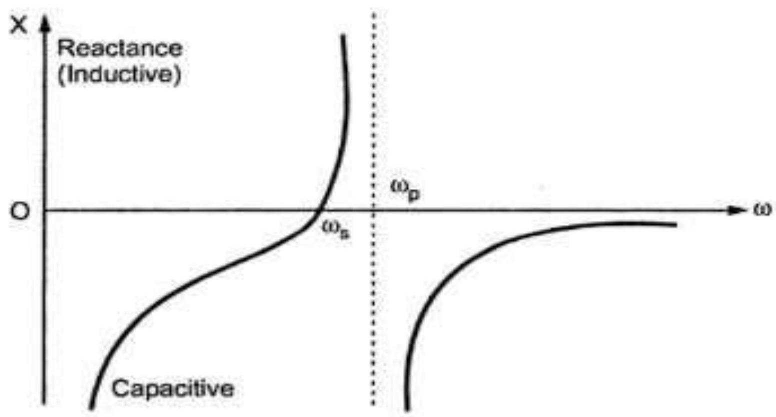


Fig. 2.57 (b) The reactance versus frequency

The oscillating frequency lies between ω_s and ω_p.

2.17.4 Crystal Stability

The frequency of the crystal tends to change slightly with time due to temperature, aging etc.

i) Temperature stability : It is defined as the change in the frequency per degree change in the temperature. This is Hz/MHz/°C. For 1 °C change in the temperature, the frequency changes by 10 to 12 Hz in MHz. This is negligibly small. So for all practical purposes it is treated to be constant. But if this much change is also not acceptable then the crystal is kept in box where temperature is maintained constant, called constant temperature oven or constant temperature box.

ii) Long term stability : It is basically due to aging of the crystal material. Aging rates are 2×10^{-8} per year, for a quartz crystal. This is also negligibly small.

iii) Short term stability : In a quartz crystal, the frequency drift with time is, typically less than 1 part in 10^6 i.e. 0.0001 % per day. This is also very small.

Key Point : *Overall crystal has good frequency stability. Hence it is used in computers, counters, basic timing devices in electronic wrist watches, etc.*

2.17.5 Pierce Crystal Oscillator

The **Colpitts** oscillator can be modified by using the crystal to behave as an inductor. The circuit is called Pierce crystal oscillator. The crystal behaves as an inductor for a frequency slightly higher than the series resonance frequency f_s. The two capacitors C_1, C_2 required in the tank circuit along with an inductor are used, as they are used in **Colpitts** oscillator circuit. As only inductor gets replaced by the crystal, which behaves as an inductor, the basic working principle of Pierce crystal oscillator is same as that of **Colpitts** oscillator. The practical transistorised pierce crystal oscillator circuit is shown in the Fig. 2.58.

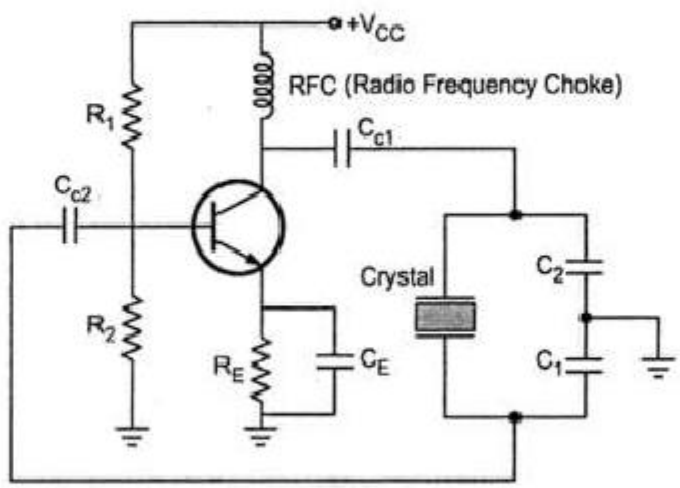


Fig. 2.58 Pierce crystal oscillator

The resistances R_1, R_2, R_E provide d.c. bias while the capacitor C_E is emitter bypass capacitor. RFC (Radio Frequency Choke) provides isolation between a.c. and d.c. operation. C_{c1} and C_{c2} are coupling capacitors.

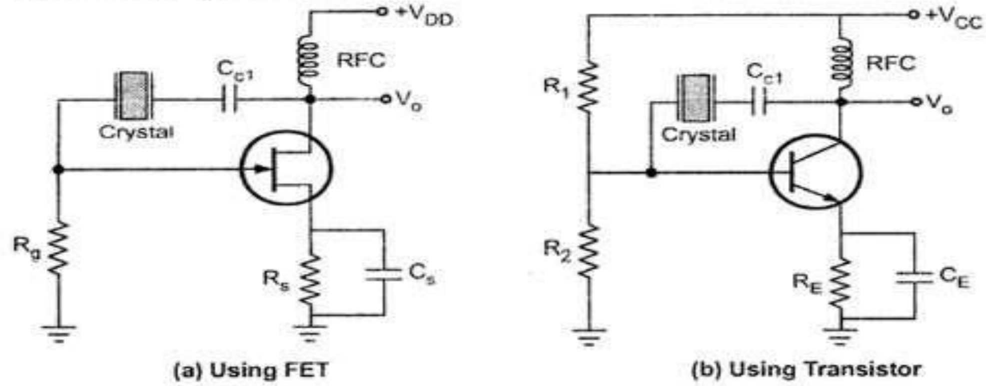


Fig. 2.59 Pierce crystal oscillator

The resulting circuit frequency is set by the series resonant frequency of the crystal, Change in the supply voltages, temperature, transistor parameters have no effect on the circuit operating conditions and hence good frequency stability is obtained.

The oscillator circuit can be modified by using the internal capacitors of the transistor used instead of C_1 and C_2. The separate capacitors C_1, C_2 are not required in such circuit. Such circuits using FET and transistor are shown in the Fig. 2.59 (a) and (b).

2.17.6 Miller Crystal Oscillator

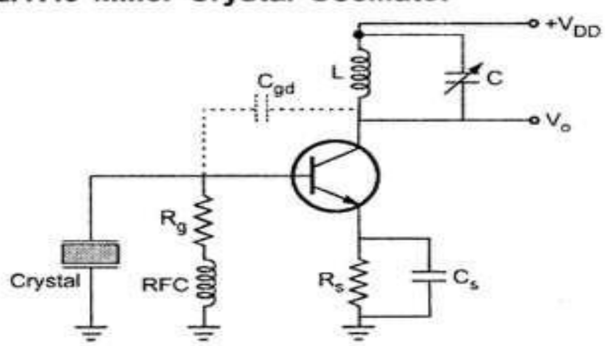


Fig. 2.60 Miller crystal oscillator

Similar to the modifications in Colpitts oscillator, the Hartley oscillator circuit can be modified, to get Miller crystal oscillator. In Hartley oscillator circuit, two inductors and one capacitor is required in the tank circuit. One inductor is replaced by the crystal which acts as an inductor for the frequencies slightly greater than the series resonant frequency. The transistorised Miller crystal oscillator circuit is shown in the Fig. 2.60.

The tuned circuit of L_1 and C is offtuned to behave as an inductor i.e. L_1. The crystal behaves as other inductance L_2 between base and ground. The internal capacitance of the transistor acts as a capacitor required to fulfill the elements of the tank circuit. The crystal decides the operating frequency of the oscillator.

Example 2.8 : *A crystal L = 0.4 H, C = 0.085 pF and C_M = 1 pF with R = 5 kΩ. Find*

i) Series resonant frequency

ii) Parallel resonant frequency

iii) By what percent does the parallel resonant frequency exceed the series resonant frequency ?

iv) Find the Q factor of the crystal.

Solution : i)

$$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.4\times 0.085\times 10^{-12}}}$$

$$= \mathbf{0.856\ MHz}$$

ii)

$$C_{eq} = \frac{CC_M}{C+C_M} = \frac{0.085\times 1}{0.085+1} = 0.078 \text{ pF}$$

∴

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.4\times 0.078\times 10^{-12}}}$$

$$= \mathbf{0.899\ MHz}$$

iii)

$$\%\ \text{increase} = \frac{0.899-0.856}{0.856}\times 100 = \mathbf{5.023\%}$$

iv)

$$Q = \frac{\omega_s L}{R} = \frac{2\pi f_s L}{R} = \frac{2\pi\times 0.856\times 10^6\times 0.4}{5\times 10^3}$$

$$= \mathbf{430.272}$$

Example 2.9 : *A crystal has L = 2 H, C = 0.01 pF and R = 2 kΩ. Its mounting capacitance is 2 pF. Calculate it series and parallel resonating frequency.*

Solution : $C_M = 2$ pF

Now

$$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{\sqrt{2\times 0.01\times 10^{-12}}}$$

$$= \mathbf{1.125\ MHz}$$

$$C_{eq} = \frac{C_M C}{C_M + C} = \frac{2\times 10^{-12}\times 0.01\times 10^{-12}}{2\times 10^{-12}+0.01\times 10^{-12}} = 9.95\times 10^{-15}\text{ F}$$

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{\sqrt{2\times 9.95\times 10^{-15}}}$$

$$= \mathbf{1.128\ MHz}$$

So f_s and f_p values are almost same.

2.18 Amplitude Stabilization

The oscillator output amplitude if not stabilized, attains the extreme levels of saturation i.e. $\pm V_{sat}$. But this can cause the distortion in the output waveform. Hence it is necessary to minimize the distortion and reduce the output amplitude within the acceptable range. The circuit used in the oscillator for this purpose is called **oscillator amplitude stabilization circuit**. It makes the oscillations damped and ensures that are not sustained if amplitude increases beyond a particular value.

The amplitude stabilization circuit used for the phase shift oscillator is shown in the Fig. 2.61(a).

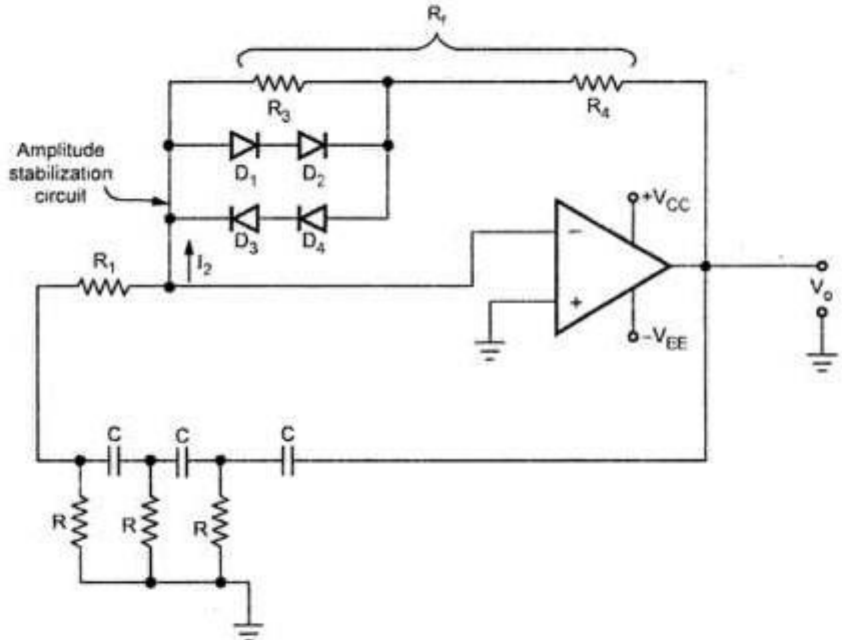


Fig. 2.61 (a) Amplitude stabilization of phase shift oscillator

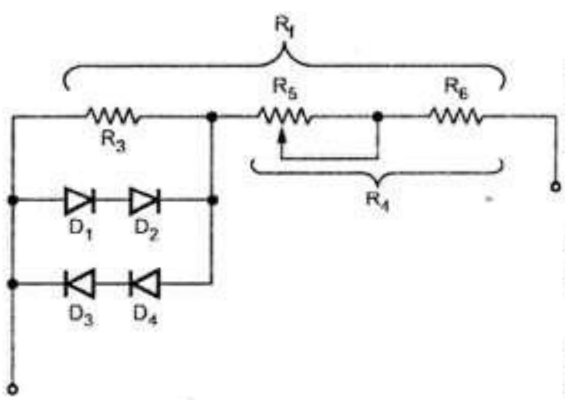


Fig. 2.61 (b) Use of adjustable resistors

When output amplitude exceeds some acceptable level, it makes the diodes D_3 and D_4 forward biased. Thus resistance R_3 gets shorted. Thus the gain of the inverting amplifier becomes $A_{CL} = -\frac{R_4}{R_1}$. The R_4 is so designed that this gain is not enough to sustain the oscillations of high amplitude.

The resistance R_4 can be made up of one fixed resistance R_6 and other variable resistance R_5 for variable adjustment of R_4, to overcome distortion. This is shown in the Fig. 2.61 (b).

Example 2.10 : *The frequency sensitive arms of the Wien bridge oscillator uses $C_1 = C_2 = 0.001\ \mu F$ and $R_1 = 10\ k\Omega$ while R_2 is kept variable. The frequency is to be varied from 20 kHz to 70 kHz by varying R_2. Find the minimum and maximum values of R_2.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

For $f = 20$ kHz,

$$20 \times 10^3 = \frac{1}{2\pi\sqrt{10\times10^3 \times R_2 \times (0.001\times10^{-6})^2}}$$

$\therefore$ $R_2 = \mathbf{6.33\ k\Omega}$

For $f = 70$ kHz

$$70 \times 10^3 = \frac{1}{2\pi\sqrt{10\times10^3 \times R_2 \times (0.001\times10^{-6})^2}}$$

$\therefore$ $R_2 = \mathbf{0.516\ k\Omega}$

So minimum value of R_2 is 0.516 kΩ while the maximum value of R_2 is 6.33 kΩ

Example 2.11 : *For phase shift oscillator, the feedback network uses R = 6 kΩ and C = 1500 pF. The transistorised amplifier used, has a collector resistance of 18 kΩ. Calculate the frequency of oscillations and minimum value of h_{fe} of the transistor.*

Solution : R = 6 kΩ , C = 1500 pF, R_C = 18 kΩ

Now $K = \frac{R_C}{R} = \frac{18}{6} = 3$

$$\therefore \quad f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$$= \frac{1}{2\pi\times6\times10^3\times1500\times10^{-12}\sqrt{6+12}}$$

$$= \mathbf{4.168\ kHz}$$

$$(h_{fe})_{min} = 4K + 23 + \frac{29}{K}$$

$$= 4 \times 3 + 23 + \frac{29}{3}$$

$$= \mathbf{44.67}$$

Example 2.15 : *In a Hartley Oscillator, L_1 = 15 mH and C = 50 pF. Calculate L_2 for a frequency of 168 kHz. The mutual inductance between L_1 and L_2 is 5 μH. Also find the required gain of the transistor to be used for the oscillations.*

Solution : For a Hartley oscillator,

$$f = \frac{1}{2\pi\sqrt{L_{eq} C}} \quad \text{where } L_{eq} = L_1 + L_2 + 2M$$

$$\therefore \quad 168\times10^3 = \frac{1}{2\pi\sqrt{L_{eq}\times50\times10^{-12}}}$$

$\therefore$ $L_{eq} = 17.95$ mH

$\therefore$ $17.95\times10^{-3} = 15\times10^{-3} + L_2 + 5\times10^{-6}$

$\therefore$ $L_2 = \mathbf{2.945\ mH}$

Now $h_{fe} = \frac{L_1 + M}{L_2 + M}$

$$= \frac{15\times10^{-3}+5\times10^{-6}}{2.945\times10^{-3}+5\times10^{-6}}$$

$$= \mathbf{5.08}$$

Example 2.14 : *A Hartley oscillator circuit has C = 500 pF, L_1 = 20 mH and L_2 = 5 mH. Find the frequency of oscillations.*

Solution : For a Hartley oscillator the frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L_{eq}\,C}} \qquad \text{where } L_{eq} = L_1 + L_2$$

$$\therefore \quad L_{eq} = 20 + 5$$

$$= 25 \text{ mH}$$

$$\therefore \quad f = \frac{2}{2\pi\sqrt{25\times10^{-3}\times500\times10^{-12}}}$$

$$= \mathbf{45.01\ kHz}$$

Example 2.24 : *In Colpitts oscillator using FET, the frequency of oscillations is observed to be 2.5 MHz. Oscillator uses : L = 10 μH, C_1 = 0.02 μF.*

Find : i) Value of C_2 ii) If L is doubled, the new value of frequency of oscillations.

Solution : f = 2.5 MHz, L = 10 μH, C_1 = 0.02 μF

For Colpitts oscillator, the frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}$$

$$\therefore \quad 2.5\times10^{6} = \frac{1}{2\pi\sqrt{10\times10^{-6}\times C_{eq}}}$$

$$\therefore \quad C_{eq} = 405.284 \text{ pF}$$

i) But

$$C_{eq} = \frac{C_1\,C_2}{C_1 + C_2}$$

$$\therefore \quad 405.284\times10^{-12} = \frac{0.02\times10^{-6}\,C_2}{0.02\times10^{-6} + C_2}$$

$$\therefore \quad 0.02\times10^{-6} + C_2 = 49.348\,C_2$$

$$\therefore \quad C_2 = \mathbf{0.4136\ nF}$$

ii)

$$L = 2\times10 = 20\ \mu H$$

and

$$C_{eq} = 405.284 \text{ pF}$$

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{20\times10^{-6}\times405.284\times10^{-12}}}$$

$$= \mathbf{1.7677\ MHz}$$

Example 2.28 : *A quartz crystal has $L = 3$ H, $C_S = 0.05$ pF, $R = 2000\ \Omega$ and $C_M = 10$ pF. Calculate the series and parallel resonant frequencies f_s and f_p of the crystal.*

Solution : $L = 3$ H, $C_s = C = 0.05$ pF is series capacitor, $R = 2000\ \Omega$

$$C_M = \text{mounting capacitor} = 10 \text{ pF}$$

i)

$$f_s = \text{Series resonant frequency} = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{3\times0.05\times10^{-12}}} = \textbf{410.9362 kHz}$$

ii)

$$C_{eq} = \frac{C_M C}{C_M + C} = \frac{10\times10^{-12}\times0.05\times10^{-12}}{10\times10^{-12}+0.05\times10^{-12}}$$

$$= 4.9751 \times 10^{-14} \text{ F}$$

$$\therefore \quad f_p = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{3\times4.975\times10^{-14}}}$$

$$= \textbf{411.9623 kHz}$$

Example 2.29 : *In a Colpitt's oscillator $C_1 = 0.001\ \mu F$, $C_2 = 0.01\ \mu F$ and $L = 10\ \mu H$. Find the frequency of oscillation, feedback factor and the voltage gain.* **(AU : Dec.-2004)**

Solution : $C_1 = 0.001\ \mu F$, $C_2 = 0.01\ \mu F$, $L = 10\ \mu H$

$$\therefore \quad C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.001\times10^{-6}\times0.01\times10^{-6}}{0.001\times10^{-6}+0.01\times10^{-6}} = 9.09 \times 10^{-10} \text{ F}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{10\times10^{-6}\times9.09\times10^{-10}}}$$

$$= \textbf{1.6692 MHz}$$

$$A_V = \text{Voltage gain} = \frac{C_2}{C_1} = \frac{0.01\times10^{-6}}{0.001\times10^{-6}} = \textbf{10}$$

For oscillations, $A_V\,\beta = 1$ where β = feedback factor

$$\therefore \quad \beta = \frac{1}{A_V} = \frac{1}{10} = \textbf{0.1}$$

Example 2.35 : *If $L_1 = 1$ mH, $L_2 = 2$ mH and $C = 0.1$ nF, what is the frequency of oscillation of the Hartley oscillator ?*

Solution : For Hartley oscillator,

$$f = \frac{1}{2\pi\sqrt{C(L_1+L_2)}} = \frac{1}{2\pi\sqrt{0.1\times10^{-9}(1\times10^{-3}+2\times10^{-3})}} = \textbf{290.575 kHz}$$

➡ **Example 2.36 :** *If C_1 and C_2 are 200 pF and 50 pF respectively. Calculate the value of inductance for producing oscillations at 1 MHz in the Colpitt's oscillator circuit.*

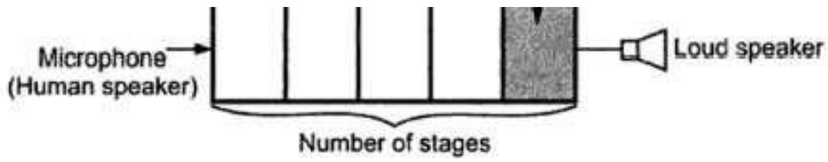
(AU : Nov./Dec.-2007, 2 Marks)

Solution : C_1 = 200 pF, C_2 = 50 pF, f = 1 MHz

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{200 \times 10^{-12} \times 50 \times 10^{-12}}{(200+50) \times 10^{-12}} = 40 \text{ pF}$$

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad \text{i.e. } 1 \times 10^6 = \frac{1}{2\pi\sqrt{L \times 40 \times 10^{-12}}}$$

$\therefore$ L = **0.6332 mH**



The system consists of many stages connected in cascade. Hence basically it is a multistage amplifier. The input is sound signal of a human speaker and the output is given to the loud speaker which is an amplified input signal. The input and the intermediate stages are small signal amplifiers. The sufficient voltage gain is obtained by all the intermediate stages. Hence these stages are called **voltage amplifiers**.

But the last stage gives an output to the load like a loud speaker. Hence the last stage must be capable of delivering an appreciable amount of a.c. power to the load. So it must be capable of handling large voltage or current swings or in other words large signals. The main aim is to develop sufficient power hence the voltage gain is not important, in the last stage. Such a stage, which develops and feeds sufficient power to the load like loudspeaker, servomotor, handling the large signals is called **Large Signal Amplifier** or **Power Amplifier.**

Power amplifiers find their applications in the public address systems, radio receivers, driving servomotor in industrial control systems, tape players, T.V. receivers, cathode ray tubes etc.

5.2 Features of Power Amplifiers

The various features of power amplifiers are,

1. A power amplifier is the last stage of multistage amplifier. The previous stages develop sufficient gain and the **input signal level or amplitude of a power amplifier is large** of the order of few volts.
2. The **output of power amplifier has large current and voltage swings**. As it handles large signals called power amplifiers.
3. **The h-parameter analysis** is applicable to the small signal amplifiers and hence **can not be used for the analysis of power amplifiers**. The analysis of power amplifiers is carried out graphically by drawing a load line on the output characteristics of the transistors used in it.

4. The power amplifiers i.e large signal amplifiers are used to feed the loads like loud speakers having low impedance. So for maximum power transfer the impedance matching is important. Hence **the power amplifiers must have low output impedance**. Hence common collecter or emitter follower circuit is very common in power amplifiers. The common emitter circuit with a step down transformer for impedance matching is also commonly used in power amplifiers.

5. The power amplifiers develop an a.c. power of the order of few watts. Similarly large power gets dissipated in the form of heat, at the junctions of the transistors used in the power amplifiers. **Hence the transistors used in the power amplifiers are of large size, having large power dissipation rating, called power transistors.** Such transistors have heat sinks. A heat sink is a metal cap having bigger surface area, press fit on the body of a transistor, to get more surface area, in order to dissipate the heat to the surroundings. In general, the power amplifiers have bulky components.

6. A faithful reproduction of the signal, after the conversion, is important. Due to nonlinear nature of the transistor characteristics, there exists a harmonic distortion in the signal. Ideally signal should not be distorted. **Hence the analysis of signal distortion in case of the power amplifiers is important.**

7. Many a times, the power amplifiers are used in public address systems and many audio circuits to supply large power to the loud speakers. **Hence power amplifiers are also called audioamplifiers or audio frequency (A.F.) power amplifiers.**

5.3 Classification of Large Signal Amplifiers

For an amplifier, a quiescent operating point (Q point) is fixed by selecting the proper d.c. biasing to the transistors used. The quiescent operating point is shown on the load line, which is plotted on the output characteristics of the transistor. The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of the power amplifiers are :

i) Class A ii) Class B iii) Class C and iv) Class AB

5.3.1 Class A Amplifiers

The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

Key Point: *For this class, position of the Q point is approximately at the midpoint of the load line.*

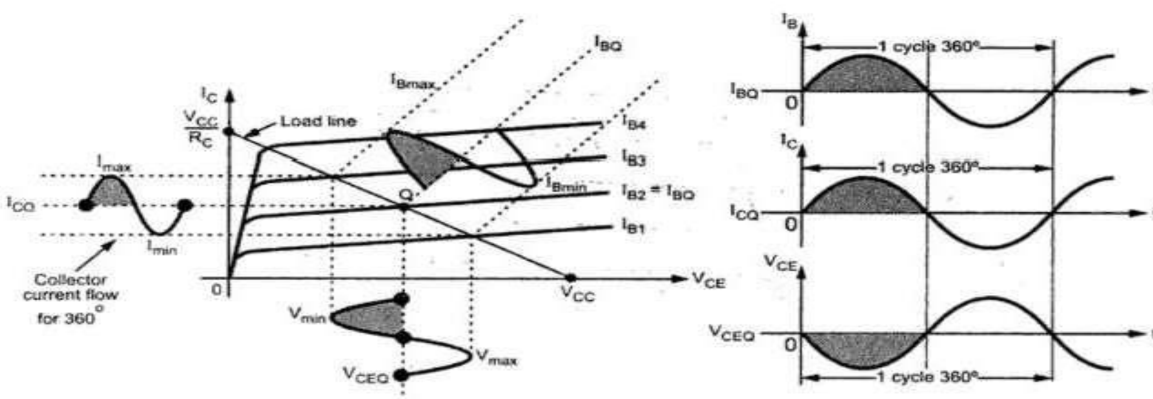
For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c. input signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360° (full cycle) of the input signal. In other words, the angle of the collector current flow is 360° i.e. one full cycle.

The current and voltage waveforms for a class A operation are shown with the help of output characteristics and the load line, in the Fig. 5.6.

As shown in the Fig. 5.6, for full input cycle, a full output cycle is obtained. Here signal is faithfully reproduced, at the output, without any distortion. This is an important feature of a class A operation. The efficiency of class A operation is very small.

▶ **Figure 5.6**

Waveforms representing class A operation



5.3.2 Class B Amplifiers

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle.

> **Key Point**: *For this operation, the Q point is shifted on X-axis i.e. transistor is biased to cut-off.*

Due to the selection of Q point on the X-axis, the transistor remains, in the active region, only for positive half cycle of the input signal. Hence this half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no signal is produced at the output. The collector current flows only for 180° (half cycle) of the input signal. In other words, the angle of the collector current flow is 180° i.e. one half cycle.

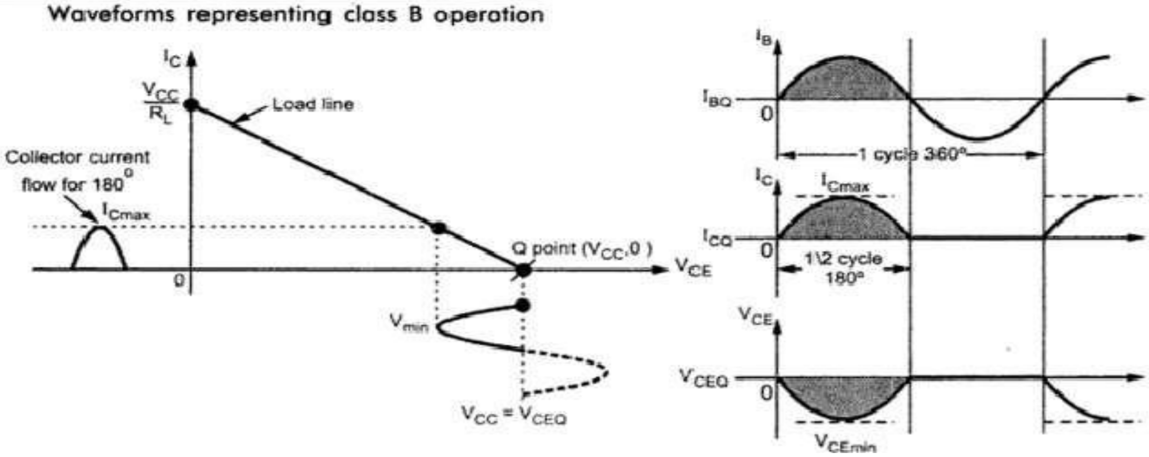
The current and voltage waveforms for a class B operation are shown in the Fig. 5.7.

As only a half cycle is obtained at the output, for full input cycle, the output signal is distorted in this mode of operation. To eliminate this distortion, practically two transistors are used in the alternate half cycles of the input signal. Thus overall a full cycle of output signal is obtained across the load. Each transistor conducts only for a half cycle of the input signal.

The efficiency of class B operation is much higher than the class A operation.

▶ **Figure 5.7**

Waveforms representing class B operation



5.3.3 Class C Amplifiers

The power amplifiers is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle.

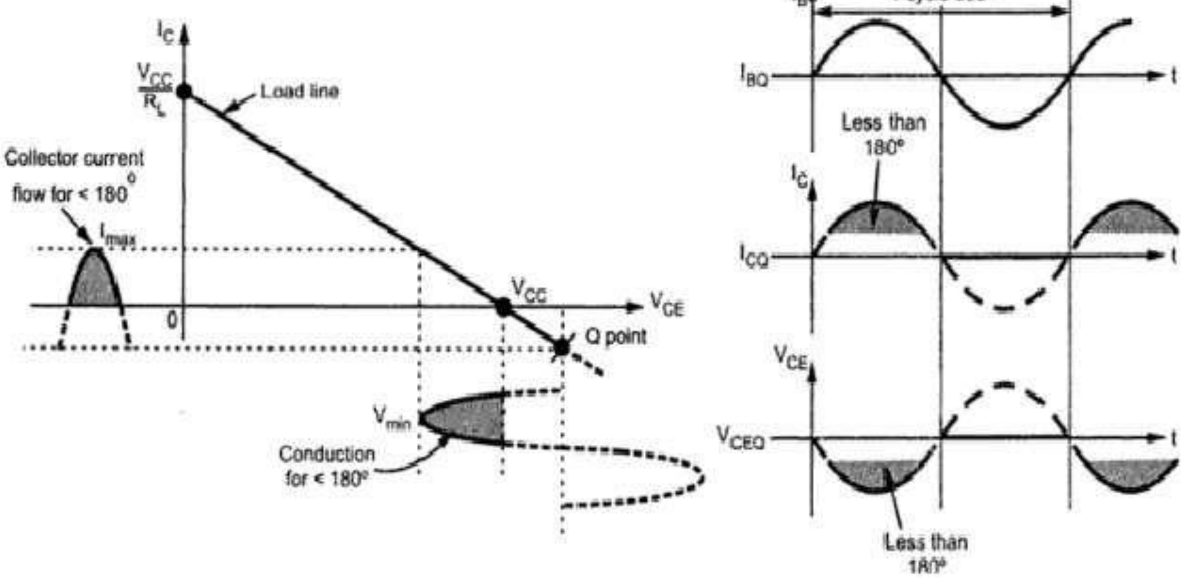
Key Point: *For this operation, the Q point is to be shifted below X-axis.*

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output. The angle of the collector current flow is less than 180°.

The current and voltage waveforms for a class C amplifier operation are shown in the Fig. 5.8.

► **Figure 5.8**

Waveform representing class C operation



Key Point: *In class C operation, the transistor is biased well beyond cut-off. As the collector current flows for less than 180°, the output is much more distorted and hence the class C mode is never used for A.F. power amplifiers.*

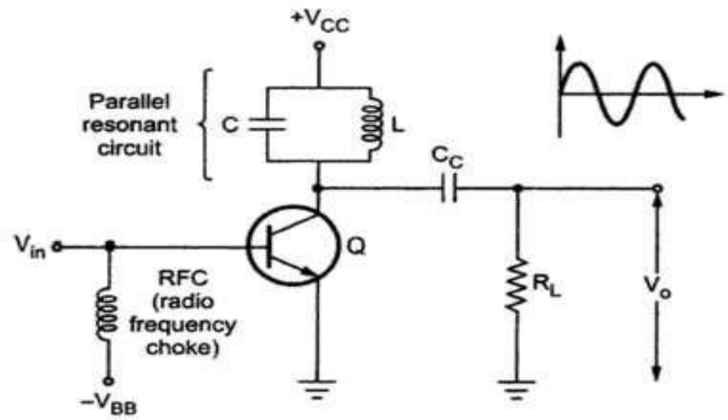
But the efficiency of this class of operation is much higher and can reach very close to 100%.

Applications : The class C operation is not suitable for audio frequency power amplifiers. The class C amplifiers are used in tuned circuits used in communication areas and in radio frequency (RF) circuits with tuned RLC loads. As used in tuned circuits, class C amplifiers are called **tuned amplifiers**. These are also used in mixer or converter circuits used in radio receivers and wireless communication systems.

The Fig. 5.9 shows the calss C tuned amplifier.

Figure 5.9

Class C tuned amplifier



The LC parallel circuit is a parallel resonant circuit. This circuit acts as a load impedance. Due to class C operation, the collector current consists of a series of pulses containing harmonics i.e. many other frequency components alongwith the fundamental frequency component of input. The parallel tuned circuit is designed to be tuned to the fundamental input frequency. Hence it elliminates the harmonics and produce a sine wave of fundamental component of input signal. As the transistor and coil losses are small, the most of the d.c. input power is converted to a.c. load power. Hence efficiency of class C is very high.

5.3.4 Class AB Amplifiers

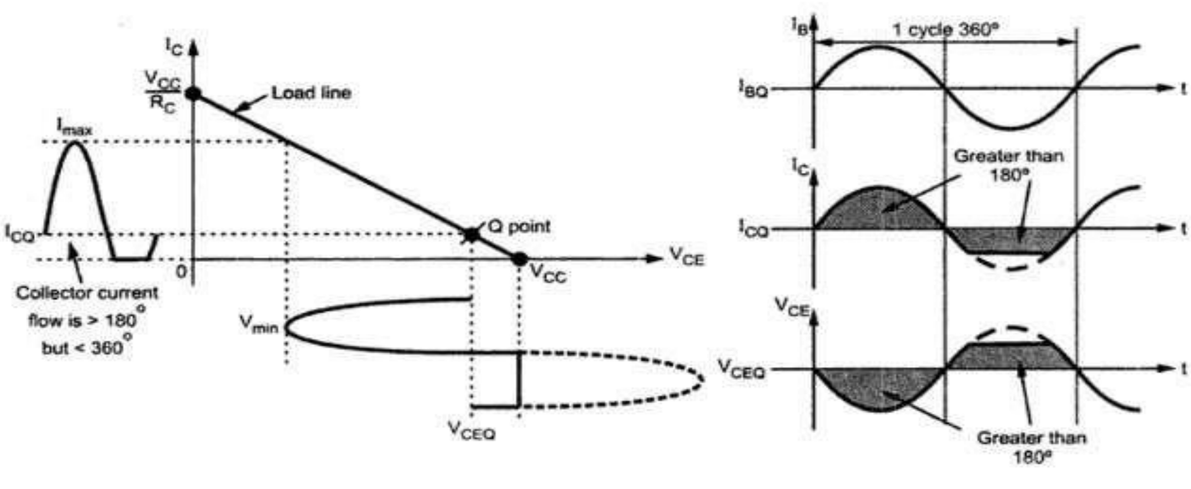
The power amplifier is said to be class AB amplifier, if the Q point and the input signal are selected such that the output signal is obtained for more than 180° but less than 360°, for a full input cycle.

Key Point: *The Q point position is above X-axis but below the midpoint of a load line.*

The current and voltage waveforms for a class AB operation, are shown in the Fig. 5.10.

Figure 5.10

Waveforms representing class AB operation



The output signal is distorted in class AB operation. The efficiency is more than class A but less than class B operation. The class AB operation is important to eliminate cross over distortion.

In general as the Q point moves away from the centre of the load line below towards the X-axis, the efficiency of class of operation increases.

5.5 Comparison of Amplifier Classes

The comparison of various amplifier classes is summarized in Table 5.1.

▶ **Table 5.1**

Class	A	B	C	AB
Operating Cycle	360°	180°	Less than 180°	180° to 360°
Position of Q point	Centre of load line	On X axis	Below X axis	Above X-axis but below the centre of load line
Efficiency	Poor, 25% to 50%	Better, 78.5%	High	Higher than A but less than B 50% to 78.5%
Distrotion	Absent No distortion	Present More than class A	Highest	Present

Key Point: *It is important to note that class C operation is never used for audio frequency amplifiers.*

This class is used in special areas of tuned circuits, such as radio or communications.

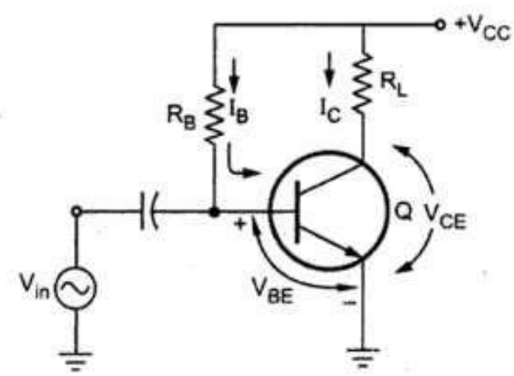
5.6 Analysis of Class A Amplifiers

The class A amplifiers are further classified as **directly coupled** and **transformer coupled** amplifiers. In directly coupled type, the load is directly connected in the collector circuit. While in the transformer coupled type, the load is coupled to the collector using a transformer called an output transformer. Let us study in detail the various aspects of the two types of Class A amplifiers.

5.7 Series Fed, Directly Coupled Class A Amplifier

▶ **Figure 5.13**

Large signal class A amplifier



A simple fixed-bias circuit can be used as a large signal class A amplifier as shown in the Fig. 5.13.

The difference between small signal version of this circuit is that the signals handled by this large signal circuit are of the order of few volts. Similarly the transistor used, is a power transistor. The value of R_B is selected in such a way that the Q point lies at the centre of the d.c. load line.

The circuit represents the directly coupled class A amplifier as the load resistance is directly connected in the collector circuit. Most of the times the load is a loudspeaker, the impedance of which varies from 3 to 4 ohms to 16 ohms. The beta of the transistor used is less than 100.

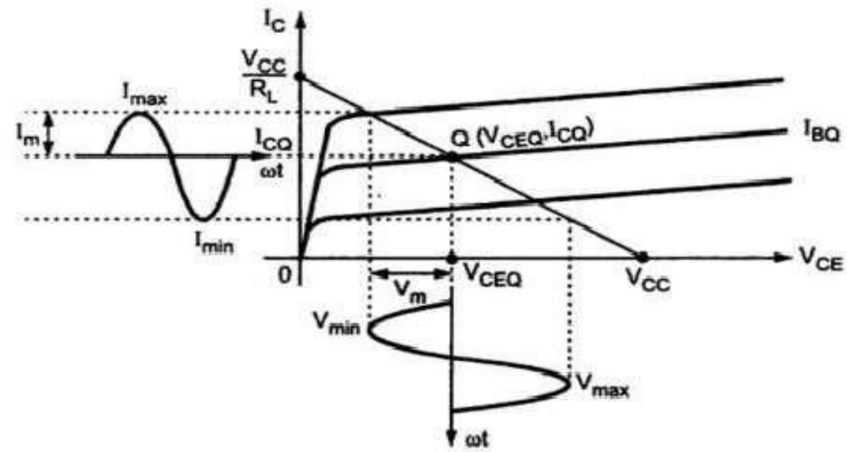
Key Point: *This is called **directly coupled**, as the load R_L is directly connected in the collector circuit of power transistor.*

The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

The graphical representation of a class A amplifier is shown in the Fig. 5.14.

▶ Figure 5.14

Graphical representation of class A amplifier



Applying Kirchhoff's voltage law to the circuit shown in the Fig. 5.13, we get

$$V_{CC} = I_C R_L + V_{CE}$$

$$\therefore \quad I_C R_L = -V_{CE} + V_{CC}$$

$$\therefore \quad I_C = \left[-\frac{1}{R_L}\right] V_{CE} + \frac{V_{CC}}{R_L} \qquad \dots (1)$$

The equation is similar to equation (1) of section 7.3 and thus the slope of the load line is $-\frac{1}{R_L}$ while the Y-intercept is $\frac{V_{CC}}{R_L}$.

The change is because the collector resistance R_C is named as load resistance R_L in this circuit. The Q point is adjusted approximately at the centre of the load line.

5.7.1 D.C.Operation

The collector supply voltage V_{CC} and resistance R_B decides the d.c. base-bias current I_{BQ}. The expression is obtained applying KVL to the B-E loop and with $V_{BE} = 0.7$ V.

$$\therefore \; I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \qquad \dots (2)$$

The corresponding collector current is then,

$$I_{CQ} = \beta \, I_{BQ} \qquad \dots (3)$$

From the equation (1), the corresponding collector to emitter voltage is,

$$V_{CEQ} = V_{CC} - I_{CQ} R_L \qquad \dots (4)$$

Hence the Q point can be defined as Q (V_{CEQ}, I_{CQ}).

5.7.2 D.C.Power Input

The d.c. power input is provided by the supply. With no a.c input signal, the d.c. current drawn is the collector bias current I_{CQ} . Hence d.c. power input is,

$$P_{DC} = V_{CC} \cdot I_{CQ} \quad \text{... (5)}$$

It is important to note that even if a.c. input signal is applied, the average current drawn from the d.c. supply remains same. Hence equation (5) represents d.c. power input to the class A series fed amplifier.

5.7.3 A.C. Operation

When an input a.c. signal is applied, the base current varies sinusoidally.

Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the Fig. 5.14.

The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector to emitter voltage varies around its quiescent value. The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

5.7.4 A.C.Power Output

For an alternating output voltage and output current swings, shown in the Fig. 5.14, we can write,

V_{min} = Minimum instantaneous value of the collector (output) voltage

V_{max} = Maximum instantaneous value of the collector (output) voltage

and V_{pp} = Peak to peak value of a.c. output voltage across the load.

$$\therefore V_{pp} = V_{max} - V_{min} \quad \text{... (6)}$$

Now V_m = Amplitude (peak) of a.c. output voltage as shown in the Fig. 5.14.

$$\therefore V_m = \frac{V_{pp}}{2} = \frac{V_{max} - V_{min}}{2} \quad \text{... (7)}$$

Similarly we can write for the output current as,

I_{min} = Minimum instantaneous value of the collector (output) current

I_{max} = Maximum instantaneous value of the collector (output) current

and I_{pp} = Peak to peak value of a.c. output (load) current

$$\therefore \quad I_{pp} = I_{max} - I_{min} \quad \text{... (8)}$$

Now I_m = Amplitude (peak) of a.c. output (load) current as shown in the Fig. 5.14

$$\therefore I_m = \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2} \quad \text{... (9)}$$

Hence the r.m.s. values of alternating output voltage and current can be obtained as,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \text{... (10)}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \text{... (11)}$$

Hence we can write,

$$V_{rms} = I_{rms} R_L \quad \text{... (12)}$$

i.e.

$$V_m = I_m R_L \quad \text{... (13)}$$

The a.c. power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

i) Using r.m.s values

$$P_{ac} = V_{rms} I_{rms} \quad \text{... (14)}$$

or

$$P_{ac} = I_{rms}^2 R_L \quad \text{... (15)}$$

or

$$P_{ac} = \frac{V_{rms}^2}{R_L} \quad \text{... (16)}$$

ii) Using peak values

$$P_{ac} = V_{rms} I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$\therefore$

$$P_{ac} = \frac{V_m I_m}{2} \quad \text{... (17)}$$

or

$$P_{ac} = \frac{I_m^2 R_L}{2} \quad \text{... (18)}$$

or

$$P_{ac} = \frac{V_m^2}{2 R_L} \quad \text{... (19)}$$

iii) Using peak to peak values

$$P_{ac} = \frac{V_m I_m}{2} = \frac{\left(\frac{V_{PP}}{2}\right)\left(\frac{I_{PP}}{2}\right)}{2}$$

$$P_{ac} = \frac{V_{pp} I_{pp}}{8} \quad \text{... (20)}$$

or

$$P_{ac} = \frac{I_{pp}^2 R_L}{8} \quad \text{... (21)}$$

or

$$P_{ac} = \frac{V_{PP}^2}{8 R_L} \quad \text{... (22)}$$

But as $V_{pp} = V_{max} - V_{min}$ and $I_{pp} = I_{max} - I_{min}$; from equation (20), the a.c. power can be expressed as below, for graphical calculations.

$$P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad \text{... (22)}$$

5.7.5 Efficiency

The efficiency of an amplifier represents the amount of a.c. power delivered or transferred to the load, from the d.c. source i.e. accepting the d.c. power input. The generalised expression for an efficiency of an amplifier is,

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \qquad \dots (24)$$

Now for class A operation, we have derived the expressions for P_{ac} and P_{dc}, hence using equations (5) and (23), we can write

$$\boxed{\% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100} \qquad \dots (25)$$

The efficiency is also called **conversion efficiency** of an amplifier.

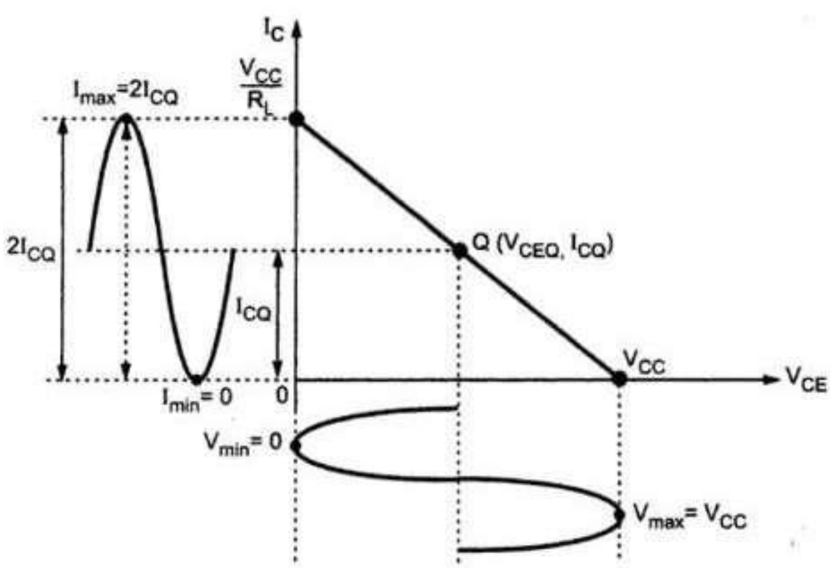
5.7.6 Maximum Efficiency

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. The maximum swings are shown in the Fig. 5.15.

From the Fig. 5.15, we can see that the minimum voltage possible is zero and maximum voltage possible is V_{CC}, for a maximum swing. Similarly the minimum current is zero and the maximum current possible is $2\ I_{CQ}$, for a maximum swing.

▶ Figure 5.15

Maximum voltage and current swings



$$\left.\begin{array}{l} V_{max} = V_{CC} \text{ and } V_{min} = 0 \\ I_{max} = 2 I_{CQ} \text{ and } I_{min} = 0 \end{array}\right\} \text{ for maximum swing}$$

Using equation (25) we can write,

$$\% \eta_{max} = \frac{(V_{CC}-0)(2I_{CQ}-0)}{8 V_{CC} I_{CQ}} \times 100 = \frac{2 V_{CC} I_{CQ}}{8 V_{CC} I_{CQ}} \times 100$$

$$= 25\%$$

Key Point: ***Thus the maximum efficiency possible in case of directly coupled series fed class A amplifier is just 25%.***

This maximum efficiency is an ideal value. For a practical circuit, it is much less than 25%, of the order of 10 to 15%.

Key Point: ***Very low efficiency is the biggest disadvantage of class A amplifier.***

5.7.7 Power Dissipation

As stated earlier, power dissipation in large signal amplifier is also large. The amount of power that must be dissipated by the transistor is the difference between the d.c. power input P_{dc} and the a.c. power delivered to the load P_{ac}.

$$P_d = \text{Power dissipation}$$

i.e.

$$\boxed{P_d = P_{DC} - P_{ac}} \quad \text{... (26)}$$

The maximum power dissipation occurs when there is zero a.c. input signal. When a.c. input is zero, the a.c. power output is also zero. But transistor operates at quiescent condition, drawing d.c. input power from the supply equal to V_{CC} I_{CQ}. This entire power gets dissipated in the form of heat. Thus d.c. power input without a.c. input signal is the maximum power dissipation.

$$\boxed{(P_d)max = V_{CC} I_{CQ}} \quad \text{... (27)}$$

Key Point: *Thus value of maximum power dissipation decides the maximum power dissipation rating of the transistor to be selected for the amplifier.*

5.7.8 Advantages and Disadvantages

The **advantages** of directly coupled class A amplifier can be stated as,

1. The circuit is simple to design and to implement
2. The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.
3. Less number of components required as load is directly coupled.

The disadvantages are :

1. The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
2. Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
3. The output impedance is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
4. The efficiency is very poor, due to large power dissipation.

Example 5.1 : *A series fed class A amplifier shown in Fig. 5.16, operates from D.C. source and applied sinusoidal input signal generates peak base current 9 mA. Calculate :*

i) Quiescent current I_{CQ}

ii) Quiescent voltage V_{CEQ}

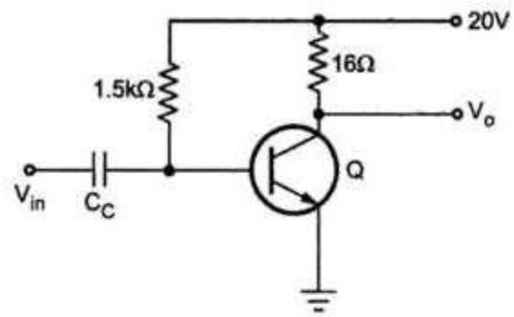
iii) D.C. input power P_{DC}

iv) A.C. output power P_{ac}

v) Efficiency.

Assume $\beta = 50$ and $V_{BE} = 0.7$ V.

Figure 5.16



Solution :

i) $\mathbf{I_{CQ}}$ $\quad I_{BQ} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{20-0.7}{1.5 \times 10^3} = 12.87 \text{ mA}$

$$I_{CQ} = \beta \times I_{BQ} = 50 \times 12.87 = 643.50 \text{ mA}$$

ii) $\mathbf{V_{CEQ}}$ $\quad V_{CC} = I_{CQ} R_L + V_{CEQ}$

$$\therefore V_{CEQ} = V_{CC} - I_{CQ} R_L = 20 - 643.50 \times 10^{-3} \times 16 = 9.70 \text{ volts}$$

iii) $\mathbf{P_{DC}}$ $\quad P_{DC} = V_{CC} \times I_{CQ} = 20 \times 643.5 \times 10^{-3} = 12.87 \text{ watt}$

iv) $\mathbf{P_{ac}}$ Peak current $i_b = 9$ mA

$$i_c = \beta i_b = 50 \times 9 = 450 \text{ mA (peak)}$$

$$\therefore \quad i_{c(rms)} = \frac{i_{c\,(peak)}}{\sqrt{2}} = \frac{450}{\sqrt{2}} = 318.19 \text{ mA} = I_{rms}$$

$$\therefore P_{ac} = I_{rms}^2 R_L = (318.19 \times 10^{-3})^2 \times 16 = 1.619 \text{ watt.}$$

v) **Efficiency** $\quad \eta = \dfrac{P_{ac}}{P_{DC}} \times 100 = \dfrac{1.619}{12.87} \times 100 = 12.58 \%$

Ans. : $I_{CQ} = 643.5$ mA, $V_{CEQ} = 9.7$ V, $P_{DC} = 12.87$ W, $P_{ac} = 1.619$ W, $\eta = 12.58\%$

5.8 Transformer Coupled Class A Amplifier

As stated earlier, for maximum power transfer to the load, the impedance matching is necessary. For loads like loudspeaker, having low impedance values, impedance matching is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directly coupled class A amplifier is very much high. This problem can be eliminated by using a transformer to deliver power to the load.

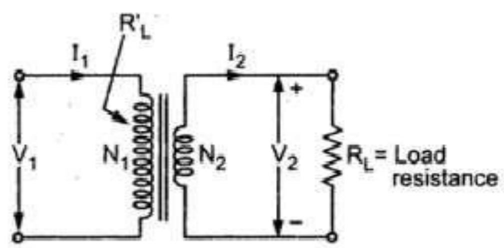
Key Point: *The transformer is called an* ***output transformer*** *and the amplifier is called* ***transformer coupled class A amplifier.***

Before studying the operation of the amplifier, let us revise few concepts regarding the transformer.

5.8.1 Properties of Transformer

Figure 5.17

Transformer with load



Consider a transformer as shown in the Fig. 5.17 which is connected to a load of resistance R_L.

While analysing the transformer, it is assumed that the transformer is ideal and there are no losses in the transformer. Similarly the winding resistances are assumed to be zero.

Let N_1 = Number of turns on primary

N_2 = Number of turns on secondary

V_1 = Voltage applied to primary

V_2 = Voltage on secondary

I_2 = Primary current

i) Turns Ratio : The ratio of number of turns on secondary to the number of turns on primary is called turns ratio of the transformer denoted by n.

$$\therefore n = \text{Turns ratio} = \frac{N_2}{N_1} \quad \text{... (1)}$$

Some times it is specified as $\frac{N_2}{N_1} : 1$ or $\frac{N_1}{N_2} : 1$.

ii) Voltage Transformation : The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be step up or step down transformer.

$$\therefore \frac{V_2}{V_1} = \frac{N_2}{N_1} = n \quad \text{... (2)}$$

In the amplifier analysis, the load impedance is going to be small. And the transformer is to be used for impedance matching. Hence it has to be a step down transformer. Hence number of turns on primary are more than the secondary and turns ratio is less than unity, for such a step down transformer.

iii) Current Transformation : The current in the secondary winding is inversely proportional to the number of turns of the windings.

$$\therefore \frac{I_2}{I_1} = \frac{N_1}{N_2} = \frac{1}{n} \qquad \text{... (3)}$$

iv) Impedance Transformation : As current and voltage get transformed from primary to secondary, an impedance 'seen' from either side (primary or secondary) also changes.

Now the impedance of the load on secondary is R_L as shown in the Fig. 5.17. The primary and secondary winding resistances are assumed to be zero. This load impedance R_L, gets reflected on the primary side and behaves as if connected in the primary side. Such impedance transferred from secondary to primary is denoted as R_L'.

Now using the equations (2) and (3) and the Fig. 5.17, we can write,

$$R_L = \frac{V_2}{I_2} \text{ and } R_L' = \frac{V_1}{I_1}$$

but $$V_1 = \frac{N_1}{N_2} V_2 \text{ and } I_1 = \frac{N_2}{N_1} I_2$$

$$\therefore R_L' = \frac{\frac{N_1}{N_2} V_2}{\frac{N_2}{N_1} I_2} = \left(\frac{N_1}{N_2}\right)^2 \times \frac{V_2}{I_2} = \frac{R_L}{\left(\frac{N_2}{N_1}\right)^2} = \frac{R_L}{n^2}$$

$$\therefore R_L' = \frac{R_L}{n^2} = \left(\frac{N_1}{N_2}\right)^2 R_L \qquad \text{... (4)}$$

The R_L' is the **reflected impedance** and is related to the square of the turns ratio of the transformer. Remember that for a step down transformer, the secondary voltage is less than the primary. And high voltage side is always high impedance side. **Hence R_L' is always higher than R_L, for a stepdown transformer.**

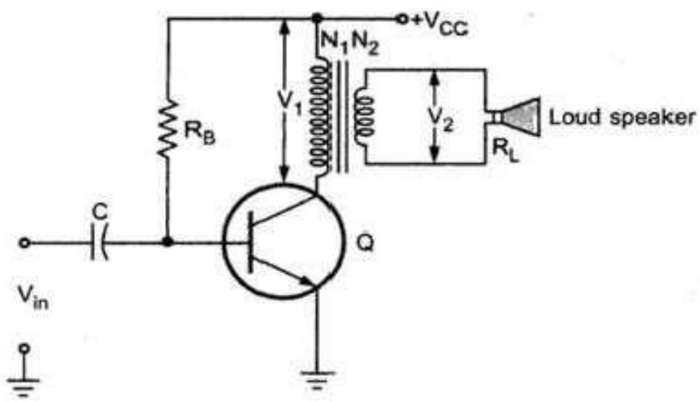
Key Point: *In the amplifier analysis, the load is on secondary while the active device, the transistor is on primary. Hence in all the calculations related to the transistor, the reflected load impedance R_L' must be considered rather than actual load impedance R_L.*

5.8.2 Circuit Diagram of Transformer Coupled Amplifier

The basic circuit of a transformer coupled amplifier is shown in the Fig. 5.18. The loudspeaker connected to the secondary acts as a load having impedance of R_L ohms.

▶ **Figure 5.18**

Transformer coupled class A amplifier



The transformer used is a step down transformer with the turns ratio as

$$n = N_2/N_1.$$

5.8.3 D.C. Operation

It is assumed that the winding resistances are zero ohms. Hence for d.c. purposes, the resistance is 0 Ω. There is no d.c. voltage drop across the primary winding of the transformer. The slope of the d.c. load line is reciprocal of the d.c. resistance in the collector circuit, which is zero in this case. Hence slope of the d.c. load line is ideally infinite. This tells that the d.c. load line in the ideal condition is a vertically straight line.

Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - V_{CE} = 0$$

i.e. $V_{CC} = V_{CE}$ ... drop across winding is zero

This is the d.c. bias voltage V_{CEQ} for the transistor.

So $$V_{CEQ} = V_{CC} \quad \text{... (5)}$$

Hence the d.c. load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{CC}$.

The intersection of d.c. load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is I_{CQ}.

The d.c. load line is shown in the Fig. 5.19.

5.8.4 D.C Power Input

The d.c. power input is provided by the supply voltage with no signal input, the d.c. current drawn is the collector bias current I_{CQ}.

Hence the d.c. power input is given by,

So $$P_{DC} = V_{CC} I_{CQ} \quad \text{... (6)}$$

The expression is same as derived earlier for series fed directly coupled class A amplifier.

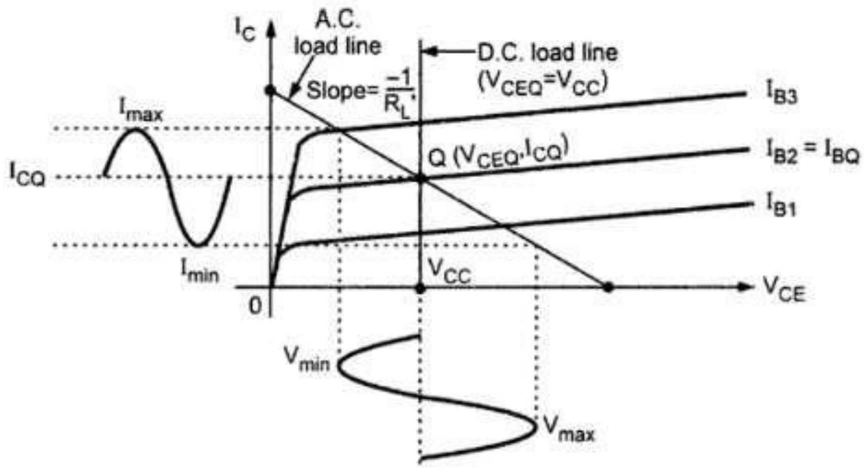
5.8.5 A.C. Operation

For the a.c. analysis, it is necessary to draw an a.c. load line on the output characteristics.

For a.c. purposes, the load on the secondary is the load impedance R_L ohms. And the reflected load on the primary i.e. R'_L can be calculated using the equation (4). The load line drawn with a slope of $\left(\frac{-1}{R'_L}\right)$ and passing through the operating point i.e. quiescent point Q is called **a.c. load line.** The d.c. and a.c. load lines are shown in the Fig. 5.19.

▶ Figure 5.19

Load lines for transformer coupled class A amplifier



The output current i.e. collector current varies around its quiescent value I_{CQ}, when a.c. input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value V_{CEQ} which is V_{CC} in this case.

5.8.6 A.C. Output Power

The a.c. power developed is on the primary side of the transformer. While calculating this power, the primary values of voltage and current and reflected load R'_L must be considered. The a.c. power delivered to the load is on the secondary side of the transformer. While calculating load voltage, load current, load power the secondary voltage, current and the load R_L must be considered.

Let V_{1m} = Magnitude or peak value of primary voltage

V_{1rms} = R.M.S value of primary voltage

I_{1m} = Peak value of primary current

I_{1rms} = R.M.S value of primary current.

Hence the a.c. power developed on the primary is given by,

$$P_{ac} = V_{1rms} I_{1rms} \quad \ldots (7)$$

$$P_{ac} = I^2_{1rms} R'_L \quad \ldots (8)$$

$$P_{ac} = \frac{V_{1rms}^2}{R'_L} \quad \dots (9)$$

$$P_{ac} = \frac{V_{1m}}{\sqrt{2}} \cdot \frac{I_{1m}}{\sqrt{2}} = \frac{V_{1m} I_{1m}}{2} \quad \dots (10)$$

$$P_{ac} = \frac{I_{1m}^2 R'_L}{2} \quad \dots (11)$$

$$P_{ac} = \frac{V_{1m}^2}{2 R'_L} \quad \dots (12)$$

Similarly the a.c. power delivered to the load on secondary, also can be calculated, using secondary quantities.

Let V_{2m} = Magnitude or peak value of secondary or load voltage

$V_{2\,rms}$ = R.M.S value of secondary or load voltage

I_{2m} = Magnitude or peak value of secondary or load current.

I_{2rms} = R.M.S. value of secondary or load current

$$P_{ac} = V_{2rms} \; I_{2rms} = I_{2rms}^2 \; R_L = \frac{V_{2rms}^2}{R_L} \quad \dots (13)$$

or

$$P_{ac} = \frac{V_{2m} \; I_{2m}}{2} = \frac{I_{2m}^2 R_L}{2} = \frac{V_{2m}^2}{2 R_L} \quad \dots (14)$$

Power delivered on primary is same as power delivered to the load on secondary, assuming **ideal transformer**. Primary and Secondary values of voltages and currents are related to each other through the turns ratio of the transformer.

Key Point: *In practical circuit, the transformer can not be ideal. Hence the power delivered to the load on the secondary is slightly less than power developed on the primary. In such case, the transformer efficiency must be considered for calculating various parameters on the primary and secondary sides of the transformer.*

The slope of the a.c. load line can be expressed in terms of the primary current and the primary voltage.

The slope of the a.c. load line is,

$$= \frac{1}{R'_L} = \frac{I_{1m}}{V_{1m}} \quad \dots (15)$$

The generalised expression for a.c. power output represented by the equation (24) in section (5.7), can be used as it is for transformer coupled amplifier. The expression is mentioned again for the convenience of the reader.

$$\therefore P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad \dots (16)$$

Key Point: *The a.c. power calculated is the power developed across the primary winding of the output transformer. Assuming ideal transformer, the power delivered to the load on secondary, is same as that developed across the primary. If the transformer efficiency is known, the power delivered to the load must be calculated from the power developed on the primary, considering the efficiency of the transformer.*

5.8.7 Efficiency

The general expression for the efficiency remains same as that given by equations (24) and (25) in section 5.7.

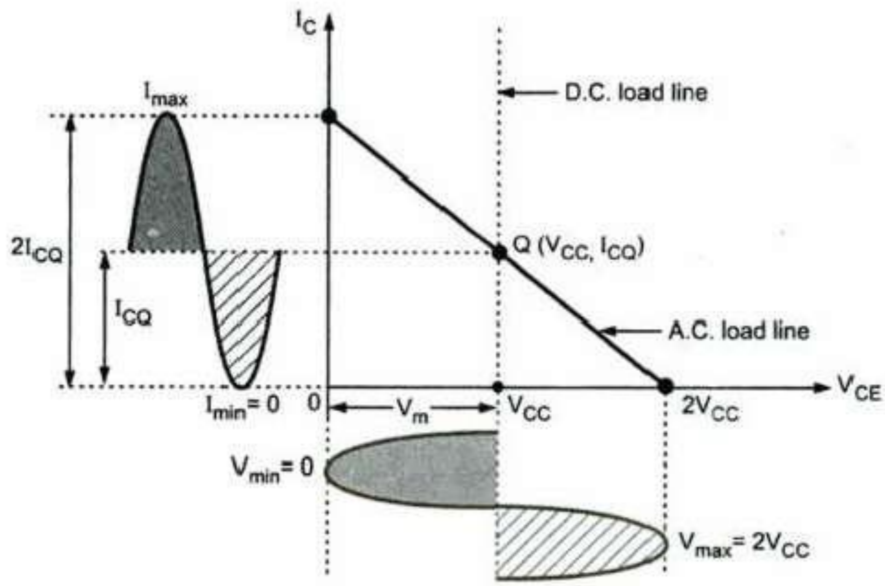
$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100$$

5.8.8 Maximum Efficiency

Assume maximum swings of both the output voltage and output current, to calculate maximum efficiency, as shown in the Fig. 5.20.

▶ Figure 5.20

Maximum voltage and current swings



From the Fig. 5.20, assuming that the Q point is exactly at the centre of the load line, for maximum swing we can write,

$$\left.\begin{array}{l} V_{min} = 0 \text{ and } V_{max} = 2V_{CC} \\ I_{min} = 0 \text{ and } I_{max} = 2I_{CQ} \end{array}\right\} \text{for maximum swing}$$

Using equation (25) of section 5.7,

$$\% \eta_{max} = \frac{(2V_{CC} - 0)(2I_{CQ} - 0)}{8 V_{CC} I_{CQ}} \times 100$$

$$= \frac{4 V_{CC} I_{CQ}}{8 V_{CC} I_{CQ}} \times 100 = 50\%$$

Key Point: *Hence maximum possible theoretical efficiency in case of transformer coupled class A amplifier is 50%.*

For practical circuit it is about 30 to 35%, which is still much more than the directly coupled amplifier. For maximum efficiency, the power output is also maximum. For such maximum output power condition, it is seen that

$$V_{min} = 0 \text{ fand } V_{max} = 2\,V_{CC}$$

i.e. V_{1m} = peak value of primary voltage

$$= \frac{V_{max} - V_{min}}{2} = V_{CC}$$

$$\therefore V_{1m} = V_{CC} \text{ for maximum output power.}$$

Similarly from the maximum output current swing shown in the Fig. 5.20, we can say that the peak value of the output current is magnitude wise equal to the biasing collector current.

$$\therefore I_{1m} = I_{CQ} \text{ magnitude wise for maximum output power.}$$

Hence the equation (15) written for the magnitude of the slope of the a.c. load line can be modified as,

$$R'_L = \frac{V_{1m}}{I_{1m}} = \frac{V_{CC}}{I_{CQ}} \qquad \text{... (15 a)}$$

Key Point: *This expression is applicable only in case of maximum power output condition.*

$$(P_{ac}) \max = \frac{1}{2}\frac{V_{CC}^2}{R'_L} \qquad \text{... as } V_{1m} = V_{CC}$$

5.8.9 Power Dissipation

The power dissipation by the transistor is the difference between the a.c. power output and the d.c. power input. The power dissipated by the transformer is very small due to negligible (d.c.) winding resistances and can be neglected.

$$\therefore P_d = P_{DC} - P_{ac} \qquad \text{... (16)}$$

When the input signal is larger, more power is delivered to the load and less is the power dissipation. But when there is no input signal, the entire d.c. input power gets dissipated in the form of heat, which is the maximum power dissipation.

$$\therefore (P_d)_{max} = V_{CC}\, I_{CQ} \qquad \text{... (17)}$$

Thus the class A amplifier dissipates less power when delivers maximum power to the load. While it dissipates maximum power while delivering zero power to the load i.e. when load is removed and there is no a.c. input signal. The maximum power dissipation decides the maximum power dissipation rating for the power transistor to be selected for an amplifier.

5.8.10 Advantages and Disadvantages

The **advantages** of transformer coupled class **A amplifier** circuit are,

1. The efficiency of the operation is higher than directly coupled amplifier.
2. The d.c. bias current that flows through the load in case of directly coupled amplifier is stopped in case of transformer coupled.
3. The impedance matching required for maximum power transfer is possible.

The **disadvantages** are,

1. Due to the transformer, the circuit becomes bulkier, heavier and costlier compared to directly coupled circuit.
2. The circuit is complicated to design and implement compared to directly coupled circuit.
3. The frequency response of the circuit is poor.

Example 5.4 : *The loudspeaker of 8 Ω is connected to the secondary of the output transformer of a class A amplifier circuit. The quiescent collector current is 140 mA. The turns ratio of the transformer is 3:1. The collector supply voltage is 10V. If a.c. power delivered to the loudspeaker is 0.48 W, assuming ideal transformer, calculate :*

1. A.C. power developed across primary

2. R.M.S. value of load voltage

3. R.M.S. value of primary voltage

4. R.M.S. value of load current

5. R.M.S. value of primary current

6. The D.C. power input

7. The efficiency

8. The power dissipation

Solution : $R_L = 8\ \Omega,\ I_{CQ} = 140\ mA,\ V_{CC} = 10\ V$

$$P_{ac} = 0.48\ W$$

The turns ratio are specified as $\frac{N_1}{N_2} : 1$ i.e. 3:1

$$\therefore \frac{N_1}{N_2} = 3$$

$$\therefore n = \frac{N_2}{N_1} = \frac{1}{3} = 0.3333$$

$$\therefore R'_L = \frac{R_L}{n^2}$$

$$= \frac{8}{(0.333)^2} = 72\ \Omega$$

1. As the transformer is ideal, whatever is the power delivered to the load, same is the power developed across primary.

$$\therefore P_{ac} \text{ (across primary)} = 0.48\ W$$

2. Using equation (9),

we get, $P_{ac} = \frac{V_{1rms}^2}{R_L'}$

$$\therefore 0.48 = \frac{V_{1rms}^2}{72}$$

$$V_{1rms}^2 = 34.56$$

$$\therefore V_{1rms} = 5.8787 \text{ V on primary.}$$

But r.m.s. value of the load voltage is V_{2rms}

So $\frac{(V_1)_{rms}}{(V_2)_{rms}} = \frac{N_1}{N_2} = \frac{3}{1}$

$$\therefore (V_2)_{rms} = \frac{(V_1)_{rms}}{3} = \frac{5.8787}{3} = 1.9595 \text{ V}$$

This is the r.m.s. value of the load voltage.

3. The r.m.s value of the primary voltage is $(V_1)_{rms}$ as calculated above.

$$\therefore (V_1)_{rms} = 5.8787 \text{ V}$$

4. The power delivered to the load $= I_{2rms}^2 \times R_L$ ... refer eq. 13.

$$\therefore 0.48 = I_{2rms}^2 \times 8$$

$$\therefore I_{2rms}^2 = 0.06$$

$$\therefore I_{2rms} = 0.2449 \text{ A}$$

This is the r.m.s value of the load current as the resistance value used is R_L and not R_L'.

5. The r.m.s values of primary and secondary are related through the transformation ratio.

$$\therefore \frac{(I_1)_{rms}}{(I_2)_{rms}} = \frac{N_2}{N_1} = n = 0.333$$

$$\therefore (I_1)_{rms} = (I_2)_{rms} \times n = 0.2449 \times 0.333 = 0.0816\text{A} = 81.64 \text{ mA.}$$

6. The d.c. power input is,

$$P_{DC} = V_{CC} I_{CQ} = 10 \times 140 \times 10^{-3} = 1.4 \text{ W}$$

7. $$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{0.48}{1.4} \times 100 = 34.28\%$$

8. $$P_d = P_{DC} - P_{ac} = 1.4 - 0.48 = 0.92 \text{ W}$$

This is the power dissipation.

■

5.9 Distortion in Amplifiers

The input signal applied to the amplifiers is alternating in nature. The basic features of any alternating signal are amplitude, frequency and phase. The amplifier output should be reproduced faithfully i.e. there should not be the change or distortion in the amplitude, frequency and phase of the signal. Hence the possible distortions in any amplifier are amplitude distortion, phase distortions and frequency distortion. But the phase distortions are not detectable by human ears as human ears are insensitive to the phase changes. While **the change in gain of the amplifier with respect to the frequency is called frequency distortion**.

Key Point: *The frequency distortion is not significant in A.F. power amplifiers.*

In the earlier discussion, it is assumed that the transistor is perfectly linear device. That is the dynamic characteristics of a transistor is a straight line over the operating range [$i_c = Ki_b$]. But in practical circuits, the dynamic characteristics is not perfectly linear. Due to such nonlinearity in the dynamic characteristics, the waveform of the output voltage differs from that of the input signal. Such a distortion is called **nonlinear distortion** or **amplitude distortion** or **harmonic distortion**.

Key Point: *The harmonic distortion plays an important role in the analysis of A.F. power amplifiers.*

Let us see, what is the exact meaning of harmonic distortion and how it affects the waveform of the output signal.

5.9.1 Harmonic Distortion

The harmonic distortion means the presence of the frequency components in the output wave form, which are not present in the input signal. The component with frequency same as the input signal is called fundamental frequency component. The additional frequency components present in the output signal are having frequency components which are integer multiples of fundamental frequency component. These components are called harmonic components or harmonics. For example if the **fundamental frequency** is f Hz, then the output signal contains fundamental frequency component at f Hz and additional frequency components at 2f Hz, 3f Hz, 4f Hz and so on. The 2f component is called **second harmonic**, the 3f component is called **third harmonic** and so on. The fundamental frequency component is not considered as a harmonic. Out of all the harmonic components, the second harmonic has the largest amplitude.

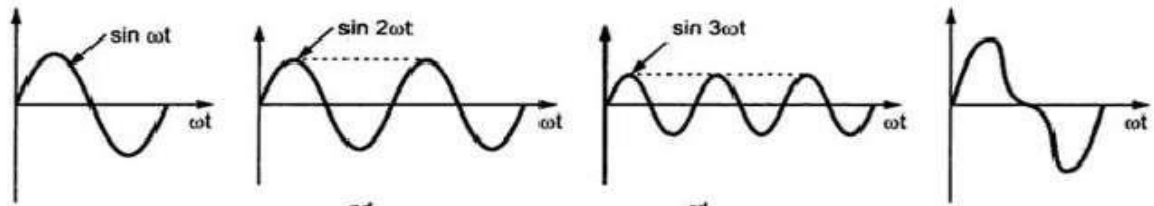
Key Point: *As the order of the harmonic increases, its amplitude decreases.*

As the second harmonic amplitude is largest, the second harmonic distortion is more important in the analysis of A.F. power amplifiers. The Fig. 5.21 shows the various harmonic components.

It can be seen from the Fig. 5.21 that the distorted waveform can be obtained by adding the fundamental and the harmonic components. The percentage harmonic distortion due to each order (2^{nd}, 3^{rd} and so on) can be calculated by comparing the amplitude of each order of harmonic with the amplitude of the fundamental frequency component.

► **Figure 5.21**

Distortion due to harmonic components



If the fundamental frequency component has an amplitude of B_1 and the n^{th} harmonic component has an amplitude of B_n then the percentage harmonic distortion due to n^{th} harmonic component is expressed as,

$$\%\ n^{th} \text{ harmonic distortion} = \%\ D_n = \frac{|B_n|}{|B_1|} \times 100 \quad \ldots (1)$$

So $$\%\ D_2 = \frac{|B_2|}{|B_1|},\ \%\ D_3 = \frac{|B_3|}{|B_1|} \text{ and so on.}$$

5.9.2 Total Harmonic Distortion

When the output signal gets distorted due to various harmonic distortion components, the total harmonic distortion, which is the effective distortion due to all the individual components is given by

$$\%D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \ldots} \times 100 \quad \ldots (2)$$

where D = Total Harmonic Distortion

As stated earlier, the most important component in the distortion is the second harmonic distortion. Let us discuss the graphical method of calculating second harmonic distortion.

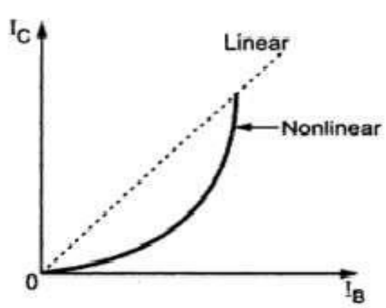
5.9.3 Second Harmonic Distortion (Three Point Method)

To investigate the second harmonic distortion, assume that the dynamic transfer characteristics of the transistor is parabolic (nonlinear) in nature rather than a straight line (linear) as shown in the Fig. 5.22.

As discussed earlier such type of nonlinearity introduces harmonic distortion, in which second harmonic distortion is the most dominant.

► **Figure 5.22**

Nonlinear dynamic characteristics



Let an a.c. input signal, causes the base current swing which is cosine in nature

$$\therefore\ i_b = I_{Bm} \cos \omega t \quad \ldots (3)$$

Due to this, collector current swings around its quiescent value but the relation between i_b and i_c is nonlinear as shown in the Fig. 5.22.

Mathematically this can be expressed as,

$$i_c = G_1\ i_b + G_2\ i_b^2$$
$$= G_1\ I_{Bm} \cos \omega t + G_2\ I_{Bm}^2 \cos^2 \omega t \quad \ldots (4)$$

But $\cos^2 \omega t = \frac{1+\cos 2\omega t}{2}$

Substituting in equation (4),

$$i_c = G_1 I_{Bm} \cos \omega t + G_2 I_{Bm}^2 \left(\frac{1+\cos 2\omega t}{2} \right)$$

$$\therefore i_c = G_1 I_{Bm} \cos \omega t + \frac{1}{2} G_2 I_{Bm}^2 + \frac{G_2}{2} I_{Bm}^2 \cos 2\omega t$$

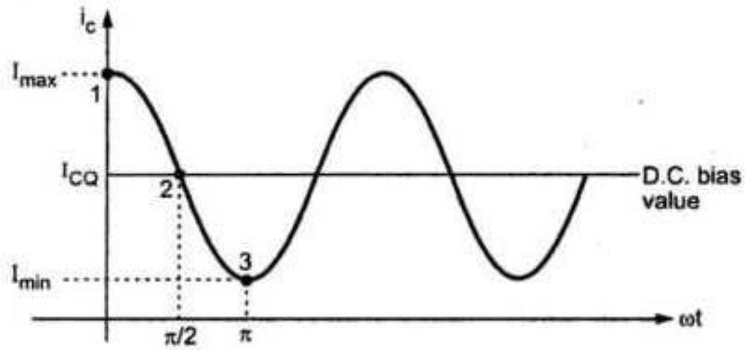
$$\boxed{\therefore i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t} \quad \dots (5)$$

The last term represents the second harmonic component. Thus the equation shows that, there is second harmonic component present.

Hence the total collector current waveform can be shown as in the Fig. 5.23, which is swinging about its quiescent value I_{CQ}.

▶ Figure 5.23

Output current waveform



Hence the total collector current can be expressed in terms of its d.c. bias value, d.c. signal component, fundamental frequency and second harmonic component as,

$$\boxed{i_c = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t} \quad \dots (6)$$

where $(I_{CQ} + B_0)$ = The d.c. component, independent of time

where $(I_{CQ} + B_0)$ = The d.c. component, independent of time

B_1 = Amplitude of the fundamental frequency

B_2 = Amplitude of the second harmonic component

It can be seen that due to the presence of harmonics, the d.c. current increases. **Practically the presence of harmonics can be detected by connecting milliammeter in the collector circuit. The readings can be observed without an a.c. input signal and with a.c. input signal. If the two readings are almost same there are no harmonics present. But if milliammeter shows an increase in the current, when an a.c. input is applied, then the harmonics can be concluded to be present in the output signal.**

Let us find out the value of the total collector current at the various instants 1, 2 and 3, shown in the Fig. 5.23.

At point 1, $\omega t = 0$, substituting in (6) we get,

$$\therefore i_c = I_{CQ} + B_0 + B_1 + B_2 \quad \dots (7)$$

At point 2, $\omega t = \frac{\pi}{2}$,

$$\therefore i_c = I_{CQ} + B_0 - B_2 \quad \dots (8)$$

At point 3, $\omega t = \pi$,

$$\therefore i_c = I_{CQ} + B_0 - B_1 + B_2 \quad \dots (9)$$

But at $\omega t = 0$, $i_c = I_{max}$

at $\omega t = \frac{\pi}{2}$, $i_c = I_{CQ}$

at $\omega t = \pi$, $i_c = I_{min}$

Hence the equations get modified as,

$$I_{max} = I_{CQ} + B_0 + B_1 + B_2 \quad \dots (10)$$

$$I_{CQ} = I_{CQ} + B_0 - B_2 \quad \dots (11)$$

$$I_{min} = I_{CQ} + B_0 - B_1 + B_2 \quad \dots (12)$$

From equation (11),

$$\boxed{B_0 = B_2} \quad \dots (13)$$

Now $I_{max} - I_{min} = 2B_1$

$$\boxed{\therefore B_1 = \frac{I_{max} - I_{min}}{2}} \quad \dots (14)$$

$$\begin{aligned} I_{max} + I_{min} &= 2I_{CQ} + 2B_0 + 2B_2 \\ &= 2I_{CQ} + 2B_2 + 2B_2 \quad \dots \text{ as } B_0 = B_2 \\ &= 2I_{CQ} + 4B_2 \end{aligned}$$

$$\boxed{\therefore B_2 = \frac{I_{max} + I_{min} - 2\,I_{CQ}}{4}} \quad \dots (15)$$

As the amplitudes of the fundamental and second harmonic are known, the second harmonic distortion can be calculated as,

$$\% D_2 = \frac{|B_2|}{|B_1|} \times 100 \quad \dots (16)$$

As the method uses three points on the collector current waveform to obtain the amplitudes of the harmonics, the method is called **'Three Point Method'** of determining the second harmonic distortion.

5.9.4 Power Output Due to Distortion

When the distortion is negligible, the power delivered to the load is given by,

$$P_{ac} = \frac{I_m^2 \ R_L}{2} \qquad \text{... refer equation (18) in section 5.7}$$

But $\quad I_m$ = peak value of the output current

$$= \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2} \qquad \text{... refer equation (9) in section 5.7}$$

But $$B_1 = \frac{I_{max} - I_{min}}{2}$$

$$\therefore I_m = B_1 = \text{fundamental frequency component}$$

$$\therefore P_{ac} = \frac{1}{2} B_1^2 R_L \qquad \text{... (17)}$$

With distortion, the power delivered to the load increases proportional to the amplitude of the harmonic component.

$$\therefore (P_{ac}')_D = \text{A.C. power output with harmonic distortion}$$

$$= \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + \cdots$$

$$\therefore (P_{ac})_D = \frac{1}{2} B_1^2 R_L \left(1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + \cdots \right)$$

$$\boxed{\therefore (P_{ac})_D = \frac{1}{2} B_1^2 R_L (1 + D_2^2 + D_3^2 + \cdots)}$$

$$\boxed{\therefore (P_{ac})_D = P_{ac} [1 + D^2]} \quad \ldots D^2 = D_2^2 + D_3^2 + \cdots \qquad \text{... (18)}$$

This is the power delivered to the load due to the harmonic distortion.

5.9.5 Higher Order Harmonic Distortion (Five Point Method)

As the nonlinearity present in dynamic characteristics increases, the order of the harmonic distortion also increases.

Let the mathematical expression for the collector current due to higher order harmonics be,

$$i_c = G_1 \ i_b + G_2 \ i_b^2 + G_3 \ i_b^3 + G_4 \ i_b^4 \qquad \text{... (19)}$$

Substituting the input signal $i_b = I_{Bm} \cos \omega t$ we get,

$$i_c = G_1 \ I_{Bm} \cos \omega t + G_2 \ I_{Bm} \cos^2 \omega t + G_3 \ I_{Bm} \cos^3 \omega t + G_4 \ I_{Bm} \cos^4 \omega t$$

Substituting $\cos^2 \omega t$, $\cos^3 \omega t$ and $\cos^4 \omega t$ and doing trigonometric operations, we get,

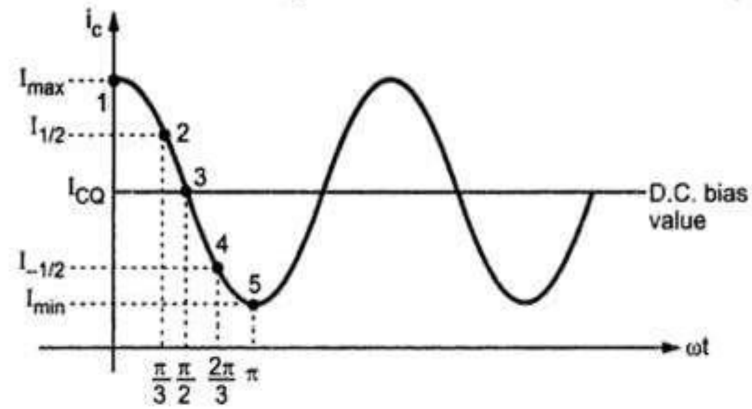
$$i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t \qquad \text{... (20)}$$

The equation shows that there are harmonics upto 4 th order. The collector current waveform and the various instants to be considered for higher order harmonic distortion calculation, are shown in the Fig. 5.24.

Figure 5.24

Output current waveform

The total collector current including d.c. bias can be written as,



$$i_c = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t \qquad \dots (21)$$

where $(I_{CQ} + B_0)$ is the d.c. component.

B_1, B_2, B_3 and B_4 are the amplitudes of the fundamental component, second, third and fourth harmonic components respectively.

Consider the five instants as shown in the Fig. 5.24 .

At point 1, $\omega t = 0$, $i_c = I_{max}$

$$\therefore \quad I_{max} = I_{CQ} + B_0 + B_1 + B_2 + B_3 + B_4 \qquad \dots (22)$$

At point 2, $\omega t = \pi/3$, $i_c = I_{1/2}$

$$\therefore \quad I_{1/2} = I_{CQ} + B_0 + 0.5B_1 - 0.5B_2 - B_3 - 0.5B_4 \qquad \dots (23)$$

At point 3, $\omega t = \frac{\pi}{2}$, $i_c = I_{CQ}$

$$\therefore \quad I_{CQ} = I_{CQ} + B_0 - B_2 + B_4 \qquad \dots (24)$$

At point 4, $\omega t = \frac{2\pi}{3}$, $i_c = I_{-1/2}$

$$\therefore \quad I_{-1/2} = I_{CQ} + B_0 - 0.5B_1 - 0.5B_2 + B_3 - 0.5B_4 \qquad \dots (25)$$

At point 5, $\omega t = \pi$, $i_c = I_{min}$

$$\therefore \quad I_{min} = I_{CQ} + B_0 - B_1 + B_2 - B_3 + B_4 \qquad \dots (26)$$

Solving the above five equations from (21) to (26) simultaneously, for the values of B_0, B_1, B_2, B_3 and B_4 we get,

$$B_0 = \frac{1}{6}[I_{max} + 2\ I_{1/2} + 2\ I_{-1/2} + I_{min}] \quad \text{... (27)}$$

$$B_1 = \frac{1}{3}[I_{max} + I_{1/2} - I_{-1/2} - I_{min}] \quad \text{... (28)}$$

$$B_2 = \frac{1}{4}[I_{max} - 2\ I_{CQ} + I_{min}] \quad \text{... (29)}$$

$$B_3 = \frac{1}{6}[I_{max} - 2\ I_{1/2} + 2\ I_{-1/2} - I_{min}] \quad \text{... (30)}$$

$$B_4 = \frac{1}{12}[I_{max} - 4\ I_{1/2} + 6\ I_{CQ} - 4\ I_{-1/2} + I_{min}] \quad \text{... (31)}$$

Hence the harmonic distortion coefficients can be obtained as,

$$D_n = \frac{|B_n|}{|B_1|} \quad \text{... refer equation (1)}$$

As the method uses five points on the output waveform to obtain the amplitudes of the various orders of harmonics, the method is called **'Five Point Method'** of determining the higher order harmonic distortion.

5.9.6 Power Output Due to Distortion

Now $P_{ac} = \frac{1}{2} B_1^2 R_L$ ... refer equation (17)

Hence the output power with harmonic distortion is,

$$(P_{ac})_D = \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + ... + \frac{1}{2} B_n^2 R_L$$

$$= \frac{1}{2} B_1^2 R_L \left[1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + ... + \frac{B_n^2}{B_1^2} \right]$$

$$\therefore \quad (P_{ac})_D = P_{ac}[1 + D_2^2 + D_3^2 + \cdots + D_n^2] \quad \text{... (32)}$$

But $D^2 = D_2^2 + D_3^2 + ... + D_n^2$ ... refer equation (2)

where D = Total Harmonic Distortion

$$\therefore \quad \boxed{(P_{ac})_D = P_{ac}(1 + D^2)} \quad \text{... (33)}$$

If the total harmonic distortion is 15% i.e. $D = 0.15$

then $(P_{ac})_D = P_{ac}[1 + (0.15)^2] = 1.0225\ P_{ac}$

So there is 2.25% increase in the power given to the load.

5.10 Analysis of Class B Amplifiers

As stated earlier, for class B operation, the quiescent operating point is located on the X-axis itself. Due to this collector current flows only for a half cycle for a full cycle of the input signal. Hence the output signal is distorted. To get a full cycle across the load, a pair of transistors is used in class-B operation. The two transistors conduct in alternate half cycles of the input signal and a full cycle across the load is obtained. The two transistors are identical in characteristics and called matched transistors.

Depending upon the types of the two transistors whether p-n-p or n-p-n, the two circuit configurations of class B amplifier are possible. These are,

1. When both the transistors are of same type i.e. either n-p-n or p-n-p then the circuit is called **push-pull class B** A.F. power amplifier circuit.
2. When the two transistors form a complementary pair i.e. one n-p-n and other p-n-p then the circuit is called **complementary symmetry class B** A.F. power amplifier circuit. Let us analyse these two circuits of class B amplifiers in detail.

5.11 Push Pull Class B Amplifier

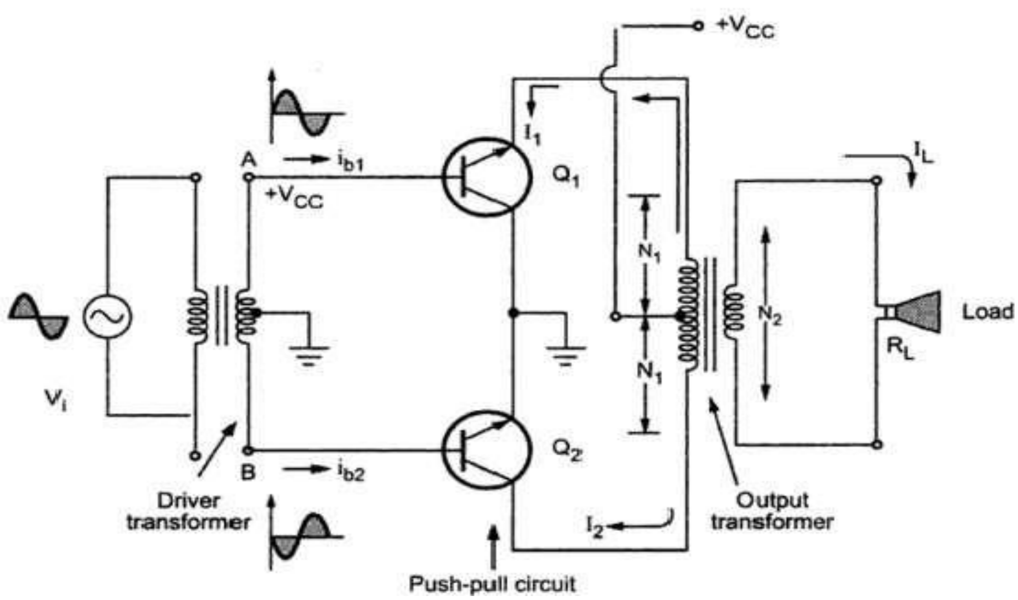
The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer**. The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 5.25.

In the circuit, both Q_1 and Q_2 transistors are of n-p-n type. The circuit can use both Q_1 and Q_2 of p-n-p type. In such a case, the only change is that the supply voltage must be $-V_{CC}$, the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage + V_{CC}.

Figure 5.25

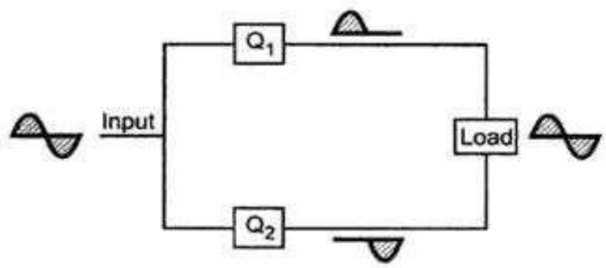
Push pull class B amplifier



With respect to the centre tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q_1 and Q_2 will be 180° out of phase.

▶ **Figure 5.26**

Basic push pull operation



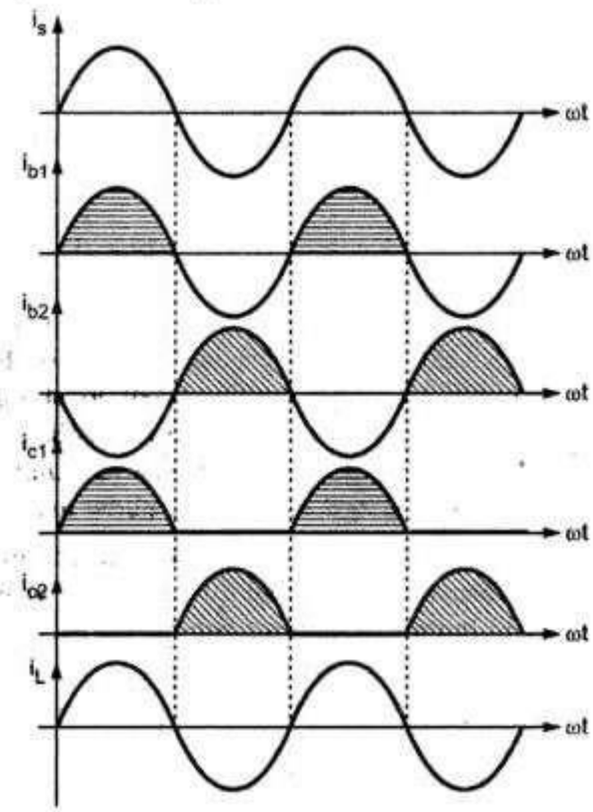
The transistor Q_1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q_2 conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 5.26.

When point A is positive, the transistor Q_1 gets driven into an active region while the transistor Q_2 is in cut off region. While when point A is negative, the point B is positive, hence the transistor Q_2 gets driven into an active region while the transistor Q_1 is in cut off region.

The waveforms of the input current, base currents, collector currents and the load current are shown in the Fig. 5.27.

▶ **Figure 5.27**

Waveforms for push pull class B amplifier



Key Point: *For the output transformer, the number of the turns of each half of the primary is N_1 while the number of the turns on the secondary is N_2. Hence the total number of primary turns is $2N_1$. So turns ratio of the output transformer is specified as $2N_1$. So turns ratio of the output transformer is specified as $2N_1 : N_2$.*

5.11.1 D.C.Operation

The d.c. biasing point i.e. Q point is adjusted on the X-axis such that $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. Hence the co-ordinates of the Q point are (V_{CC}, 0). There is no d.c. base bias voltage.

5.11.2 D.C.Power Input

Each transistor output is in the form of half rectified waveform. Hence if I_m is the peak value of the output current of each transistor, the d.c. or average value is $\frac{I_m}{\pi}$, due to half rectified waveform. **The two currents, drawn by the two transistors, form the d.c. supply are in the same direction. Hence the total d.c. or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.**

$$\therefore \quad \boxed{I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2\,I_m}{\pi}} \qquad \dots (1)$$

The total d.c. power input is given by,

$$P_{DC} = V_{CC} \times I_{dc}$$

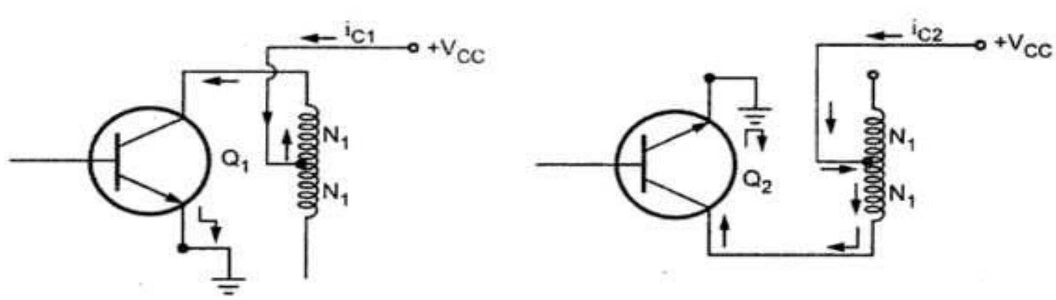
$$\therefore \quad \boxed{P_{DC} = \frac{2}{\pi} V_{CC} \; I_m} \qquad \dots (2)$$

5.11.3 A.C.Operation

When the a.c. signal is applied to the driver transformer, for positive half cycle Q_1 conducts. The path of the current drawn by the Q_1 is shown in the Fig. 5.28.

For the negative half cycle Q_2 conducts. The path of the current drawn by the Q_2 is shown in the Fig. 5.28 (b).

► **Figure 5.28**



(a) Q_1 conduction (b) Q_2 conduction

It can be seen that when Q_1 conducts, lower half of the primary of the output transformer does not carry any current. Hence only N_1 number of turns carry the current. While when Q_2 conducts, upper half of the primary does not carry any current. Hence again only N_1 number of turns carry the current. Hence the reflected load on the primary can be written as,

$$\therefore \boxed{R_L' = \frac{R_L}{n^2}} \qquad \dots (3)$$

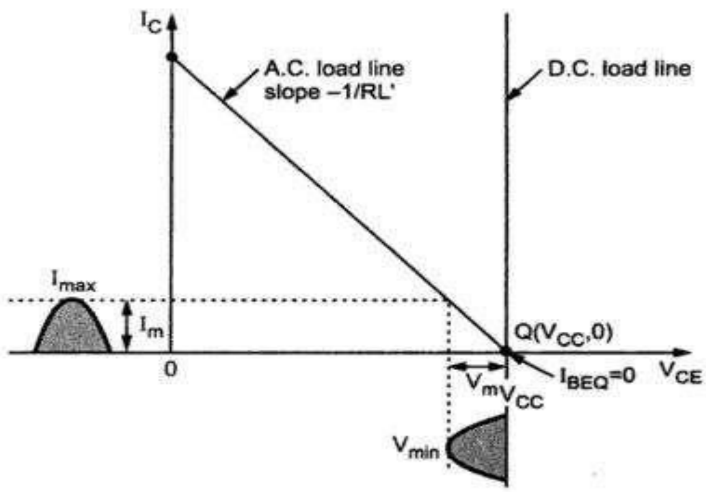
where $\quad n = \frac{N_2}{N_1}$

It is important to note that the step down turns ratio is $2N_1 : N_2$ but while calculating the reflected load, the ratio n becomes N_2/N_1. So each transistor shares equal load which is the reflected load R_L' given by the equation (3).

The slope of the a.c. load line is $-1/R_L'$ while the d.c. load line is the vertical line passing through the operating point Q on the x-axis. The load lines are shown in the Fig. 5.29.

▶ Figure 5.29

Load lines for push pull class B amplifier



The slope of the a.c. load line (magnitude of slope) can be represented in terms of V_m and I_m as,

$$\frac{1}{R_L'} = \frac{I_m}{V_m}$$

$$\therefore \boxed{R_L' = \frac{V_m}{I_m}} \qquad \dots (4)$$

where $\quad I_m$ = Peak value of the collector current

5.11.4 A.C. Power Output

As I_m and V_m are the peak values of the output current and the output voltage respectively, then

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

and $\quad I_{rms} = \frac{I_m}{\sqrt{2}}$

Hence the a.c. power output is expressed as,

$$P_{ac} = V_{rms} \; I_{rms} = I_{rms}^2 \; R_L' = \frac{V_{rms}^2}{R_L'} \qquad \dots (5)$$

While using peak values it can be expressed as,

$$\therefore \quad P_{ac} = \frac{V_m I_m}{2} = \frac{I_m^2 R_L'}{2} = \frac{V_m^2}{2R_L'} \quad \dots (6)$$

5.11.5 Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation.

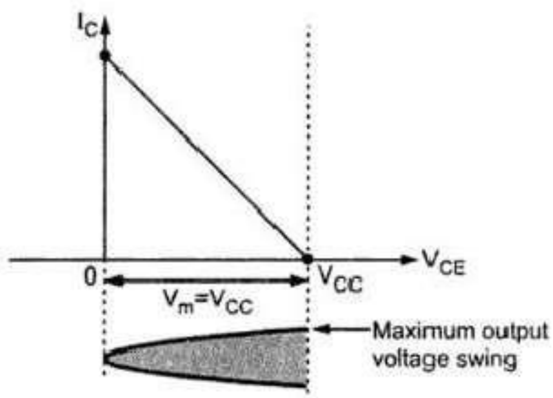
$$\%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left(\frac{V_m I_m}{2}\right)}{\frac{2}{\pi} V_{CC} I_m} \times 100$$

$$\therefore \quad \%\eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100 \quad \dots (7)$$

5.11.6 Maximum Efficiency

From the equation (7), it is clear that as the peak value of the collector voltage V_m increases, the efficiency increases. The maximum value of V_m possible is equal to V_{CC} as shown in the Fig. 5.30.

▶ **Figure 5.30**



$V_m = V_{CC}$ for maximum η

$$\therefore \% \eta_{max} = \frac{\pi}{4} \times \frac{V_{CC}}{V_{CC}} \times 100$$

$$= 78.5 \%$$

Key Point: *Thus the maximum possible theoretical efficiency in case of push pull class B amplifier is 78.5% which is much higher than the transformer coupled class A amplifier.*

For practical circuits it is upto 65 to 70%.

Key Point: *Practically the collector-emitter voltage of transistor is neglected as small. But if $V_{CE(min)}$ is given then maximum collector voltage V_m reduces by $V_{CE(min)}$ and becomes $V_m = V_{CC} - V_{CE(min)}$ under maximum efficiency condition.*

5.11.7 Power Dissipation

The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$\therefore P_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC} I_m - \frac{V_m I_m}{2}$$

$$\therefore\ P_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R'_L} - \frac{V_m^2}{2R'_L} \quad \text{... (8)}$$

Let us find out the condition for maximum power dissipation. In case of class A amplifier, it is maximum when no input signal is there. But in class B operation, when the input signal is zero, $V_m = 0$ hence the power dissipation is zero and not the maximum.

Maximum power dissipation : The condition for maximum power dissipation can be obtained by differentiating the equation (8) with respect to V_m and equating it to zero.

$$\therefore\ \frac{dP_d}{dV_m} = \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{2V_m}{2R'_L} = 0$$

$$\therefore\ \frac{2}{\pi} \frac{V_{CC}}{R'_L} = \frac{V_m}{R'_L}$$

$$\boxed{V_m = \frac{2}{\pi} V_{CC}} \quad \text{... For maximum power dissipation} \quad \text{... (9)}$$

This is the **condition for maximum power dissipation**. Hence the maximum power dissipation is,

$$(P_d)_{max} = \frac{2}{\pi} V_{CC} \times \frac{2}{\pi} \frac{V_{CC}}{R'_L} - \frac{4}{\pi^2} \frac{V_{CC}^2}{2R'_L}$$

$$= \frac{4}{\pi^2} \frac{V_{CC}^2}{R'_L} - \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L}$$

$$\therefore\ \boxed{(P_d)_{max} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R'_L}} \quad \text{... (10)}$$

Key Point: *For maximum efficiency,* $V_m = V_{CC}$ *hence the power dissipation is not maximum when the efficiency is maximum. And when power dissipation is maximum, efficiency is not maximum.* ***So maximum efficiency and maximum power dissipation do not occur simultaneously,*** *in case of class B amplifiers.*

Now $\quad P_{ac} = \dfrac{V_m^2}{2R'_L}$

and $\quad V_m = V_{CC}$ is the maximum condition.

$$\text{Hence} (P_{ac})_{max} = \frac{V_{CC}^2}{2R'_L} \quad \text{... (11)}$$

$$\text{Now}\ (P_d)_{max} = \frac{2V_{CC}^2}{\pi^2 R'_L} = \frac{4}{\pi^2}\left(\frac{V_{CC}^2}{2R'_L}\right)$$

$$\therefore\ (P_d)_{max} = \frac{4}{\pi^2}(P_{ac})_{max} \quad \text{... (12)}$$

This much power is dissipated by both the transistors hence the maximum power dissipation per transistor is $(P_d)_{max} / 2$.

$$\therefore (P_d)_{max} \text{ per transistor} = \frac{\frac{4}{\pi^2}(P_{ac})_{max}}{2}$$

$$\boxed{\therefore (P_d)_{max} \text{ per transistor} = \frac{2}{\pi^2}(P_{ac})_{max}} \quad \ldots (13)$$

This is the **maximum power dissipation rating** of each transistor. For example, if 10 W maximum power is to be supplied to the load, then power dissipation rating of each transistor should be $\frac{2}{\pi^2} \times 10$ i.e. 2.02 W.

5.11.8 Harmonic Distortion

Let the base input currents are sinusoidal in nature and given by,

$$i_{b1} = I_{Bm} \cos \omega t \text{ and } i_{b2} = -I_{Bm} \cos \omega t$$

The negative sign indicates that both are 180° out of phase.

Due to nonlinear dynamic characteristics, the collector current of the two transistors can be expressed in terms of harmonic components as,

$$i_{c1} = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots \quad \ldots (14)$$

Now $\quad i_{b1} = -I_{Bm} \cos \omega t = I_{Bm} \cos(\omega t + \pi)$

Hence the collector current for the second transistor can be obtained by replacing ωt by $\omega t + \pi$, in the expression for i_{c1}.

$$\therefore i_{c2} = I_{CQ} + B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos 2(\omega t + \pi p) + \ldots$$

$$= I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \ldots \quad \ldots (15)$$

Now the load current is the difference between the two. This is because, in the primary of the transformer the two currents are in opposite direction.

$$\therefore i_L = i_{c1} - i_{c2}$$

$$= (I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots)$$

$$-(I_{CQ} + B_0 - B_1 \cos \omega t + B_2 \cos 2\omega t - B_3 \cos 3\omega t + \ldots)$$

$$\boxed{\therefore i_L = 2B_1 \cos \omega t + 2B_3 \cos 3\omega t + \ldots} \quad \ldots (16)$$

It can be seen that **the even harmonic components 2nd, 4th, 6th and so on, get eliminated. Similarly the d.c. component also gets eliminated**. Hence the total distortion is less and as d.c. component flowing is zero, there is no possibility of d.c. saturation of the core. Hence the percentage harmonic distortion is only due to odd harmonics given by,

$$\% D_3 = \frac{|B_3|}{|B_1|} \times 100, \; \% D_5 = \frac{|B_5|}{|B_1|} \times 100 \; \ldots$$

Hence the total harmonic distortion is,

$$\boxed{\% D = \sqrt{D_3^2 + D_5^2 + D_7^2 + \ldots} \times 100} \quad \ldots (17)$$

This is based on the assumption that the two transistors are exactly matched. Otherwise even harmonics may be present in the output signal.

5.11.9 Advantages and Disadvantages

The advantages of push pull class B operation are :

1. The efficiency is much higher than the class A operation.
2. When there is no input signal, the power dissipation is zero.
3. The even harmonics get cancelled. This reduces the harmonic distortion.
4. As the d.c. current components flow in opposite direction through the primary winding, there is no possibility of d.c. saturation of the core.
5. Ripples present in supply voltage also get eliminated.
6. Due to the transformer, impedance matching is possible.

The disadvantages of the circuit are :

1. Two center tap transformers are necessary.
2. The transformers, make the circuit bulky and hence costlier.
3. Frequency response is poor.

Example 5.9 *A class B, push pull amplifier drives a load of 16 Ω, connected to the secondary of the ideal transformer. The supply voltage is 25 V. If the number of turns on the primary is 200 and the number of turns on the secondary is 50, calculate maximum power output, d.c. power input, efficiency and maximum power dissipation per transistor.*

Solution : $R_L = 16\ \Omega \qquad V_{CC} = 25\ V$

Now $2N_1 = 200 \quad N_2 = 50$

$$\therefore \quad N_1 = 100$$

$$\therefore \quad n = \frac{N_2}{N_1} = \frac{50}{100} = 0.5$$

$$\therefore \quad R'_L = \frac{R_L}{n^2} = \frac{16}{(0.5)^2}$$

$$= 64\ \Omega$$

For maximum power output, $V_m = V_{CC}$

i) $$(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R'_L} = \frac{1}{2} \times \frac{(25)^2}{64}$$

$$= 4.8828\ W$$

ii) $$P_{dc} = \frac{2}{\pi} V_{CC}\, I_m$$

Now $$\frac{V_m}{I_m} = R'_L$$

and $$V_m = V_{CC}$$ ... refer equation (4)

$$\therefore \quad I_m = \frac{V_{CC}}{R'_L} = \frac{25}{64} = 0.3906\ A$$

$$\therefore \quad P_{DC} = \frac{2}{\pi} \times 25 \times 0.3906$$

$$= 6.2169\ W$$

iii) $$\%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{4.8828}{6.2169} \times 100$$

$$= 78.5\%$$

5.12 Complementary Symmetry Class B Amplifier

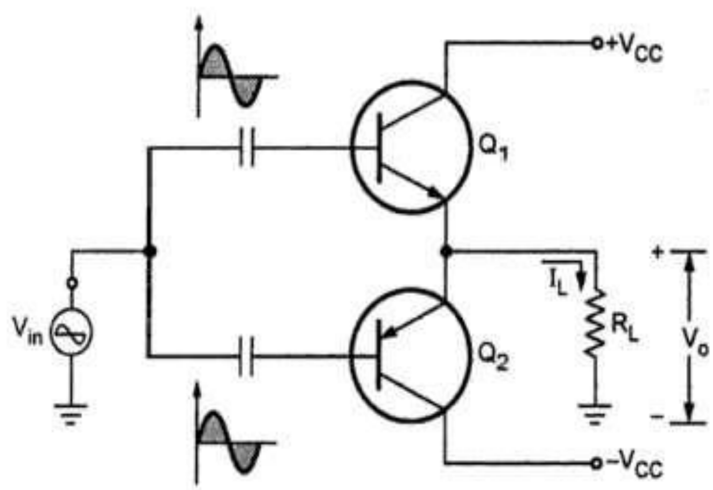
As stated earlier, instead of using same type of transistors (n-p-n or p-n-p), one n-p-n and other p-n-p is used, the amplifier circuit is called as complementary symmetry class B amplifier. This circuit is transformer less circuit. But with common emitter configuration, it becomes difficult to match the output impedance for maximum power transfer without an output transformers. Hence the matched pair of complementary transistors are used in common collector (emitter follower) configuration, in this circuit.

Key Point: *This is because common collector configuration has lowest output impedance and hence the impedance matching is possible.*

In addition, voltage feedback can be used to reduce the output impedance for matching.

▶ **Figure 5.32**

Complementary symmetry class B amplifier



The basic circuit of complementary symmetry class-B amplifier is shown in the Fig. 5.32.

The circuit is driven from a dual supply of $\pm V_{CC}$. The transistor Q_1 is n-p-n while Q_2 is of p-n-p type.

In the positive half cycle of the input signal, the transistor Q_1 gets driven into active region and starts conducting. The same signal gets applied to the base of the Q_2 but as it is of complementary type, remains in off condition, during positive half cycle. This results into positive half cycle across the load R_L. This is shown in the Fig. 5.33.

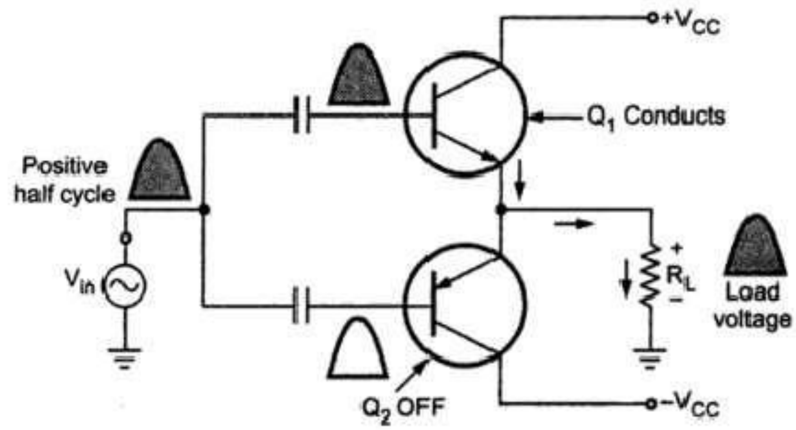
iv) $(P_d)_{max} = \frac{2}{\pi^2} \times (P_{ac})_{max}$ for each transistor

$$= \frac{2}{\pi^2} \times 4.8828$$

$$= 0.9894 \text{ W} = 1 \text{ W}$$

▶ **Figure 5.33**

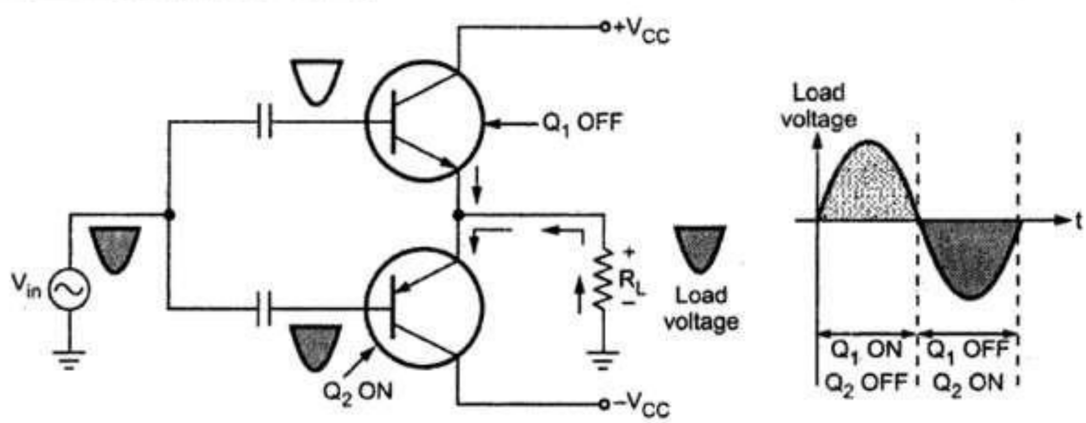
Positive half cycle operation



During the negative half cycle of the signal, the transistor Q_2 being p-n-p gets biased into conduction. While the transistor Q_1 gets driven into cut off region. Hence only Q_2 conducts during negative half cycle of the input, producing negative half cycle across the load R_L, as shown in the Fig. 5.34 (a).

Thus for a complete cycle of input, a complete cycle of output signal is developed across the load as shown in the Fig. 5.34 (b)

▶ **Figure 5.34**



(a) Negative half cycle operation **(b) Load voltage waveform**

5.12.1 Mathematical Analysis

All the results derived for push pull transformer coupled class B amplifier are applicable to the complementary class B amplifier. The **only change is that as the output transformer is not present, hence in the expressions, R_L value must be used as it is, instead of R'_L.**

5.12.2 Advantages and Disadvantages

The advantages are :

1. As the circuit is transformerless, its weight, size and cost are less.
2. Due to common collector configuration, impedance matching is possible.
3. The frequency response improves due to transformerless class B amplifier circuit.

The disadvantages are :

1. The circuit needs two separate voltage supplies.
2. The output is distorted to cross-over distortion.

Key Point : *While solving the problems on class B large signal amplifiers, given power is to be assumed maximum unless and otherwise specified and use* $(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L}$ *or* $\frac{1}{2}\frac{V_{CC}^2}{R_L'}$ *depending upon type of the circuit.*

If V_{in} *is given then as common collector circuit has unity gain,* $V_{out} = V_{in}$ *and then voltage across* R_L *is same as* V_{in}. *The peak value of* V_{in} *is* V_m *and* $V_m \neq V_{CC}$ *in such a case.*

If supply given is dual such as $V_{CC} = \pm 12$ V, ± 20 V *etc. , it is dual supply version.*

But if supply given is $V_{CC} = 12$ V, 20 V *then it is single supply version and in such a case use* $V_{CC} = \frac{1}{2}$ *(given +* V_{CC} *) i.e* $\frac{12}{2} = 6$ V, $\frac{20}{2} = 10$ V *etc. The single supply version is discussed in the section 5.16.*

5.13 Comparison of Push Pull and Complementary Symmetry Circuits

▶ **Table 5.2**

	Push Pull Class B	Complementary Symmetry Class B
1.	Both the transistors are similar either pnp or npn.	Transistors are complementary type i.e. one npn other pnp.
2.	The transformer is used to connect the load as well as input.	The circuit is transformerless.
3.	The impedance matching is possible due to the output transformer.	The impedance matching is possible due to common collector circuit.
4.	Frequency response is poor.	Frequency response is improved.
5.	Due to transformers, the circuit is bulky, costly and heavier.	As transformerless, the circuit is not bulky and costly.
6.	Dual power supply is not required.	Dual power supply is required.
7.	Efficiency is higher than class A.	The efficiency is higher than the push pull.

5.14 Cross-Over Distortion

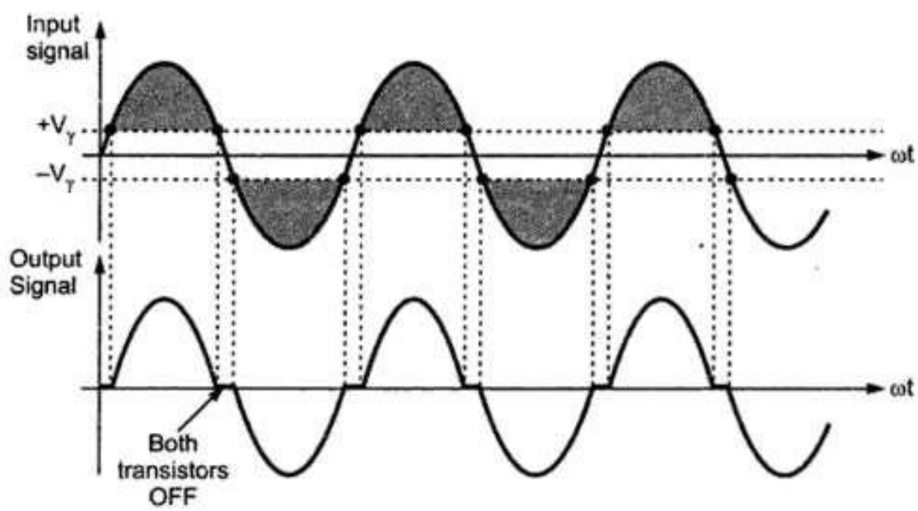
For a transistor to be in active region the base emitter junction must be forward biased. The junction cannot be made forward biased till the voltage applied becomes greater than cut-in voltage (V_γ) of the junction, which is generally 0.7 V for silicon and 0.2V for germanium transistors. Hence as long as the magnitude of the input signal is less than the cut in voltage of the base emitter junction, the collector current remain zero and transistor remains in cut-off region,

Hence there is a period between the crossing of the half cycles of the input signal, for which none of the transistors is active and the output is zero. Hence the nature of the output signal gets distorted and no longer remains same as that of input. Such a distorted output wave form due to cut-in voltage is shown in the Fig. 5.36.

Such a distortion in the output signal is called a **cross-over distortion**. Due to cross-over distortion each transistor conducts for less than a half cycle rather than the complete half cycle. The part of the input cycles for which the two transistors conduct alternately is shown shaded in the Fig. 5.36. The cross-over distortion is common in both the types of class B amplifiers.

▶ **Figure 5.36**

Cross-over distortion



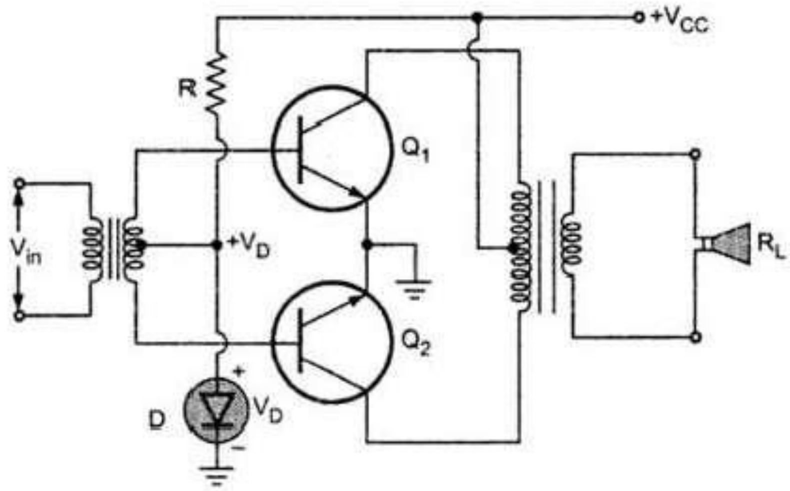
5.15 Elimination of Cross-Over Distortion

To eliminate the cross-over distortion some modifications are necessary, in the basic circuits of the class B amplifiers. The basic reason for the cross over distortion is the cut in voltage of the transistor junction. To overcome this cut-in voltage, a small forward biased is applied to the transistors. Let us see the practical circuits used to apply such forward biased, in the two types of class B amplifiers.

5.15.1 Push Pull Class B Amplifier

► **Figure 5.37**

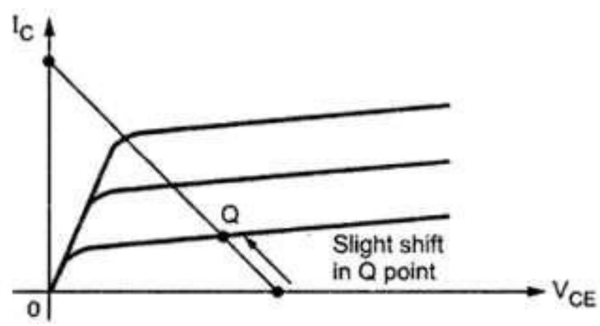
Use of Diode



The forward biased across the base-emitter junction of each transistor is provided by using a diode as shown in the Fig. 5.37.

The drop across the diode D is equal to the cut-in voltage of the base-emitter junction of the transistor. Hence both the transistors conduct for full half cycle, eliminating the cross-over distortion.

► **Figure 5.38**



Due to the forward biased provided to eliminate the cross over distortion, the Q point shifts upwards on the load line as shown in the Fig. 5.38. Hence the operation of the amplifier no longer remains class-B but becomes class AB operation.

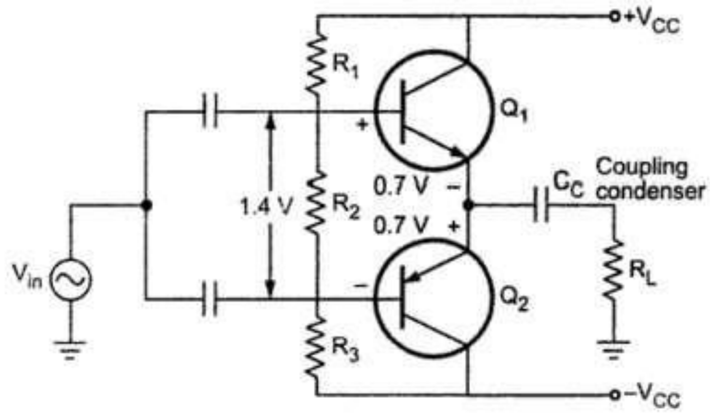
But as the amplifier handles the large signals in the range of volts, compared to these signals the shift in Q point is negligibly small.

Key Point: *For all the practical purposes, the operation is treated as class B operation and all the expression derived are applicable to these modified circuits.*

5.15.2 Complementary Symmetry Class B Amplifier

▶ **Figure 5.39**

Use of potential divider

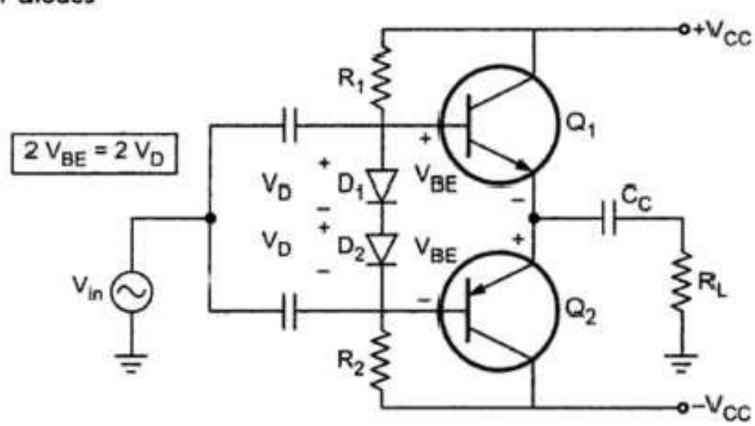


In push pull, transformer coupled type, the drop across forward biased one diode is sufficient, to provide necessary cut in voltage. But in case of complementary symmetry circuit, base emitter junctions of both Q_1 and Q_2, are required to provide a fixed bias. Hence for silicon transistors a fixed bias of 0.7 + 0.7 = 1.4 V is required. This can be achieved by using a potential divider arrangement as shown in the Fig. 5.39.

But in this circuit, the fixed bias provided is fixed equal to say 1.4 V. While the junction cut-in voltage changes with respect to the temperature. Hence there is still possibility of a distortion when there is temperature change. Hence instead of R_2, the two diodes can be used to provide the required fixed bias. As the temperature changes, along with the junction characteristics, the diode characteristics get changed and maintain the necessary biasing required to overcome the cross-over distortion when there is temperature change. The arrangement of the circuit with the two diodes is shown in the Fig. 5.40.

▶ **Figure 5.40**

Use of pair of diodes

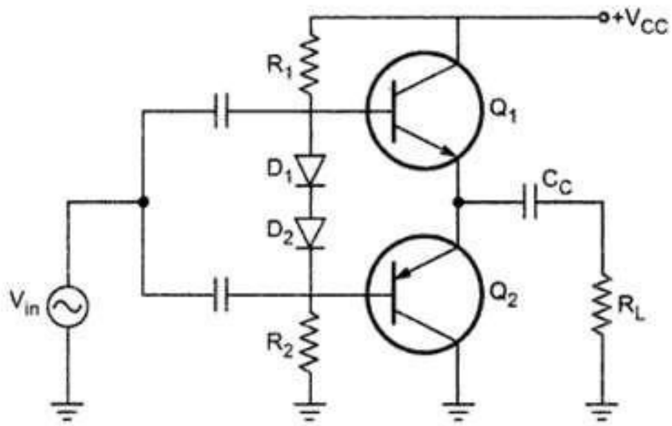


5.16 Complementary Symmetry Single Supply Version

The main disadvantage as seen earlier of complementary amplifier is the use of dual supply. But in practice the circuit can be modified by grounding – V_{CC} terminal. The resulting circuit is called single supply version of complementary symmetry class B amplifier as shown in the Fig. 5.41.

▶ **Figure 5.41**

Single supply version of complementary symmetry class B amplifier



Key Point: *All the expression derived for dual supply version are still applicable to single supply version.* ***Only change required is that the value of V_{CC} must be taken as $V_{CC}/2$, while calculating the various parameters of the circuit.***

7.20 Heat Sink for Power Transistors

The maximum power handled by a particular power transistor and the temperature of the transistor junctions are closely related. This is because of the fact that the junction temperature increases due to the power dissipation. The collector dissipation can be obtained as

$$P_d = V_{CE} I_C$$

Let T_J be the junction temperature which due to power dissipation. Manufacture provides the maximum permissible value of T_J and corresponding maximum available value of the power dissipation P_d. If the temperature keeps on increasing, at a certain temperature, the crystalline structure is destroyed and there is no chance of recovery. The lower limit of a semiconductor is taken as,

$$\boxed{-65°C \leq T_J \leq (T_J)_{max}} \quad \ldots(1)$$

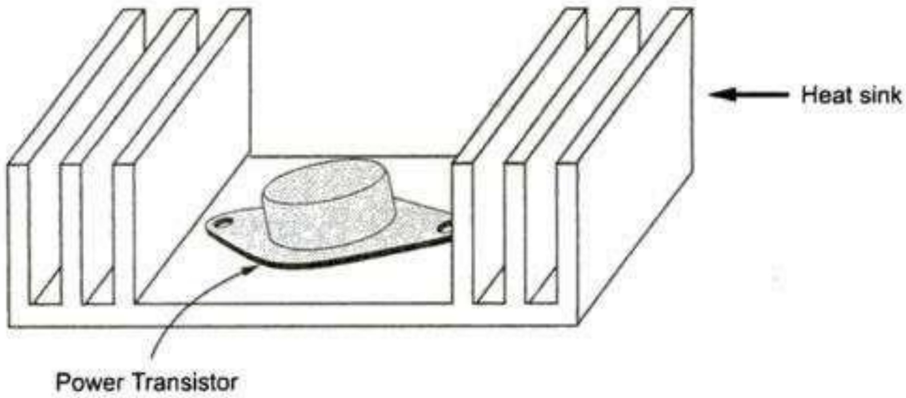
Where $(T_J)_{max}$ is specified by the manufacturers.

Thus practically it is necessary to keep the junction temperature less than $(T_J)_{max}$ specified for the power transistor used in the power amplifier.

Key Point: *A heat sink is a mechanical device which is connected or press fit to the case of the transistor that provides a large surface area, to dissipate the developed heat. The heat sink carries the heat to the surroundings.*

The heat sink draws heat from the power transistor via thermal condition and expels the heat into the ambient air via thermal convection and heat radiation. The Fig. 7.46 shows a power transistor with a heat sink.

▶ **Figure 7.46**



If the heat developed is transformed to the surroundings instantaneously, the collector dissipation rating would be infinite. But in practice such ideal situation is not possible due to thermal lag.

The important advantages of heat sink are,

1. The temperature of the case gets lowered.
2. The power handling capacity of the transistors can approach the rated maximum value.

7.22.1 Types of Heat Sinks

The various standard shapes and sizes of the heat sink are shown in the Fig. 7.69. The heat sinks shown in (a) and (b) are called natural convection coolers while shown in (c), (d) and (e) are typical shape-on dissipators for various case sizes.

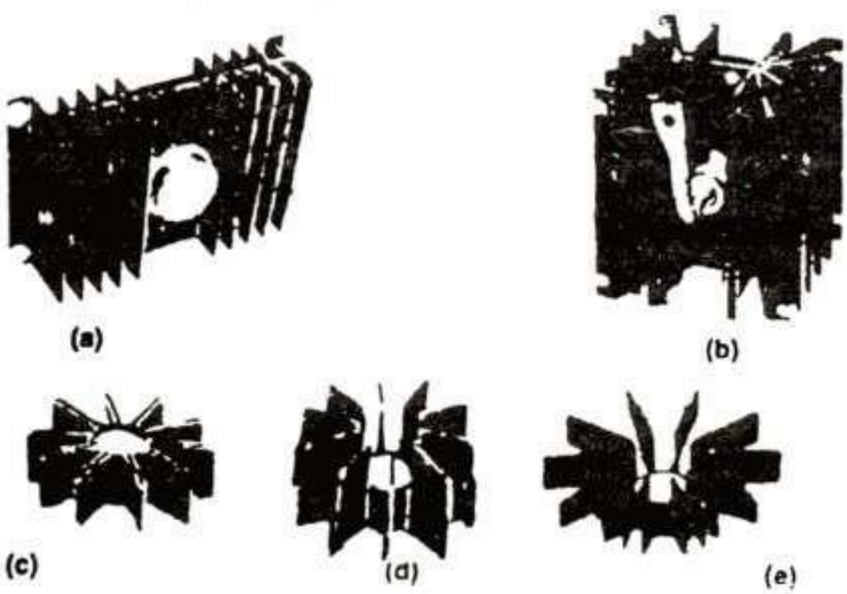


Fig. 7.69 Typical heat sinks

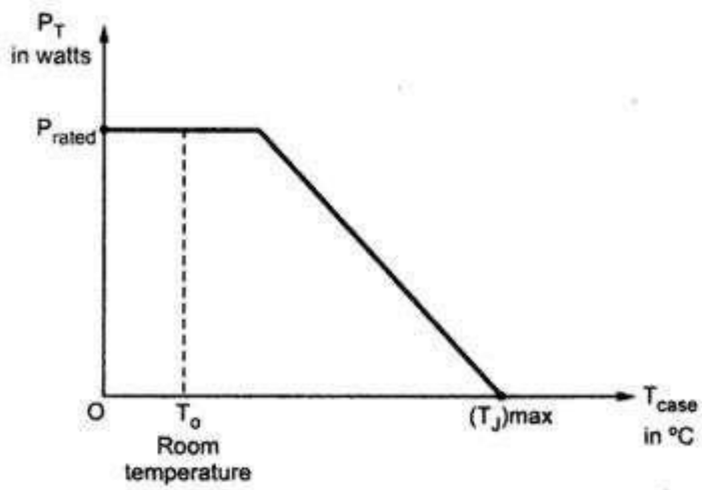
7.22.2 Derating of Power Transistor

If heat sink is ideal, the power transistor can be operated at its maximum rated power handling capacity. But practically as junction temperature increases the power handling capacity of the transistor decreases. Thus it is necessary to **derate** the power handling capacity of the power transistor as a function of the case temperature. Such a derating is possible by providing a **derating curve** for the transistor. Such a derating curve is provided by the manufacturer. The Fig. 7.70 shows a typical derating curve for a power transistor, which is a plot of P_T against T_{case}. The P_T is the maximum total power dissipation and T_{case} is the case temperature.

The safe electrical power that device can handle when case temperature is equal to room temperature T_0 is called **rated power handling capacity** (P_{rated}). Usually room temperature is 25 °C. The temperature at which the derating curve crosses the horizontal axis is called **maximum allowable junction temperature** $(T_J)_{max}$. If T_{case} increases beyond $(T_J)_{max}$, the transistor gets damaged.

Figure 7.48

Typical power transistor derating curve



In some cases, instead of derating curve, a **derating factor** is specified and rated power handling capacity at T_0 is specified. From this data, power handling capacity at any other temperature can be obtained as,

$$P_d(T_1) = P_d(T_0) - (T_1 - T_0)\ (\text{derating factor}) \qquad \dots (2)$$

where $P_d(T_0)$ = Rated power handling capacity at T_0

$P_d(T_1)$ = Power handling capacity at T_1

The derating factor is expressed in the units, watts/degree of temperature or milliwatts/degree of temperature.

7.20.3 Thermal Analogy of Power Transistors

The heat dissipation problem is very much analogous to a simple electric circuit and the Ohm's law. An electric current flows when there exists a potential difference while the heat flows when there exists a temperature difference $(T_2 - T_1)$. Then similar to a electric resistance a thermal resistance can be obtained as, Now tu develop the thermal-electyiC analogy let ur define some parameters .as,

T -)uncGcm Temperalune

Th = Case Temperahire

T = Ambient Temperature

= Total thermal resistance

(junction to ambient)

= Transistor thetmaT his(ance

(juncEon to case)

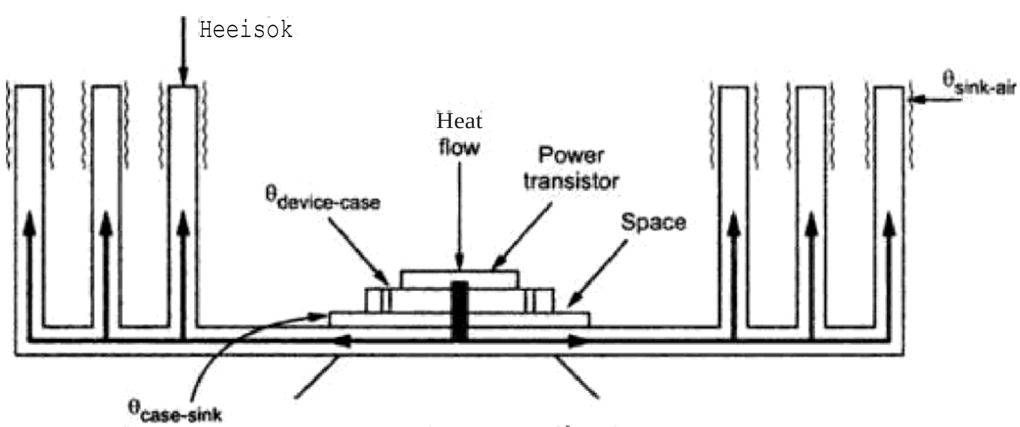
= Irtsu\ator thermal zesisfance

(case to heat .sink)

= bleat sink thermal resistance

(heat sink tu ambient)

The Fig. 7.49 shows e heat flow from a power transistor to ambient air x'ia a heat sink.



$$\theta = \frac{T \bullet - T}{P_d} \cdot C/W \text{ or } ^\circ C/mW \quad .(3)$$

YVbere Pd is the heat dLwip«trd nr heal How, due tri the power dissipation.

T re *m t* he above relation we cen write,

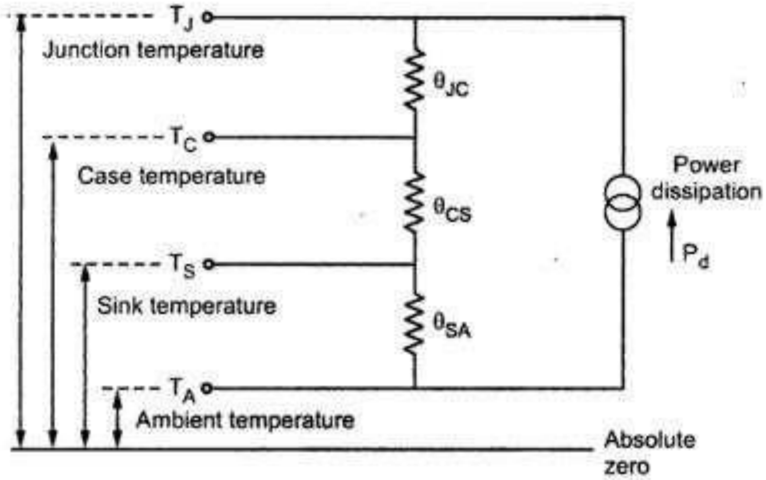
$$T_2 - T_1 \;\; \theta P_d \; ^\circ C \quad ..(4)$$

and P $\frac{T_2 - T_1}{}$ W or mW (5)

From this heat flow diagram, an electrical analogous circuit can be obtained as,

▶ Figure 7.50

Electrical analogous circuit



The electrical analogous circuit is a simple series circuit.

Key Point: *A special silicon grease is often used to establish good heat conducting path between the case and the heat sink. Hence the temperature of heat sink and case are considered different.*

Thus from the property of series circuit, the total thermal resistance can be obtained as,

$$\boxed{\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad ^\circ C/W} \qquad \dots (6)$$

But $$\theta_{JA} = \frac{T_J - T_A}{P_d} \qquad \text{... from definition of } \theta \text{ in equation (3)}$$

$\therefore$ $$\boxed{T_J = P_d\, \theta_{JA} + T_A} \qquad \dots (7)$$

Thus the total power handling capacity P_d of the device can be obtained as,

$$\boxed{P_d = \frac{T_J - T_A}{\theta_{JA}} = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}} \qquad \dots (8)$$

Similarly the temperatures of case and sink can be obtained from,

$$\theta_{CS} = \frac{T_C - T_S}{P_d} \qquad \dots (9)$$

$$\theta_{SA} = \frac{T_S - T_A}{P_d} \qquad \dots (10)$$

or $$\theta_{CS} + \theta_{SA} = \frac{T_C - T_A}{P_d} \qquad \dots (11)$$

7.20.4 Heat Sink Design

Manufacturers usually specify the total thermal resistance from the case to air i.e. θ_{CA} for heat sinks. From the electrical analogous circuit we can write,

$$\theta_{CA} = \theta_{CS} + \theta_{SA} = \theta_{JA} - \theta_{JC} \quad \dots (12)$$

where $$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad \dots (13)$$

For the given circuit, V_{CE} and I_C values are known hence power dissipation P_d can be obtained as,

$$P_d = V_{CE} I_C \quad \dots (14)$$

But $$\theta_{JA} = \frac{T_J - T_A}{P_d} \quad \dots (15)$$

Now the limiting junction temperature is T_J beyond which temperature of junction should not exceed is known. The air temperature T_A is known. Using (15), θ_{JA} can be obtained.

Thus from (12), θ_{CA} can be obtained as for the transistor θ_{JC} is known. As for various heat sinks θ_{CA} values are provided by the manufacturer, the proper heat sink with θ_{CA} less than that calculated in design should be selected.

➡ **Example 7.15 :** *Determine the junction, case and sink temperature for a power transistor if it carries $I_C = 1A$ at an average voltage of $V_{CE} = 10$ V. Assume $\theta_{JC} = 5$ °C/W, $\theta_{SA} = 4$ °C/W and $\theta_{CS} = 1$ °C/W.*

The ambient temperature is 25 °C.

Solution : $T_A = 25$ °C, $I_C = 1$ A, $V_{CE} = 10$ V

$$P_d = V_{CE} I_C = 10 \text{ W}$$

Now $$\theta_{SA} = \frac{T_S - T_A}{P_d}$$

$$\therefore \quad 4 = \frac{T_S - 25}{10}$$

$$\therefore \quad T_S = \mathbf{65\ °C} \quad \dots \text{Sink temperature}$$

$$\theta_{CS} = \frac{T_C - T_S}{P_d}$$

$$\therefore \quad 1 = \frac{T_C - 65}{10}$$

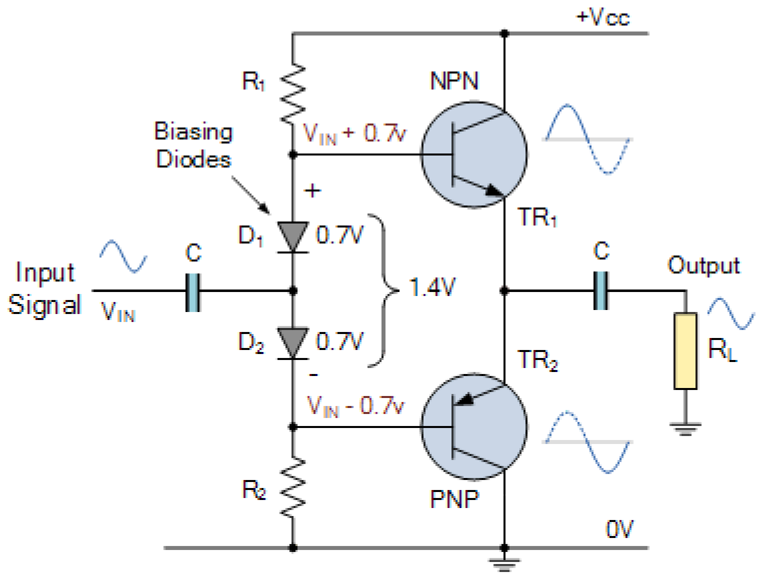
$$\therefore \quad T_C = \mathbf{75\ °C} \quad \dots \text{case temperature}$$

And $$\theta_{JA} = \frac{T_J - T_A}{P_d} \quad \text{and} \quad \theta_{JA} = \theta_{JC} + \theta_{SA} + \theta_{CS}$$

$$\therefore \quad (5 + 4 + 1) = \frac{T_J - 25}{10}$$

$$\therefore \quad T_J = \mathbf{125\ °C} \quad \dots \text{Junction temperature}$$

Class AB Power Amplifier:



In class AB power amplifiers, the biasing circuit is so adjusted that the operating point Q lies near the cut-off voltage. During a small portion of negative half cycle and for complete positive half cycle of the signal, the input circuit remains forward biased⁻and hence collector current flows. But during a small portion (less than half cycle) of the negative cycle"' the input circuit is reverse biased and, therefore, no collector current flows during this period. Class AB operation needs a push-pull connection to achieve a full output cycle.

One way to produce an amplifier with the high efficiency output of the Class B configuration along with the low distortion of the Class A configuration is to create an amplifier circuit which is a combination of the previous two classes resulting in a new type of amplifier circuit called a **Class AB Amplifier**. Then the Class AB amplifier output stage combines the advantages of the Class A amplifier and the Class B amplifier while minimising the problems problems of low efficiency and distortion associated with them.

As we said above, the *Class AB Amplifier* is a combination of Classes A and B in that for small power outputs the amplifier operates as a class A amplifier but changes to a class B amplifier for larger current outputs. This action is achieved by pre-biasing the two transistors in the amplifiers output stage. Then each transistor will conduct between $180^o$and 360^o of the time depending on the amount of current output and pre-biasing. Thus the amplifier output stage operates as a Class AB amplifier.

While the use of biasing resistors may not solve the temperature problem, one way to compensate for any temperature related variation in the base-emitter voltage, (V_{BE}) is to use a pair of normal forward biased diodes within the amplifiers biasing arrangement as shown.

UNIT V

TUNED AMPLIFIERS

To amplify the selective range of frequencies, the resistive load R_C is replaced by a tuned circuit. The tuned circuit is capable of amplifying a signal over a narrow band of frequencies centered at f_r. The amplifiers with such a tuned circuit as a load are known as tuned amplifier.

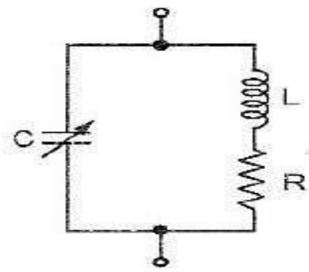


Fig. 3.1 Tuned circuit

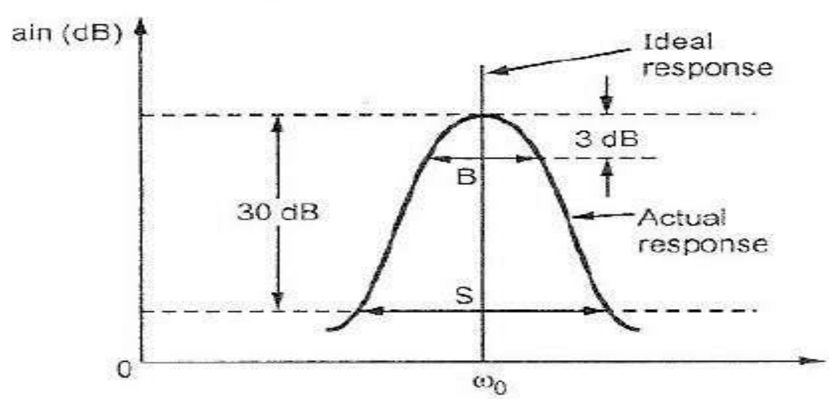


Fig. 3.2 Frequency response of a tuned amplifier

The Fig. 3.1 shows the tuned parallel LC circuit which resonates at a particular frequency. The resonance frequency and impedance of tuned circuit is given as,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad \ldots (1)$$

and

$$Z_r = \frac{L}{CR} \qquad \ldots (2)$$

The response of tuned amplifiers is maximum at resonant frequency and it falls sharply for frequencies below and above the resonant frequency, as shown in the Fig. 3.2. In the Fig. 3.2, 3 dB bandwidth is denoted as and 30dB bandwidth is denoted as S. The ratio of the 30dB bandwidth (S) to the 3 dB bandwidth (B) is known as Skirt selectivity.

At resonance, inductive and capacitive effects of tuned circuit cancel each other. As a result, circuit is like resistive and cos φ = 1 i.e. voltage and current are in phase. For frequencies above resonance, circuit is capacitive and for frequencies below resonance, circuit is inductive. Since tuned circuit is purely resistive at resonance it can be used as a load for amplifier.

Coil Losses:

As shown in the Fig. 3.1, the tuned circuit consists of a coil. Practically, coil is not purely inductive. It consists of few losses and they are represented in the form of leakage resistance in with the inductor. The total loss of the coil is comprised of copper loss, eddy current loss and hysteresis loss. The copper loss at low frequencies is equivalent to the d.c. resistance of the coil. Copper loss is inversely proportional to frequency. Therefore, as frequency increases, the copper loss decreases. Eddy current loss in iron and copper coil are due to currents flowing within the copper or core based by induction. The result of eddy currents is a loss due to heating within the inductors copper or core. Eddy current losses are directly proportional to frequency. Hysteresis loss is proportional to the area enclosed by the hysteresis loop and to the rate at which this loop is transversed. It is a function of signal level and increase with frequency. Hysteresis loss is however independent of frequency.

As mentioned earlier, the total losses in the coil or inductor is represented by inductance in series with leakage resistance of the coil. It is shown in the Fig.3.3

Q Factor:

Quality Factor (Q) is important characteristics of inductor. The Q is the ratio of reactance to resistance and therefore it is unitless. It is the measure of how 'pure' or 'real' an inductor is (i.e. the inductor consists only reactance). The higher the Q of an inductor, the fewer losses there are in the inductor. The Q factor also can be defined as the measure of efficiency with which inductor can store the energy. The dissipation factor (D) that can be referred to as the total loss within a component is defined as 1/Q. The fig. 3.4 shows the quality factor equations for series and parallel circuits and its relation with dissipation factor.

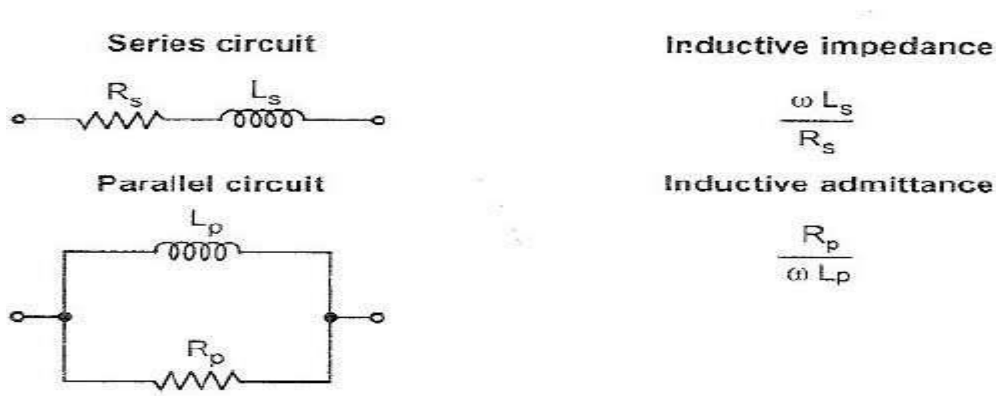


Fig. 3.4 Quality factor equations

$$\text{Quality factor equation } Q = \frac{1}{D} = \frac{\omega L_s}{R_s} = \frac{R_p}{\omega L_p}$$

Unloaded and Loaded Q:

Unloaded Q is the ratio of stored energy to dissipated energy in a reactor or resonator. The unloaded Q or Q_U, of an inductor or capacitor is X/R_S, where X represents the reactance and R_S represents the series resistance. The loaded Q or Q_L, of a resonator is determined by how

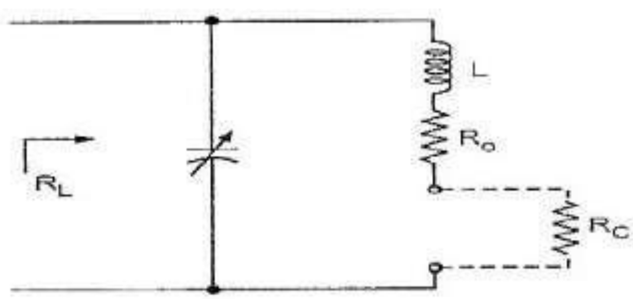


Fig. 3.5 Tuned load circuit

tightly the resonator is coupled to its terminations.

Let us consider the tuned load circuit as shown in the Fig. 3.5. Here, L and C represent tank circuit. The internal circuit losses of inductor are represented by R_o and R_C represents the coupled in load.

For this circuit we can write,

$$R_o = \frac{\omega_o L}{Q_U} \text{ and } R_C = \frac{\omega_o L}{Q_L}$$

where Q_U is unloaded Q and Q_L is loaded Q.

The circuit efficiency for the above tank circuit is given as,

$$\eta = \frac{I^2 R_C}{I^2 (R_C + R_o)} = \frac{Q_U}{Q_U + Q_L} \times 100 \%$$

From above equation, it can be easily realized that for high overall power efficiency, the coupled-in load R_C should be large in comparison to the internal circuit losses represented by R_o of the inductor.

The quality factor Q_L determines the 3 dB bandwidth for the resonant circuit. The 3 dB bandwidth for the resonant circuit is given as,

$$BW = \frac{f_r}{Q_L}$$

Where f_r represents the centre frequency of a resonator and BW represents the bandwidth.

If Q is large, bandwidth is small and circuit will be highly selective. For small Q values, bandwidth is high and selectivity of the circuit is lost, as shown in the Fig. 3.6.

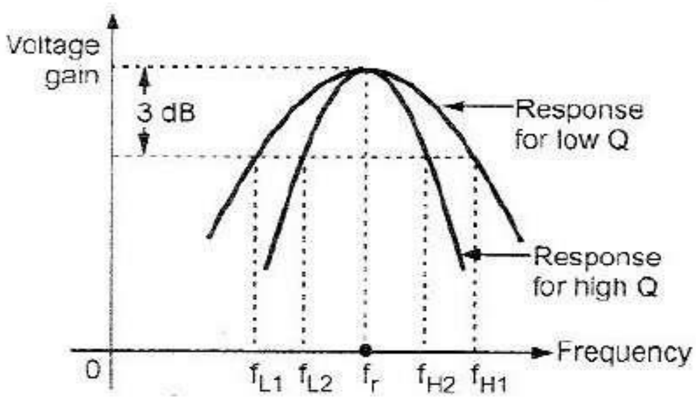


Fig. 3.6 Variation of 3dB bandwidth with variation in quality factor

Thus in tuned amplifier Q is kept as high as possible to get the better selectivity. Such tuned amplifiers are used in communication or broadcast receivers where it is necessary to amplify only selected band of frequencies.

Requirements of Tuned Amplifier:

The basic requirements of Tuned Amplifiers are:

1. The amplifier should provide selectivity of resonant frequency over a very narrow band.
2. The signal should be amplified equally well at all frequencies in the selected narrow band.
3. The tuned circuit should be so mounted that it can be easily tuned. If there is more than one circuit to be tuned, there should be an arrangement to tune all circuit simultaneously.
4. The amplifier must provide the simplicity in tuning of the amplifier components to the desired frequency over a considerable range of band of frequencies.

Classification of Tuned Amplifier:

We know that, multistage amplifiers are used to obtain large overall gain. The cascaded stages of multistage tuned amplifiers can be categorized as given below:

1. Single Tuned Amplifiers
2. Double Tuned Amplifiers
3. Stagger Tuned Amplifiers

These amplifiers are further classified according to coupling used to cascade the stages of multistage amplifier. They are,

1. Capacitive Coupled
2. Inductive Coupled
3. Transformer Coupled

Small Signal Tuned Amplifier:

A common emitter amplifier can be converted into a single tuned amplifier by including a parallel tuned circuit as shown in the Fig. 3.7. The biasing components are not shown for simplicity.

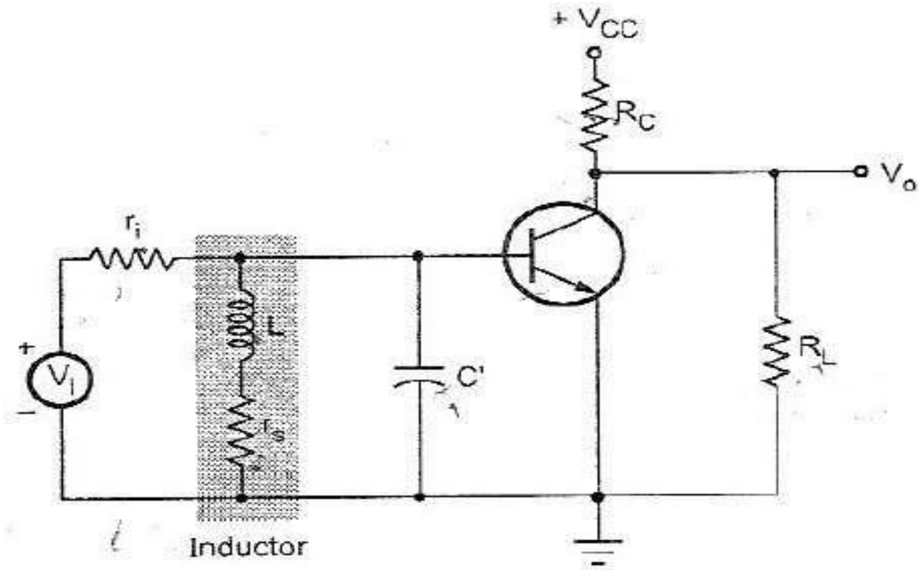


Fig. 3.7 Single tuned transistor amplifier

Before going to study the analysis of this amplifier, the practical assumptions to simplify the analysis are:

Assumptions:

1. $R_L << R_C$
2. $r_{bb'} = 0$

With these assumptions, the simplified equivalent circuit for a single tuned amplifier is shown in Fig 3.8.

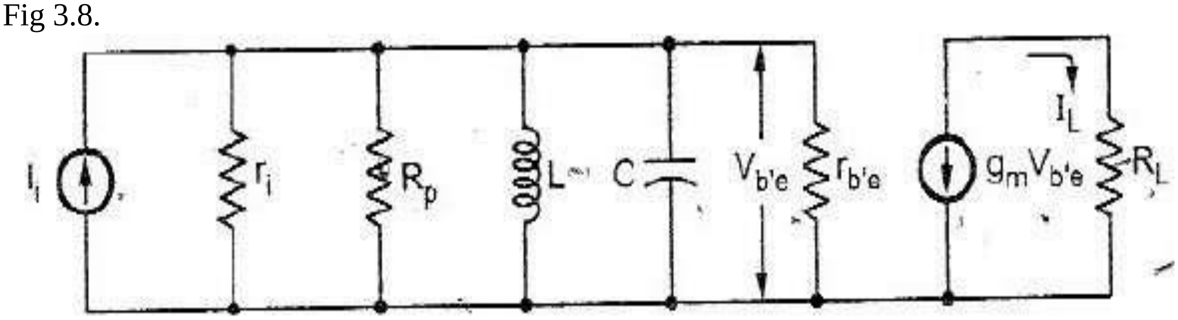


Fig. 3.8 Equivalent circuit of single tuned amplifier

Where $C_{eq} = C' + C_{b'e} + (1 + g_m R_L) C_{b'c}$ and C' is the external capacitance used to tune the circuit, $(1 + g_m R_L) C_{b'c}$ is the Miller Capacitance. r_s represents the losses in the coil. The series RL circuit in Fig. 3.7 is replaced by the equivalent RL circuit in Fig 3.8 assuming coil losses are low over the frequency band of interest, i.e. the coil Q is high.

$$\therefore \qquad \boxed{Q_c = \frac{\omega L}{r_c} >> 1}$$

The conditions for equivalence are most easily established by equating the admittances of the two circuits shown in the Fig. 3.9.

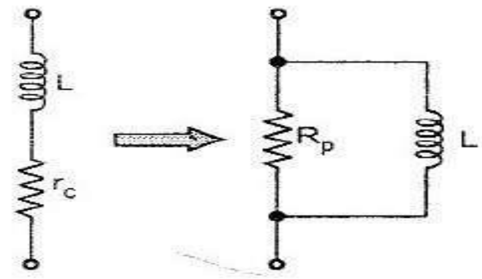


Fig. 3.9 Equivalent circuits

$$Y_1 = \frac{1}{r_c + j\omega L} = \frac{r_c - j\omega L}{r_c^2 + \omega^2 L^2}$$

$$\approx \frac{r_c}{r_c^2 + \omega^2 L^2} - \frac{j\omega L}{r_c^2 + \omega^2 L^2}$$

$$Y_1 = \frac{r_c}{\omega^2 L^2} + \frac{1}{j\omega L} \qquad \because \omega L >> r_c \text{ from equation (1)}$$

$$Y_2 = \frac{1}{R_p} + \frac{1}{j\omega L}$$

$\therefore$ Therefore, equating Y_1 and Y_2 we get,

$$\frac{r_c}{\omega^2 L^2} + \frac{1}{j\omega L} = \frac{1}{R_p} + \frac{1}{j\omega L}$$

$$\therefore \qquad \frac{1}{R_p} = \frac{r_c}{\omega^2 L^2}$$

$$\boxed{\frac{1}{Q_c} = \frac{r_c}{\omega L}} \Rightarrow Q_c = \frac{\omega L}{r_c}$$

$$= \frac{r_c^2}{r_c\, \omega^2 L^2} = \frac{1}{r_c\, Q_c^2}$$

$$\therefore \qquad \boxed{R_p = r_c\, Q_c^2 = \omega L Q_c} \qquad \because \omega L = Q_c\, r_c \text{ from equation (1)} \quad \ldots (2)$$

Looking at Fig. 3.8 we have,

$$\therefore \qquad \boxed{R = r_i \parallel R_p \parallel r_{b'e}} \qquad \ldots (3)$$

The current gain of the amplifier is then

$$A_i = \frac{-g_m R}{1 + j(\omega RC - R/\omega L)} = \frac{-g_m R}{1 + j\,\omega_o RC(\omega/\omega_o - \omega_o/\omega)} \qquad \ldots (4)$$

where $\qquad \omega_o^2 = \frac{1}{LC}$

We define the Q of the tuned circuit at the resonant frequency w_0 to be

$$Q_i = \frac{R}{\omega_0 L} = \omega_0 RC \qquad \ldots(5)$$

$$\therefore \quad \boxed{A_i = \frac{-g_m R}{1 + jQ_i(\omega/\omega_o - \omega_o/\omega)}}$$

At $\omega = \omega_0$, gain is maximum and it is given as,

$$\therefore \quad \boxed{A_{i\,(max)} = -g_m R} \qquad \ldots(6)$$

The Fig. 3.10 shows the gain versus frequency plot for the single tuned amplifier. It shows the variation of the magnitude of the gain as a function of frequency.

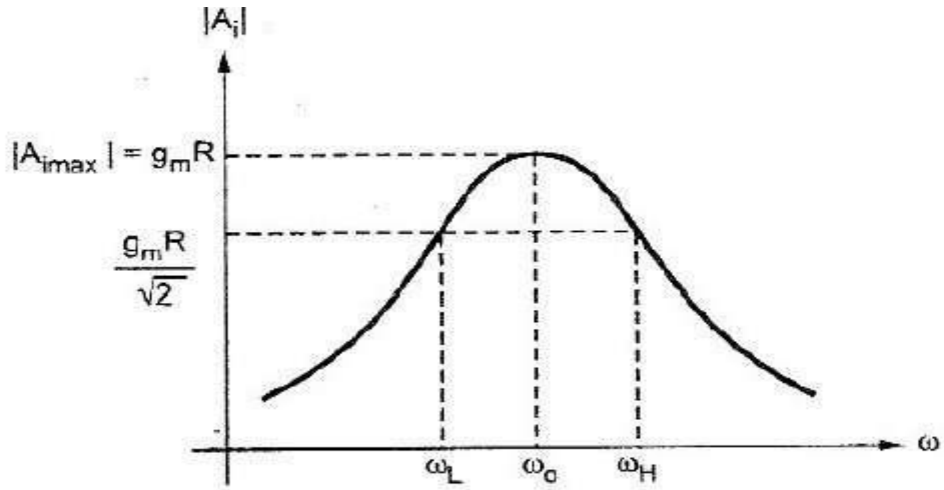


Fig. 3.10 Gain versus frequency for single tuned amplifier

At 3 dB frequency,

$$|A_i| = \frac{g_m R}{\sqrt{2}} \qquad \ldots(7)$$

$\therefore$ At 3 dB frequency

$$1 + jQ_i\,[(\omega/\omega_o) - (\omega_o/\omega)] = \sqrt{2}$$

$$\therefore \quad 1 + Q_i^2\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)^2 = 2 \qquad \ldots(8)$$

This equation is quadratic in w^2 and has two positive solutions, w_H and w_L. After solving equation (8), 3 dB bandwidth is given below:

$BW = f_H - f_L = w_0/2\pi Q_i = 1/2\pi RC$ (since $Q_i = w_0 RC$) ….. (9)

$$\therefore \quad \boxed{BW = \frac{1}{2\pi RC}}$$

Example 3.1 : *Design a single tuned amplifier for following specifications :*

1. *Centre frequency = 500 kHz*
2. *Bandwidth = 10 kHz*

Assume transistor parameters : $g_m = 0.04$ *S,* $h_{fe} = 100$*,* $C_{b'e} = 1000$ *pF and* $C_{b'c} = 100$ *pF. The bias network and the input resistance are adjusted so that* $r_i = 4\ k\Omega$ *and* $R_L = 510\ \Omega$*.*

Solution : From equation (9) we have,

$$BW = \frac{1}{2\pi RC}$$

$$\therefore \quad RC = \frac{1}{2\pi BW} = \frac{1}{2\pi \times 10 \times 10^3}$$

$$= 15.912 \times 10^{-6}$$

From equation (3) we have,

$$R = r_i \parallel R_p \parallel r_{b'e}$$

where

$$r_i = 4\ k\Omega$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{0.04} = 2500\ \Omega$$

$$R_p = Q_c\, \omega_o L = \frac{Q_c}{\omega_o C}$$

$$\therefore \quad R = 4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{\omega_o C}$$

$$C = \frac{1}{2\pi \times 10 \times 10^3 \times R}$$

$$\therefore \quad C = \frac{1}{2\pi \times 10 \times 10^3 \times \left[4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{2\pi \times 500 \times 10^3 \times C}\right]}$$

The typical range for Q_c is 10 to 150. However, we have to assume Q such that value of C_p should be positive. Let us assume Q = 100.

$$\therefore \quad C = \frac{1}{2\pi \times 10 \times 10^3 \left[1538.5 \parallel \frac{1}{2\pi \times 5000 \times C}\right]}$$

$$= \frac{1}{2\pi \times 10 \times 10^3 \left[\frac{1}{\frac{1}{1538.5} + 2\pi \times 5000 \times C}\right]}$$

Solving for C we get,

$$C = 0.02\ \mu F$$

We have,

$$C = C' + C_{b'e} + (1 + g_m R_L) C_{b'c}$$

$$\therefore \quad C' = C - [C_{b'e} + (1 + g_m R_L) C_{b'c}]$$

$$= 0.02 \times 10^{-6} - [1000 \times 10^{-12} + (1 + 0.04 \times 510) \times 100 \times 10^{-12}]$$

$$\therefore \quad C' = \mathbf{0.01686\ \mu F}$$

We have,

$$\omega_o^2 = \frac{1}{LC}$$

$$\therefore \quad L = \frac{1}{\omega_o^2 C} = \frac{1}{(2\pi \times 500 \times 10^3)^2 \times 0.02 \times 10^{-6}}$$

$$= \mathbf{5\ \mu H}$$

From equation (2) we have,

$$R_p = \omega L Q_c = 2\pi \times 500 \times 10^3 \times 5 \times 10^{-6} \times 100$$

$$= \mathbf{1570\ \Omega}$$

$$\therefore \quad R = r_i \parallel R_p \parallel r_{b'e}$$

$$= 4 \times 10^3 \parallel 1570 \parallel 2500$$

$$= \mathbf{777\ \Omega}$$

We have mid frequency gain as,

$$A_{i\,max} = -g_m R = (-0.04)(777) = -31$$

Single Tuned FET Amplifier:

The Fig.3.11 shows the single tuned FET amplifier.

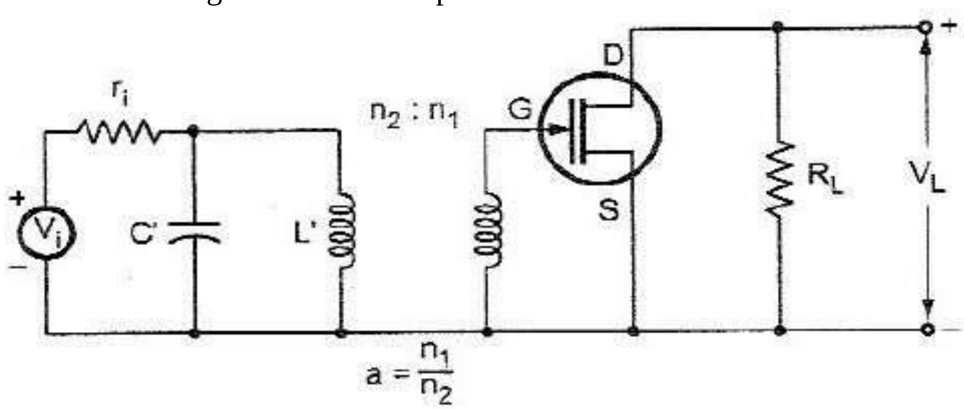


Fig. 3.11 Single tuned FET amplifier

The equivalent circuit for the given amplifier is as shown in the Fig. 3.12.

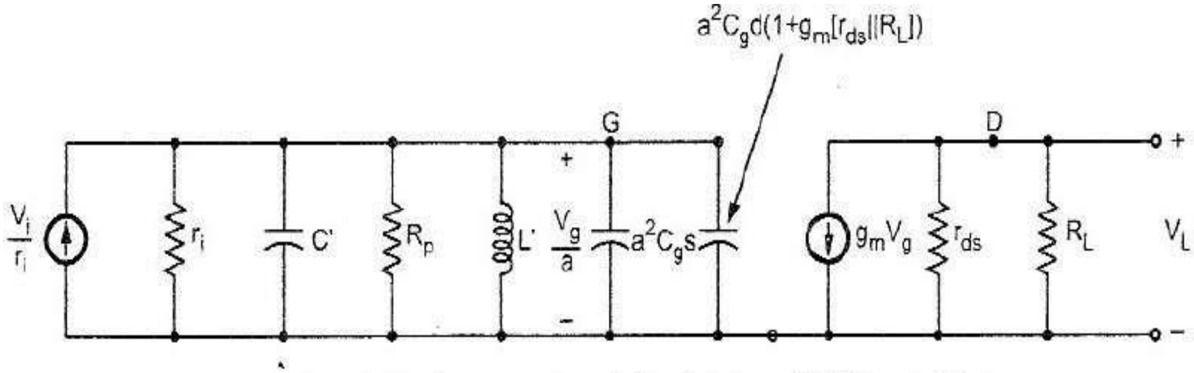


Fig. 3.12 Equivalent circuit of single tuned FET amplifier

The voltage gain is given by,

$$A_v = -a\, g_m\, (r_{ds} \parallel R_L)\, [(r_i \parallel R_p)/\, r_i] \qquad \dots (1)$$

where

$$C_i = a^2\, \{C_{gs} + C_{gd}\, [1 + g_m\, (r_{ds} \parallel R_L)]\} \qquad \dots (2)$$

$$Q_i = \omega_o\, (r_i \parallel R_p)\, (C' + C_i) \qquad \dots (3)$$

$$\omega_o^2 = \frac{1}{L\,(C'+C_i)} \qquad \dots (4)$$

At centre frequency, i.e., at $\omega = \omega_o$ gain is

$$A_{v\,max} = -a\, g_m\, (r_{ds} \parallel R_L)\, \frac{R_p}{r_i + R_p} \qquad \dots (5)$$

The 3 dB bandwidth is given by,

$$BW = \frac{1}{2\pi\,(r_i \parallel R_p)\,(C'+C_i)} \qquad \dots (6)$$

Single Tuned Capacitive Coupled Amplifier:

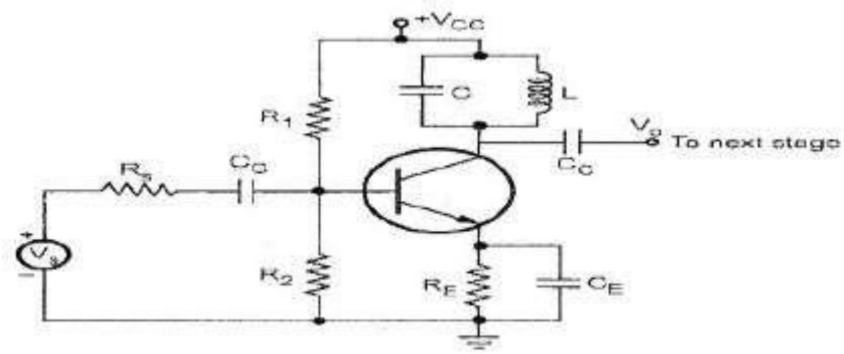


Fig. 3.13 Single tuned capacitive coupled transistor amplifier

Single Tuned multistage amplifier circuit uses one parallel tuned circuit as a load in each stage with tuned circuits in all stages tuned to same frequency. Fig 3.13 shows a typical single tuned amplifier in CE configuration. As shown in Fig.3.13, tuned circuit formed by L and C acts as collector load and resonates at frequency of operation. Resistors R_1, R_2 and R_E along with capacitor C_E provides self bias for the circuit.

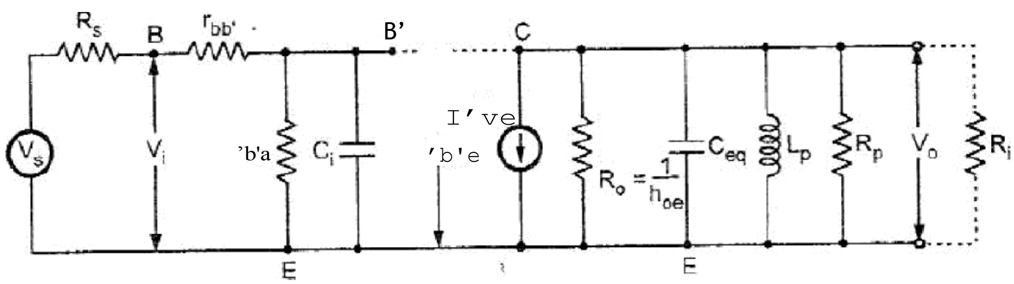


Fig. 3.15 Simplified equivalent circuit for single tuned amplifier

Here C_i and Cq represent inpvit and output circuit capacitance, respectively. They can be given as,

C, = C ,, + C,,, (1 — A) where A is the voltage gain of the amplifier. ,..(1I

$C_{eq} = C_{b'c} \left(\frac{A - I}{A}\right)$ C where C 1s the tuned circuit capacitance. (2)

The gp is represented as the output resistance of current generator ,.

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m h_{re} \approx h_{oe} = \frac{1}{R_o} \qquad (3\}$$

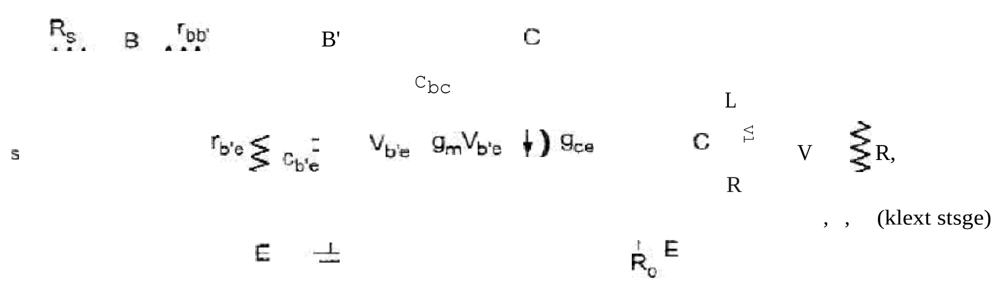


Fig. 3.14 Equivalent circuit of single tuned amplifier

The Fig. 3.14 shows the equivalent circuit for single tuned amplifier using hybrid z paraotetcrs.

As shown in the Fig, 3,I4, is the input Eesistarice of the next stage and is the output resistance of the current generator gp<b,,. TI-ie reactarices of the bypass capacitor C_E and the couphn a •• pacitors Lp are negiiginiy »mau at tne operanng rrequency anci rtcnc.< these elements are neglected in the equivalent circuit shown in the Pig. 3.14.

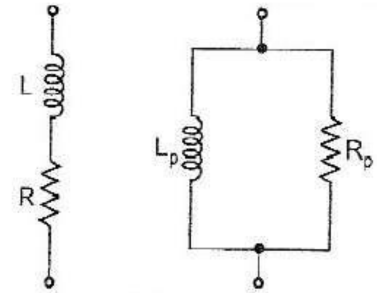


Fig. 3.16

The series RL circuit is represented by its equivalent parallel circuit. The conditions for equivalence are most easily established by equating the admittances of the two circuits shown in Fig. 3.16.

Admittance of the series combination of RL is given as,

$$Y = \frac{1}{R + j\omega L}$$

Multiplying numerator and denominator by $R - j\omega L$ we get,

$$Y = \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega L}{R^2 + \omega^2 L^2}$$

$$= \frac{R}{R^2 + \omega^2 L^2} - \frac{j\omega^2 L}{\omega(R^2 + \omega^2 L^2)}$$

$$= \frac{1}{R_p} + \frac{1}{j\omega L_p}$$

where $$R_p = \frac{R^2 + \omega^2 L^2}{R} \quad \dots (4)$$

and $$L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L} \quad \dots (5)$$

Centre frequency

The centre frequency or resonant frequency is given as,

$$f_r = \frac{1}{2\pi\sqrt{L_p C_{eq}}} \quad \dots (6)$$

where $$L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

and $$C_{eq} = C_{b'c}\left(\frac{A-1}{A}\right) + C \quad \dots (7)$$

$$= C_0 + C$$

Therefore, C_{eq} is the summation of transistor output capacitance and the tuned circuit capacitance.

Quality factor Q

The quality factor Q of the coil at resonance is given by,

$$Q_r = \frac{\omega_r L}{R} \quad \dots (8)$$

where ω_r is the centre frequency or resonant frequency.

This quality factor is also called unloaded Q. But in practice, transistor output resistance and input resistance of next stage act as a load for the tuned circuit. The quality factor including load is called as loaded Q and it can be given as follows :

The Q of the coil is usually large so that $\omega L >> R$ in the frequency range of operation.

From equation (4) we have,

$$R_p = \frac{R^2 + \omega^2 L^2}{R} = R + \frac{\omega^2 L^2}{R}$$

$$\text{As } \frac{\omega^2 L^2}{R} >> 1, \quad R_p \approx \frac{\omega^2 L^2}{R} \qquad \ldots(9)$$

From equation (5) we have,

$$L_p = \frac{R^2 + \omega^2 L^2}{\omega^2 L} = \frac{R^2}{\omega^2 L} + L$$

$$\approx L \qquad \because \omega L >> R \qquad \ldots(10)$$

From equation (9), we can express R_p at resonance as,

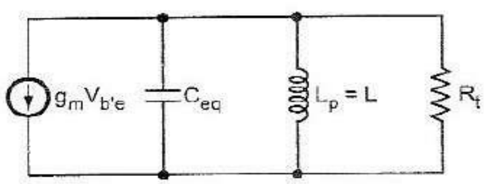
$$R_p = \frac{\omega_r^2 L^2}{R}$$

$$= \omega_r Q_r L \qquad \because Q_r = \frac{\omega_r L}{R} \qquad \ldots(11)$$

Therefore, Q_r can be expressed interms of R_p as,

$$Q_r = \frac{R_p}{\omega_r L} \qquad \ldots(12)$$

The effective quality factor including load can be calculated looking at the simplified equivalent output circuit for single tuned amplifier.



where $R_t = R_o \| R_p \| R_i$

Fig. 3.17 Simplified output circuit for single tuned amplifier

$$\text{Effective quality factor } Q_{eff} = \frac{\text{Susceptance of inductance L or capacitance C}}{\text{Conductance of shunt resistance } R_t}$$

$$= \frac{R_t}{\omega_r L} \text{ or } \omega_r C_{eq} R_t \qquad \ldots(13)$$

Voltage gain (A_v)

The voltage gain for single tuned amplifier is given by,

$$A_v = -g_m \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \times \frac{R_t}{1 + 2jQ_{eff}\delta}$$

where $R_t = R_o || R_p || R_i$

δ = Fraction variation in the resonant frequency

$$A_v \text{ (at resonance)} = -g_m \frac{r_{b'e}}{r_{bb'} + r_{b'e}} \times R_t$$

$$\therefore \left| \frac{A_v}{A_v(\text{at resonance})} \right| = \frac{1}{\sqrt{1 + (2\delta Q_{eff})^2}} \quad \text{... (14)}$$

3 dB bandwidth

The 3 dB bandwidth of a single tuned amplifier is given by,

$$\Delta f = \frac{1}{2\pi R_t C_{eq}}$$

$$= \frac{\omega_r}{2\pi Q_{eff}} \quad \because Q_{eff} = \omega_r R_t C_{eq} \quad \text{... (15)}$$

$$= \frac{f_r}{Q_{eff}} \quad \because \omega_r = 2\pi f_r \quad \text{... (16)}$$

Example 3.2 : *A single tuned RF amplifier uses a transistor with an output resistance of 50 K, output capacitance of 15 pF and input resistance of next stage is 20 kΩ. The tuned circuit consists of 47 pF capacitance in parallel with series combination of 1 μH inductance and 2 Ω resistance. Calculate*

i) Resonant frequency

ii) Effective quality factor

iii) Bandwidth of the circuit

Solution : i) Resonant frequency f_r is given as,

$$f_r = \frac{1}{2\pi\sqrt{L C_{eq}}}$$

$$= \frac{1}{2\pi\sqrt{1\ \mu H \times (15\ pF + 47\ pF)}}$$

$$= \mathbf{20.2\ MHz}$$

ii) Effective quality factor is given as,

$$Q_{eff} = \omega_r C_{eq} R_t$$

$$= 2\pi f_r C_{eq} \times (R_o || R_p || R_i)$$

where $R_p = \frac{\omega_r^2 L^2}{R} = \frac{(2\pi \times 20.2 \times 10^6)^2 (1 \times 10^{-6})^2}{2}$

$= 8054\ \Omega$

$\therefore \quad Q_{eff} = 2\pi \times 20.2 \times 10^6 \times (15\text{ pF} + 47\text{ pF}) \times (50\text{ K} \,||\, 8.054\text{ K} \,||\, 20\text{ K})$

$= \mathbf{40.52}$

iii) Bandwidth of the circuit is given as,

$BW = \frac{f_r}{Q_{eff}} = \frac{20.2 \times 10^6}{40.52}$

$= \mathbf{498.5\ kHz}$

Example 3.3 : *A single tuned transistor amplifier is used to amplify modulated RF carrier of 600 kHz and bandwidth of 15 kHz. The circuit has a total output resistance, $R_t = 20\ k\Omega$ and output capacitance $C_o = 50\ pF$. Calculate values of inductance and capacitance of the tuned circuit.*

Solution : Given : $f_r = 600$ kHz

$BW = 15$ kHz

$R_t = 20\ k\Omega$

$C_o = 50$ pF

$\therefore \quad C_{eq} = (50\text{ pF} + C)$

$Q_{eff} = \frac{f_r}{BW} = \frac{600\text{ kHz}}{15\text{ kHz}}$

$= 40$

i) We know that,

$Q_{eff} = \omega_r C_{eq} R_t$

$\therefore \quad C_{eq} = \frac{Q_{eff}}{\omega_r R_t} = \frac{40}{2\pi \times 600 \times 10^3 \times 20 \times 10^3}$

$= 530.5$ pF

$C_{eq} = (50\text{ pF} + C)$

$\therefore \quad C = 530.5\text{ pF} - 50\text{ pF}$

$= \mathbf{480.5\ pF}$

ii) We know that,

$f_r = \frac{1}{2\pi\sqrt{L C_{eq}}}$

$\therefore \quad L = \frac{1}{(2\pi f_r)^2 C_{eq}} = \frac{1}{(2\pi \times 600 \times 10^3)^2 \times 530.5 \times 10^{-12}}$

$= \mathbf{132.6\ \mu H}$

Double Tuned Amplifier:

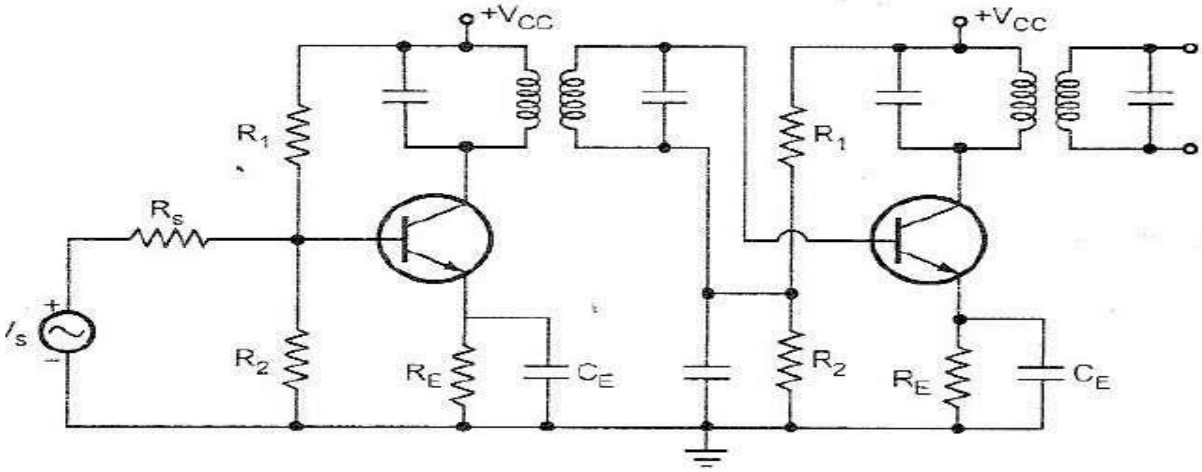
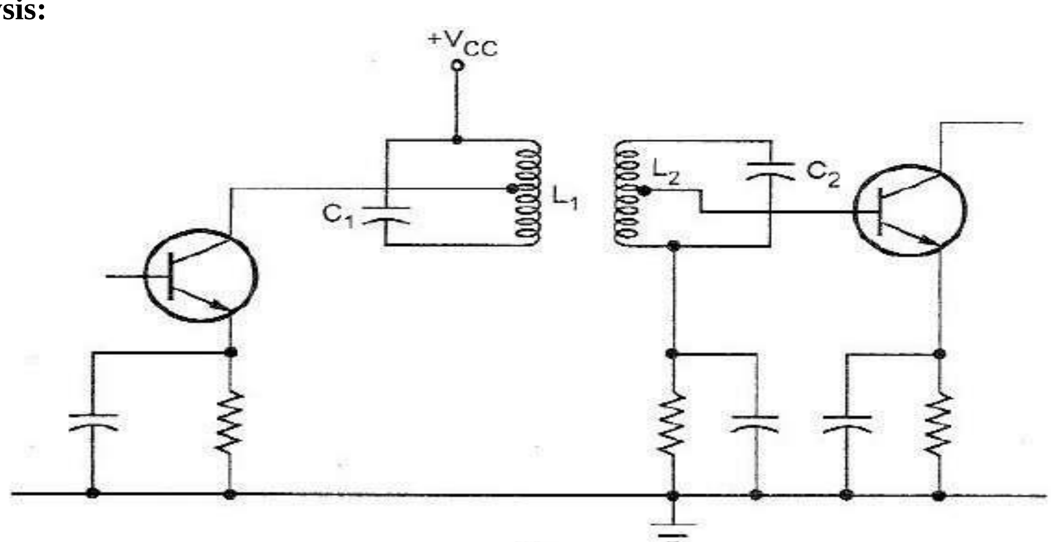


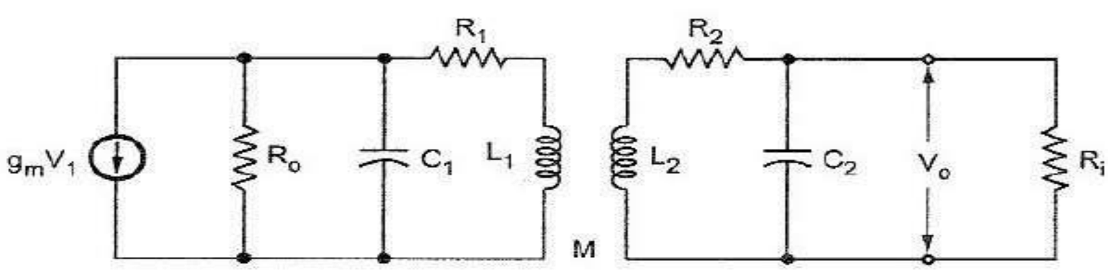
Fig. 3.18 Double tuned amplifier

Fig 3.18 shows double tuned RF amplifier in CE configuration. Here, voltage developed across tuned circuit is coupled inductively to another tuned circuit. Both tuned circuits are tuned to the same frequency. The double tuned circuit can provide a bandwidth of several percent of the resonant frequency and gives steep sides to the response curve. Let us analyze the double tuned circuit.

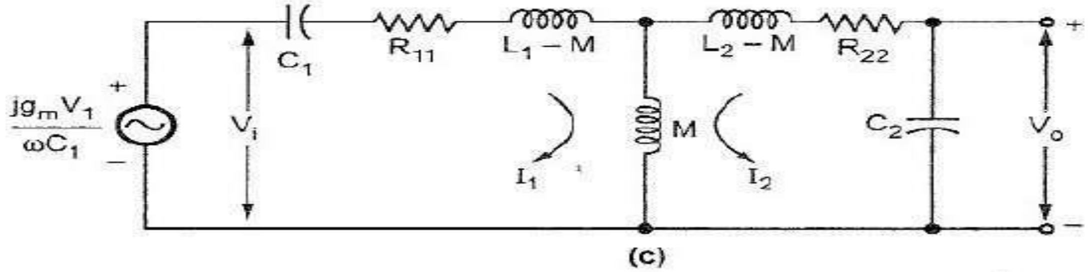
Analysis:



(a)



(b)



(c)

Fig. 3.19 Equivalent circuits for double tuned amplifier

The Fig. 3.19 (a) shows the coupling section of a transformer coupled double tuned amplifier. The Fig. 3.19 (b) shows the equivalent circuit for it, in which transistor is replaced by the current source with its output resistance (R_o). The C_1 and L_1 are the tank circuit components of the primary side. The resistance R_1 is the series resistance of the inductance L_1. Similarly on the second side L_2 and C_2 represent the tank circuit components of the secondary side and R_2 represents resistance of the inductance L_2. The resistance R_i represents the input resistance of the next stage.

The Fig. 3.19 (c) shows the simplified equivalent circuit for the Fig. 3.19 (b). In simplified equivalent circuit the series and parallel resistances are combined into series elements. Referring equation (9) we have,

$$R_p = \frac{\omega^2 L^2}{R} \text{ i.e. } R = \frac{\omega^2 L^2}{R_p}$$

where R represents series resistance and R_p represents parallel resistance.

Therefore we can write,

$$R_{11} = \frac{\omega_o^2 L_1^2}{R_o} + R_1$$

$$R_{12} = \frac{\omega_o^2 L_2^2}{R_i} + R_2$$

In the simplified circuit the current source is replaced by voltage source, which is now in series with C_1. It also shows the effect of mutual inductance on primary and secondary sides.

We know that, $Q = \frac{\omega_r L}{R}$

Therefore, the Q factors of the individual tank circuits are

$$Q_1 = \frac{\omega_r L_1}{R_{11}} \text{ and } Q_2 = \frac{\omega_r L_2}{R_{22}} \quad \ldots(1)$$

Usually, the Q factors for both circuits are kept same. Therefore, $Q_1 = Q_2 = Q$ and the resonant frequency $\omega_r^2 = 1/L_1 C_1 = 1/L_2 C_2$.

Looking at Fig. 3.19 (c), the output voltage can be given as,

$$V_o = -\frac{j}{\omega_r C_2} I_2 \quad \ldots(2)$$

$$Y_T \quad \frac{I_2}{V_1} = \frac{I_2}{I_1 Z_{11}} \quad \frac{A_i}{Z_{11}}$$

here

$$Z_{11} \quad \frac{1}{I_1} \quad Z_i - \frac{Z_f}{Z_o + Z_L} \text{ and}$$

The simplified :cQuivalenf circuit for double tuned amplifier: is similar to. the circuit shorn in Fig. 3,20 with

$$Z_f = j\,\omega_r M$$

$$Z_i \quad R_{11} + j\left(\omega L_1 - \frac{1}{\omega C_1}\right)$$

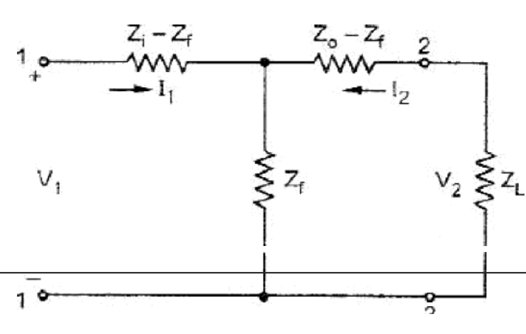
$$Z_o + Z_L \quad R_{22} + j\left(\omega L_2 - \frac{1}{\omega C_2}\right)$$

The equations Ior Zp and Z.3 + cm be furthur simp1i‘fied as shown be1or.

$$Z_f = j\omega_r M = j\omega_r k\sqrt{L_1 L_2}$$

where, k is the coeffioent of coupling..

To calculate Vq/V, it is necessary to represent 1_2 interns of V;. For tRis we have to find the transfer admikance Y_T. Let xis consider the circuit shown in Fig. 3W. For this circuit, the transfer admittance can be given as.



Multiplying numerator and denominator by $\omega_r L_1$ for Z_i we get,

$$Z_i = \frac{R_{11}\,\omega_r\,L_1}{\omega_r\,L_1} + j\omega_r\,L_1\left(\frac{\omega L_1}{\omega_r\,L_1} - \frac{1}{\omega C_1\,\omega_r L_1}\right)$$

$$= \frac{\omega_r\,L_1}{Q} + j\omega_r\,L_1\left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right) \qquad \because Q = \frac{\omega_r\,L}{R_{11}} \text{ and } \frac{1}{\omega_r\,L} = \omega_r\,C$$

$$= \frac{\omega_r\,L_1}{Q} + j\omega_r\,L_1\,(2\,\delta) \qquad \because \frac{\omega}{\omega_r} - \frac{\omega_r}{\omega} = 1 + \delta - (1 - \delta) = 2\,\delta$$

$$= \frac{\omega_r\,L_1}{Q} + (1 + j2\,Q\,\delta)$$

$$Z_o + Z_L = R_{22} + j\left(\omega L_2 - \frac{1}{\omega C_2}\right)$$

By doing similar analysis as for Z_i we can write,

$$Z_o + Z_L = \frac{\omega_r\,L_2}{Q} + (1 + j2\,Q\,\delta)$$

Then

$$Y_T = \frac{Z_f}{Z_f^2 - Z_i\,(Z_o + Z_L)} = \frac{1}{Z_f - Z_i\,(Z_o + Z_L)\,/\,Z_f}$$

$$Y_T = \frac{1}{j\,\omega_r\,k\sqrt{L_1\,L_2} - \dfrac{\left[\dfrac{\omega_r\,L_1}{Q}\,(1 + j\,2\,Q\delta)\left\{\dfrac{\omega_r\,L_2}{Q}\,(1 + j\,2\,Q\delta)\right\}\right]}{j\,\omega_r\,k\sqrt{L_1\,L_2}}}$$

$$Y_T = \frac{kQ^2}{\omega_r\,\sqrt{L_1\,L_2}\left[4\,Q\,\delta - j\,(1 + k^2Q^2 - 4\,Q^2\,\delta^2)\right]} \qquad \dots (3)$$

Substituting value of I_2, i.e. $V_i \times Y_T$ we get,

$$V_o = \frac{-j}{\omega_r\,C_2}\,\frac{j\,g_m\,V_i}{\omega_r\,C_1}\left[\frac{kQ^2}{\omega_r\,\sqrt{L_1\,L_2}\left[4\,Q\,\delta - j\,(1 + k^2Q^2 - 4\,Q^2\,\delta^2)\right]}\right]$$

$$\because V_i = \frac{j\,g_m\,V_1}{\omega C_1}$$

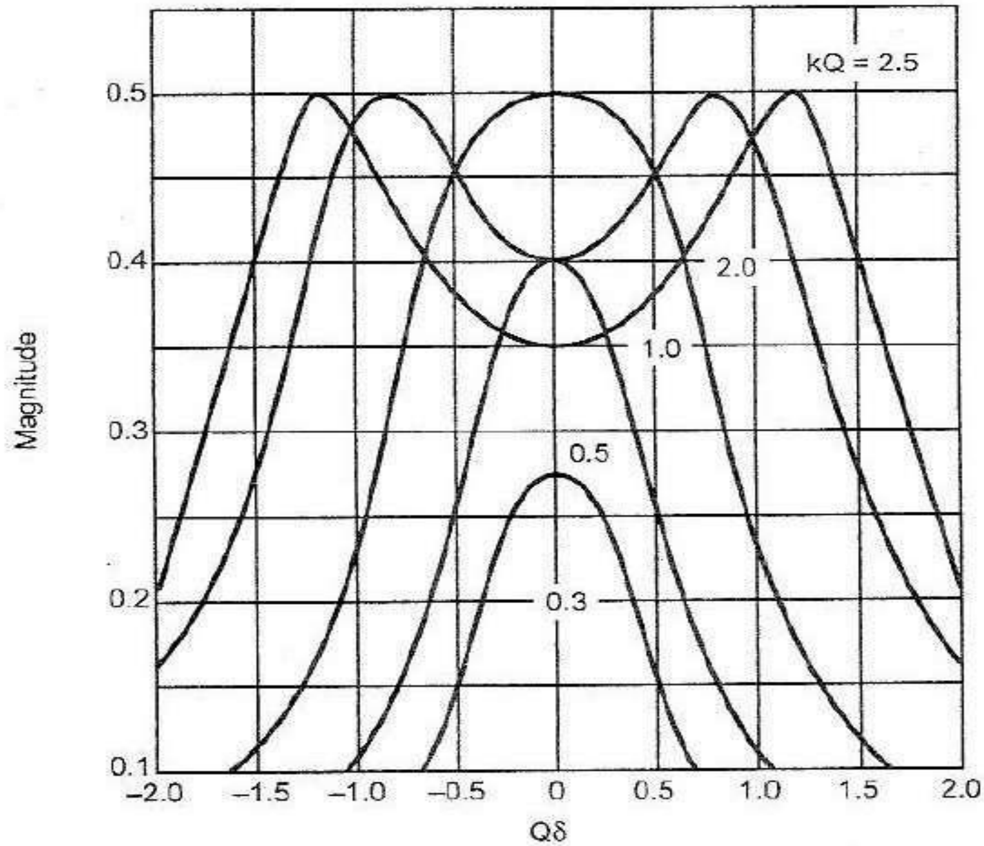


Fig. 3.21

$$\therefore \quad A_v = \frac{V_o}{V_i} = g_m \, \omega_r^2 \, L_1 L_2 \left[\frac{kQ^2}{\omega_r \sqrt{L_1 \, L_2} \left[4\,Q\delta - j\,(1 + k^2Q^2 - 4\,Q^2\,\delta^2) \right]} \right]$$

$$\because \frac{1}{\omega_r \, C} = \omega_r \, L$$

$$= \left[\frac{g_m \, \omega_r \sqrt{L_1 \, L_2} \; kQ^2}{4\,Q\delta - j\,(1 + k^2Q^2 - 4\,Q^2\,\delta^2)} \right] \qquad \dots (4)$$

Taking the magnitude of equation (4) we have,

$$|A_v| = g_m \, \omega_r \sqrt{L_1 \, L_2} \; Q \frac{kQ}{\sqrt{1 + k^2Q^2 - 4\,Q^2\,\delta^2 + 16\,Q^2\,\delta^2}} \qquad \dots (5)$$

The Fig. 3.21 shows the universal response curve for double tuned amplifier plotted with kQ as a parameter.

The frequency deviation δ at which the gain peaks occur can be found by maximizing equation (4), i.e.

$$4Q\delta - j\,(1 + k^2Q^2 - 4Q^2\delta^2) = 0 \qquad \dots (6)$$

As shown in the Fig. 3.22, two gain peaks in the frequency response of the double tuned amplifier can be given at frequencies :

$$f_1 = f_r\left(1-\frac{1}{2Q}\sqrt{k^2Q^2-1}\right) \text{ and}$$

$$f_2 = f_r\left(1+\frac{1}{2Q}\sqrt{k^2Q^2-1}\right) \quad \dots (7)$$

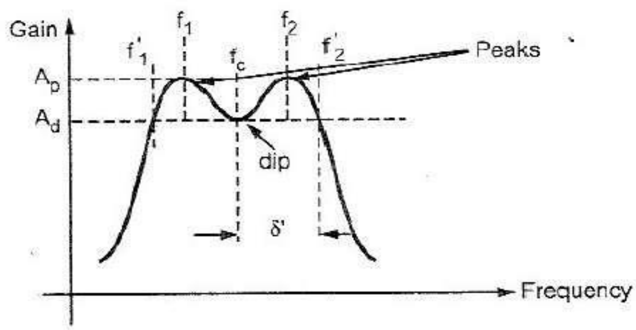


Fig. 3.22

At $k^2Q^2 = 1$, i.e. $k = \frac{1}{Q}$, $f_1 = f_2 = f_r$. This condition is known as **critical coupling**. For values of $k < 1/Q$, the peak gain is less than maximum gain and the coupling is poor.

At $k > 1/Q$, the circuit is overcoupled and the response shows the double peak. Such double peak response is useful when more bandwidth is required.

The gain magnitude at peak is given as,

$$|A_p| = \frac{g_m\, \omega_o \sqrt{L_1 L_2}\, kQ}{2} \quad \dots (8)$$

And gain at the dip at $\delta = 0$ is given as,

$$|A_d| = |A_p|\,\frac{2\,kQ}{1+k^2Q^2} \quad \dots (9)$$

The ratio of peak gain and dip gain is denoted as γ and it represents the magnitude of the ripple in the gain curve.

$$\gamma = \left|\frac{A_p}{A_d}\right| = \frac{1+k^2Q^2}{2\,kQ} \quad \dots (10)$$

Using quadratic simplification and choosing positive sign we get,

$$kQ = \gamma+\sqrt{\gamma^2-1} \quad \dots (11)$$

The bandwidth between the frequencies at which the gain is $|A_d|$ is the useful bandwidth of the double tuned amplifier. It is given as,

$$BW = 2\,\delta' = \sqrt{2}\,(f_2-f_1) \quad \dots (12)$$

At 3 dB bandwidth,

$$\gamma = \sqrt{2}$$

$$\therefore \quad kQ = \gamma + \sqrt{\gamma^2 + 1} = \sqrt{2} + \sqrt{\sqrt{2}^2 + 1} = 2.414$$

$$\therefore \quad 3 \text{ dB BW} = 2\,\delta' = \sqrt{2}\,(f_2 - f_1)$$

$$= \sqrt{2}\left[f_r\left(1 + \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right) - f_r\left(1 - \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right)\right]$$

$$= \sqrt{2}\left[\left(\frac{f_r}{Q}\sqrt{k^2Q^2 - 1}\right)\right]$$

$$= \sqrt{2}\left[\frac{f_r}{Q}\sqrt{(2.414)^2 - 1}\right] = \frac{3.1\,f_r}{Q}$$

We know that, the 3 dB bandwidth for single tuned amplifier is $2f_r$ / Q. Therefore, the 3 dB bandwidth provided by double tuned amplifier ($3.1f_f$ / Q) is substantially greater than the 3 dB bandwidth of single tuned amplifier.

Compared with a single tuned amplifier, the double tuned amplifier

1. Possesses a flatter response having steeper sides.
2. Provides larger 3 dB bandwidth.
3. Provides large gain-bandwidth product.

Effect of cascading Single Tuned Amplifier on Bandwidth:

In order to obtain a high overall gain, several identical stages of amplifiers can be used in cascade. The overall gain is the product of the voltage gains of the individual stages. Let us see the effect of cascading of stages on bandwidth.

Consider n stages of single tuned direct coupled amplifiers connected in cascade. We know that the relative gain of a single tuned amplifier w.r.t. the gain at resonant frequency f_r is given from equation (14).

$$\left|\frac{A_v}{A_v\,(\text{at resonance})}\right| = \frac{1}{\sqrt{1 + (2\delta Q_{eff})^2}}$$

Therefore, the relative gain of n stage cascaded amplifier becomes

$$\left|\frac{A_v}{A_v\,(\text{at resonance})}\right|^n = \left[\frac{1}{\sqrt{1 + (2\delta Q_{eff})^2}}\right]^n = \frac{1}{\left[1 + (2\delta Q_{eff})^2\right]^{\frac{n}{2}}}$$

The 3 dB frequencies for the n stage cascaded amplifier can be found by equating

$$\left|\frac{A_v}{A_v\,(\text{at resonance})}\right|^n = \frac{1}{\sqrt{2}}$$

$$\therefore \quad \left|\frac{A_v}{A_v\,(\text{at resonance})}\right|^n = \frac{1}{\left[1 + (2\delta Q_{eff})^2\right]^{\frac{n}{2}}} = \frac{1}{\sqrt{2}}$$

$$\therefore \quad \left[1 + (2\delta Q_{eff})^2\right]^{\frac{n}{2}} = 2^{\frac{1}{2}}$$

$$\therefore \quad \left[1 + (2\delta Q_{eff})^2\right]^n = 2$$

$$\therefore \quad 1 + (2\delta Q_{eff})^2 = 2^{\frac{1}{n}}$$

$$\therefore \quad 2\delta Q_{eff} = \pm\sqrt{2^{\frac{1}{n}} - 1}$$

Substituting for δ, the fractional frequency variation, i.e.

$$\delta = \frac{\omega - \omega_r}{\omega_r} = \frac{f - f_r}{f_r}$$

$$\therefore \quad 2\left(\frac{f - f_r}{f_r}\right) Q_{eff} = \pm\sqrt{2^{\frac{1}{n}} - 1}$$

$$\therefore \quad 2(f - f_r) Q_{eff} = \pm f_r \sqrt{2^{\frac{1}{n}} - 1}$$

$$\therefore \quad f - f_r = \pm \frac{f_r}{2 Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1}$$

Let us assume f_1 and f_2 are the lower 3 dB and upper 3 dB frequencies, respectively. Then we have

$$f_2 - f_r = + \frac{f_r}{2 Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1} \text{ and similarly,}$$

$$f_r - f_1 = + \frac{f_r}{2 Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1}$$

The bandwidth of n stage identical amplifier is given as,

$$BW_n = f_2 - f_1 = (f_2 - f_r) + (f_r - f_1)$$

$$= \frac{f_r}{2 Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1} + \frac{f_r}{2 Q_{eff}} \sqrt{2^{1/n} - 1}$$

$$= \frac{f_r}{Q_{eff}} \sqrt{2^{\frac{1}{n}} - 1}$$

$$= BW_1 \sqrt{2^{\frac{1}{n}} - 1} \quad \dots (1)$$

where BW_1 is the bandwidth of single stage and BW_n is the bandwidth of n stages.

Example 3.4 : *The bandwidth for single tuned amplifier is 20 kHz. Calculate the bandwidth if such three stages are cascaded. Also calculate the bandwidth for four stages.*

Solution : i) We know that,

$$BW_n = BW_1 \sqrt{2^{\frac{1}{n}} - 1} = 20 \times 10^3 \times \sqrt{2^{\frac{1}{3}} - 1}$$

$$= \mathbf{10.196\ kHz}$$

ii) $$BW_n = 20 \times 10^3 \times \sqrt{2^{\frac{1}{4}} - 1} = \mathbf{8.7\ kHz}$$

The above example shows that bandwidth decreases as number of stages increase.

Effect of cascading Double Tuned Amplifiers on Bandwidth:

When a number of identical double tuned amplifier stages are connected in cascade, the overall bandwidth, of the system is thereby narrowed and the steepness of the sides of the response is increased, just as when single tuned stages are cascaded. The quantitative relation between the 3 dB bandwidth of n identical double tuned critically coupled stages compared with the bandwidth Δ_2 of such a system can be shown to be 3 dB bandwidth for n identical stages double tuned amplifiers is,

$$\Delta_2 \times \left(2^{\frac{1}{n}} - 1\right)^{\frac{1}{4}}$$

where Δ_2 is the 3 dB bandwidth of single stage double tuned amplifier.
The above equation assumes that the bandwidth Δ_2 is small compared with the resonant frequency.

Example 3.5 : *The bandwidth for double tuned amplifier is 20 kHz. Calculate the bandwidth if such three stages are cascaded.*

Solution : We know that for double tuned cascaded stages,

$$BW_n = BW_1 \times \left(2^{1/n} - 1\right)^{\frac{1}{4}}$$

$$= 20\text{ K} \times \left(2^{1/3} - 1\right)^{\frac{1}{4}}$$

$$= \mathbf{14.28\ kHz}$$

Example 3.6 : *A three stage double tuned amplifier system is to have a half power BW of 20 kHz centred on a centre frequency of 450 kHz. Assuming that all stages are identical, determine the half power bandwidth of single stage. Assume that each stage couple to get maximum flatness.*

Solution : We get maximum flat response when each stage is critically coupled. When stages are critically coupled we have

$$BW_n = BW_1 \times (2^{1/n} - 1)^{1/4}$$

$$BW_n = \frac{BW_n}{(2^{1/n} - 1)^{1/4}}$$

For $n = 3$

$$BW_n = \frac{BW_n}{(2^{1/3} - 1)^{1/4}}$$

$$= \frac{20 \times 10^3}{(2^{1/3} - 1)^{1/4}}$$

$$= \mathbf{28.01\ kHz}$$

Staggered Tuned Amplifier:

Double tuned amplifiers give greater 3 dB bandwidth having steeper sides and flat top. But alignment of double tuned amplifier is difficult. To overcome this problem, two single tuned cascaded amplifiers having certain bandwidth are taken and their resonant frequencies are so that they are separated by an amount equal to the bandwidth of each stage. Since the resonant frequencies are displaced or staggered, they are known as stagger tuned amplifiers. The advantage of stagger tuned amplifier is to have better flat, wideband characteristics in contrast with a very sharp, narrow band characteristic of synchronously tuned circuits (tuned to same resonant frequencies). Fig 3.23 shows the relation of amplification characteristics of individual stages in a staggered pair to the overall amplification of the two stages.

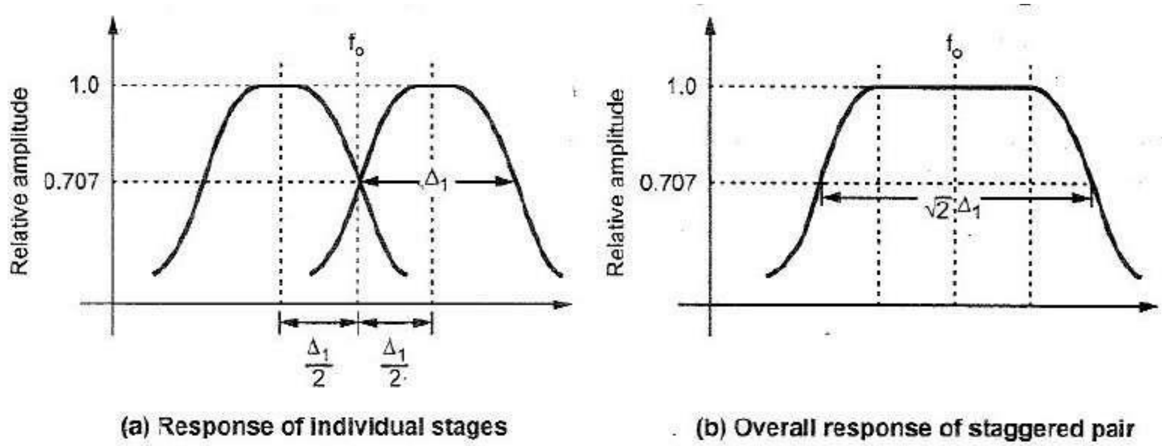


Fig. 3.23

The overall response of the two stage stagger tuned pair is compared in the Fig. 3.24 with the corresponding individual single tuned stages having same resonant circuits. Looking at Fig 3.24, it can be seen that staggering reduces the total amplification of the centre frequency to 0.5 of the peak amplification of the individual stage and at the centre frequency each stage has amplification that is 0.707 of the peak amplification of the individual stage. Thus the equivalent voltage amplification per stage of the staggered pair is 0.707 times as great as when the same two stages are used without staggering. However, the half power (3 dB) bandwidth of the staggered pair is √2 times as great as the half power (3 dB) bandwidth of on individual single tuned stage. Hence the equivalent gain bandwidth product per stage of a stagger tuned pair is 0.707 x √2 = 1.00 times that of the individual single tuned stages.

The stagger tuned idea can be easily extended to more stages. In case of three stages staggering, the first tuning circuit is tuned to a frequency lower than centre frequency while the third circuit is tuned to higher frequency than centre frequency. The middle tuned circuit is tuned at exact centre frequency.

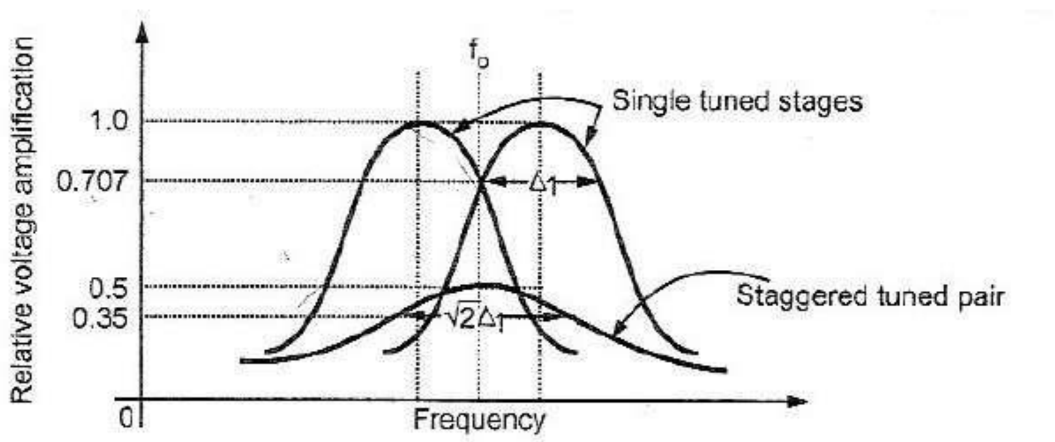


Fig. 3.24 Response of individually tuned and staggered tuned pair

Analysis:

Form equation (14), the gain of the single stage tuned amplifier can be written as,

$$\frac{A_v}{A_v \text{ (at resonance)}} = \frac{1}{1+2jQ_{eff}\,\delta}$$

$$= \frac{1}{1+jX} \text{ where } X = 2\,Q_{eff}\,\delta$$

Since in stagger tuned amplifiers the two single tuned cascaded amplifiers with separate resonant frequencies are used, we can assume that the one stage is tuned to the frequency $f_r + \delta$ and other stage is tuned to the frequency $f_r - \delta$. Therefore we have,

$$f_{r1} = f_r + \delta$$

and $$f_{r2} = f_r - \delta$$

According to these tuned frequencies the selectivity functions can be given as,

$$\frac{A_v}{A_v \text{ (at resonance)}_1} = \frac{1}{1+j(X+1)} \text{ and}$$

$$\frac{A_v}{A_v \text{ (at resonance)}_2} = \frac{1}{1+j(X-1)}$$

The overall gain of these two stages is the product of individual gains of the two stages.

$$\therefore \quad \frac{A_v}{A_v \text{ (at resonance)}_{\text{cascaded}}} = \frac{A_v}{A_v \text{ (at resonance)}_1} \times \frac{A_v}{A_v \text{ (at resonance)}_2}$$

$$= \frac{1}{1+j(X+1)} \times \frac{1}{1+j(X-1)}$$

$$= \frac{1}{2+2jX-X^2} = \frac{1}{(2-X^2)+(2jX)}$$

$$\therefore \quad \left|\frac{A_v}{A_v \text{ (at resonance)}}\right|_{\text{cascaded}} = \frac{1}{\sqrt{(2-X^2)^2+(2X)^2}}$$

$$= \frac{1}{\sqrt{4-4X^2+X^4+4X^2}} = \frac{1}{\sqrt{4+X^4}}$$

Substituting the value of X we get,

$$\left|\frac{A_v}{A_v \text{ (at resonance)}}\right|_{\text{cascaded}} = \frac{1}{\sqrt{4+(2Q_{eff}\,\delta)^4}} = \frac{1}{\sqrt{4+16\,Q_{eff}^4\,\delta^4}}$$

$$= \frac{1}{2\sqrt{1+4\,Q_{eff}^4\,\delta^4}}$$

5.9 Large Signal Tuned Amplifiers:

The output efficiency of an amplifier increases as the operation shifts from class A to class C through class AB and class B. As the output power of a radio transmitter is high and the efficiency is of prime concern, class B and class C amplifiers are used at the output stages in transmitters.

The operation of class B and class C amplifiers are non-linear since the amplifying elements remain cut-off during a part of the input signal cycle. The non-linearity generates harmonics of the signal frequency at the output of the amplifier. In the push-pull arrangement where the bandwidth requirement is no limited, these harmonics can be eliminated or reduced. When a narrow bandwidth is desired, a resonant circuit is employed in class B and class C tuned RF power amplifiers to eliminate the harmonics.

Class B Tuned Amplifier:

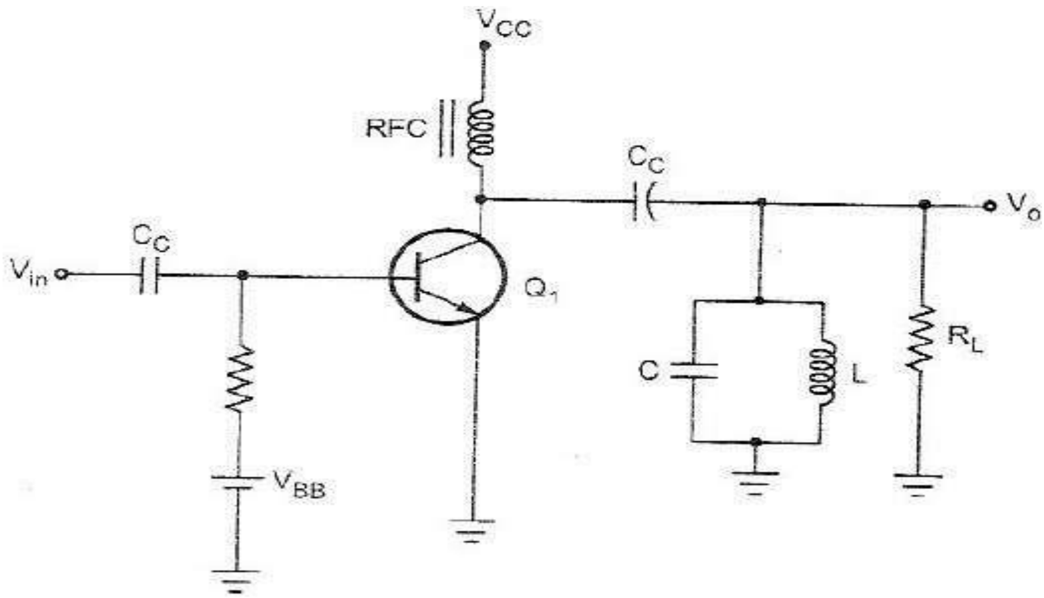


Fig. 3.25 Class B tuned amplifier

The Fig 3.25 shows the class B tuned amplifier. It works with a single transistor by sending half sinusoidal current pulses to the load. The transistor is biased at the edge of the conduction. Even though the input is half sinusoidal, the load voltage is sinusoidal because a high Q RLC tank shunts harmonics to ground. The negative half is delivered by the RLC tank. The Q factor of the tank needs to be large enough to do this. This is analogous to pushing someone in swing. We only need to push in one direction, and the reactive energy stored will swing the person back in the reverse direction.

Class C Tuned Amplifier:

The amplifier is said to be class C amplifier, if the Q point and the input signal are selected such the output signal is obtained for less than a half cycle, for a full cycle.

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output.

The current and voltage waveforms for a class C operation are shown in the Fig. 3.26. Looking at Fig 3.26, it is apparent that the total angle during which current flows is less than 180^0. This angle is called the conduction angle, θ_c.

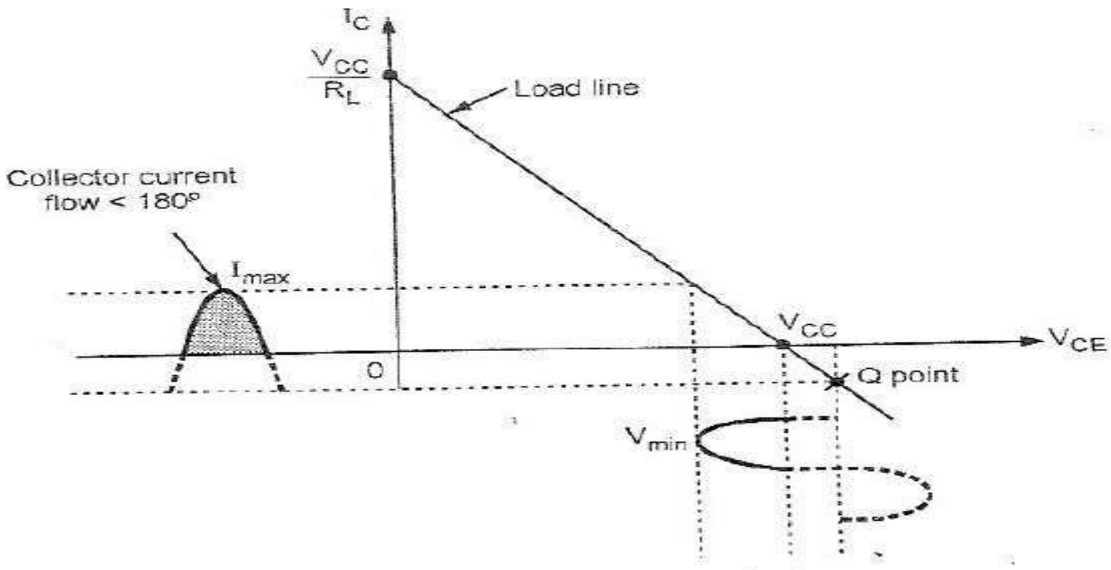


Fig. 3.26 Waveform representing class C operation

Fig 3.27 shows the class C tuned amplifier. Here a parallel resonant circuit as load impedance. As collector current flows for less than half a cycle, the collector current consists of a series of pulses with the harmonics of the input signal. A parallel tuned circuit acting as load impedance is tuned to the input frequency. Therefore, it filters the harmonic frequencies and produces a sine wave output voltage consisting of fundamental component of the input signal.

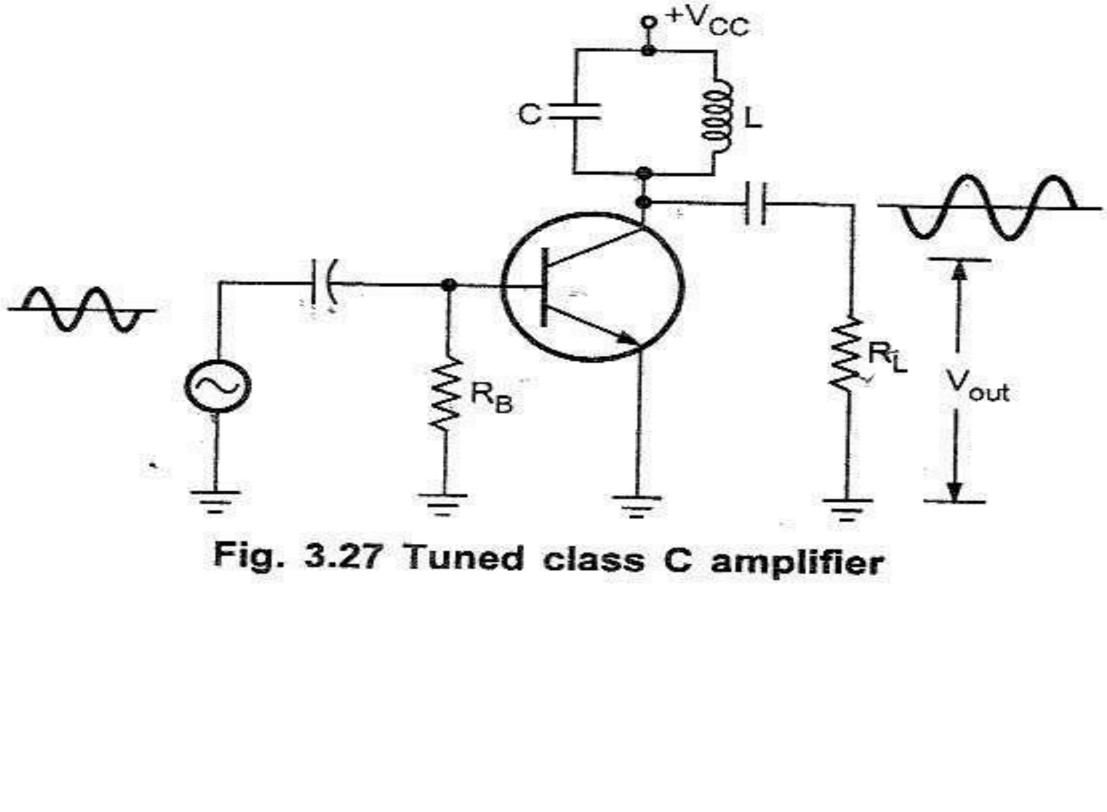


Fig. 3.27 Tuned class C amplifier

A class C tuned amplifier can be used as a frequency multiplier if the resonant circuit is tuned to a harmonic of the input signal.

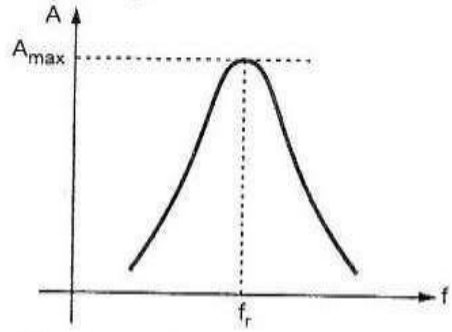


Fig. 3.28 Frequency response

Resonant frequency

Here, class C amplifier is used with parallel tuned circuit. Therefore, the output voltage is maximum at the resonant frequency. The resonant frequency for parallel tuned circuit is given as,

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad \dots (1)$$

Power gain

Power gain is defined as,

$$G = \frac{P_{out}}{P_{in}} \quad \dots (2)$$

In words, the power gain equals the a.c. output power divided by the a.c. input power.

Output power

If we measure the output voltage of Fig. 3.27 in r.m.s. volts, the output power is given by

$$P_{out} = \frac{V_{rms}^2}{R_L} \quad \dots (3)$$

Usually we measure the output voltage in peak to peak volts (V_{pp}) with an oscilloscope and

$$V_{pp} = 2\sqrt{2}\, V_{rms}$$

$$\therefore \quad V_{rms} = \frac{V_{pp}}{2\sqrt{2}}$$

Substituting value of V_{rms} we get,

$$P_{out} = \frac{\left(V_{pp} / 2\sqrt{2}\right)^2}{R_L} = \frac{V_{pp}^2}{8R_L} \quad \dots (4)$$

A.C. collector resistance

Any inductor has a series resistance R, as indicated in Fig. 3.29. The Q of the inductor is defined as,

$$Q_L = \frac{X_L}{R} = \frac{\omega_r L}{R} \quad \dots (5)$$

where Q_L = Quality factor of coil

X_L = Inductive reactance

R = Coil resistance

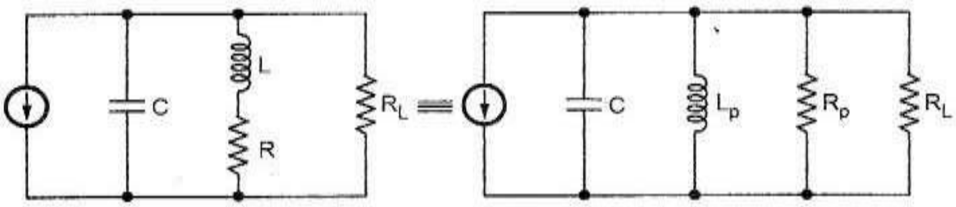


Fig. 3.29

As shown in the Fig. 3.29, the series resistance of the coil can be replaced by a parallel resistance R_p. This equivalent parallel resistance can be given as,

$$R_p = Q_L \omega_r L \quad \dots (6)$$

At resonance, X_L cancels X_C, leaving only R_p in parallel with R_L. Therefore, the a.c. resistance seen by the collector at resonance is :

$$r_c = R_p \parallel R_L \quad \dots (7)$$

∴ Q of the overall circuit is given by,

$$Q = \frac{r_c}{\omega_r L} \quad \dots (8)$$

Transistor power dissipation

Fig. 3.30 shows the ideal collector-emitter voltage in a class C transistor amplifier. In Fig. 3.30, the maximum output is given by,

$$V_{pp\,(max)} = 2\,V_{CC} \quad \dots (9)$$

Since the maximum voltage is approximately 2 V_{CC}, the transistor must have V_{CEO} rating greater than 2 V_{CC}.

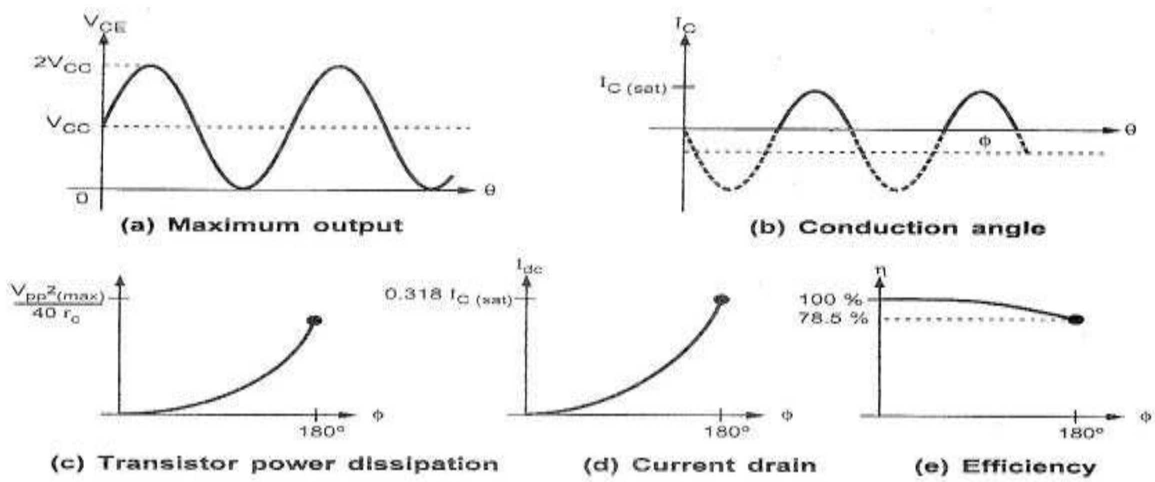


Fig. 3.30

Fig. 3.30 (b) shows the collector current for a class C amplifier. Typically, the conduction angle ϕ is much less than 180°. The power dissipation of the transistor depends on the conduction angle. It increases when conduction angle increases as shown in Fig. 3.30 (c). The maximum power dissipation for class C amplifier can be given as,

$$P_{D\,max} = \frac{V^2_{pp(max)}}{40 r_c} \quad \dots (10)$$

where r_c = A.C. collector resistance

Under normal condition, conduction angle will be less than 180° and the transistor power dissipation will be less than $V^2_{pp(max)}/40\ r_c$. But considering worst case condition, transistor power rating must be greater than $P_{D\,max}$.

D.C. input power

D.C. input power can be given as,

$$P_{dc} = V_{CC}\, I_{dc} \quad \dots (11)$$

Efficiency

The efficiency of the amplifier is given as

$$\eta = \frac{P_{out}}{P_{dc}} \times 100\ \% = \frac{P_{out}}{V_{CC} \times I_{dc}} \times 100\ \% \quad \dots (12)$$

The d.c. collector current depends on the conduction angle for a conduction angle of 180° (a half-wave signal), the average or d.c. collector current is $I_{C\,(sat)}/\pi$. For smaller conduction angles, the d.c. collector current is less than this, as shown in Fig. 3.30 (d).

In a class C amplifier, most of the d.c. input power is converted into a.c. load power because the transistor and coil losses are small. When the conduction angle is 180°, the efficiency is 78.5 %. The efficiency increases when conduction angle decreases. As indicated class C amplifier has maximum efficiency of 100 %, approached at very small conduction angles.

Bandwidth

We know that, bandwidth of resonant circuit is defined as

$$BW = f_2 - f_1$$

where f_1 = Lower half power (3 dB) frequency

f_2 = Upper half power (3 dB) frequency

The half power frequencies are identical to the frequencies at which the voltage gain equal 0.707 times the maximum gain.

The bandwidth of the class C tuned amplifier is given as,

$$BW = \frac{f_r}{Q} \quad \dots (13)$$

where Q is the quality factor of the circuit,

Example 3.7 : *A class C tuned amplifier has inductance of 3 μH and capacitance of 470 pF in the tank circuit. Calculate the resonant frequency.*

Solution : We know that,

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{3\ \mu H \times 470\ pF}} = \mathbf{4.238\ MHz}$$

Now we will discuss a few equations that are useful in the analysis of class C amplifier.

Example 3.8 : *For the circuit shown in Fig. 3.31, calculate resonant frequency, ac collector resistance, quality factor and bandwidth. Assume $Q_L = 100$.*

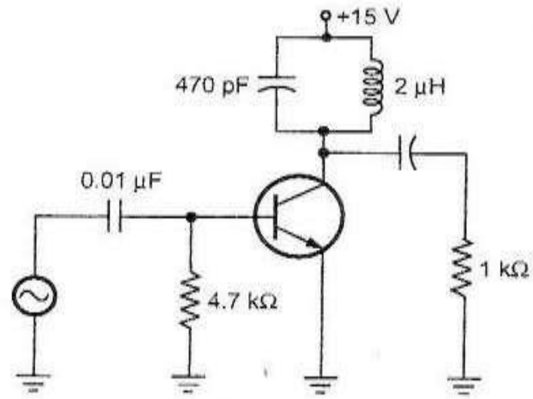


Fig. 3.31

Solution : i) Resonant frequency

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{2\ \mu H \times 470\ pF}} = \mathbf{5.19\ MHz}$$

ii) A.C. collector resistance is given as,

$$\begin{aligned} r_c &= R_p \parallel R_L = Q_L\,\omega_r\,L \parallel R_L \\ &= (Q_L\,2\pi f_r L) \parallel R_L \\ &= (100 \times 2\pi \times 5.19 \times 10^6 \times 2\,\mu H) \parallel 1\ k\Omega \\ &= 6.52\ k\Omega \parallel 1\ k\Omega = \mathbf{867\ \Omega} \end{aligned}$$

iii) Quality factor of the overall circuit is given as,

$$Q = \frac{r_c}{\omega_r L} = \frac{r_c}{2\pi f_r L}$$

$$= \frac{867}{2\pi \times 5.19 \times 10^6 \times 2 \times 10^{-6}} = \mathbf{13.29}$$

iv) Bandwidth is given as,

$$BW = \frac{f_r}{Q} = \frac{5.19 \times 10^6}{13.29} = \mathbf{390.5\ kHz}$$

Example 3.9 : *For the circuit shown in example 3.8, what is the worst case power dissipation?*

Solution : The maximum peak to peak output is given as,

$$V_{pp(max)} = 2V_{CC} = 2 \times 15 = \mathbf{30\ V}$$

The worst case power dissipation (maximum power dissipation) of the transistor is given as,

$$P_{D(max)} = \frac{V_{pp}^2}{40 r_c} = \frac{30^2}{40 \times 867} = \mathbf{26\ mW}$$

Example 3.10 : *For the circuit shown in Fig. 3.32, calculate*

i) Output power if the output voltage is 50 V_{pp}.

ii) Maximum ac output power.

iii) D.C. input power if current drain is 0.5 mA.

iv) Efficiency if the current drain is 0.4 mA and the output voltage is 30 V_{pp} .

v) Bandwidth of amplifier if Q = 125.

vi) Worst case transistor power dissipation.

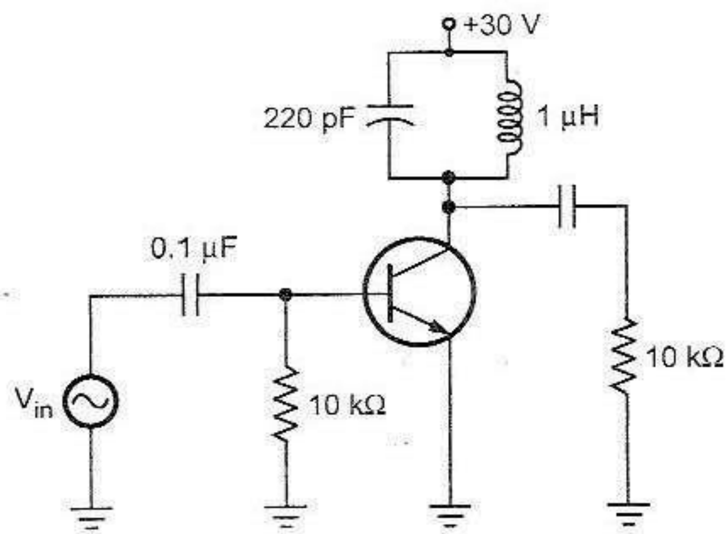


Fig. 3.32

Solution : i) The output power of amplifier is given as

$$P_{out} = \frac{(V_{out})^2}{8\,R_L}$$

$$= \frac{(V_{pp})^2}{8R_L} = \frac{(50)^2}{8\times10\,K} = \mathbf{31.25\ mW}$$

ii) Maximum a.c. output power is given as,

$$P_{ac(max)} = \frac{\left(V_{pp(max)}\right)^2}{8R_L} = \frac{(2\times V_{CC})^2}{8R_L}$$

$$= \frac{(60)^2}{8\times10\,K} = \mathbf{45\ mW}$$

iii) D.C. input power is given as,

$$P_{dc} = V_{CC}\times I_{dc}$$

$$= 30\times0.5\,mA = \mathbf{15\ mW}$$

iv) Efficiency is given as,

$$\eta = \frac{P_{out}}{P_{dc}}\times100$$

Given : I_{dc} = 0.4 mA, $V_{out} = V_{pp}$ = 30 V

$$= \frac{\left(\frac{V_{pp}{}^2}{8R_L}\right)}{V_{CC}\ I_{dc}}\times100 = \frac{\frac{30^2}{8\times10\,K}}{30\times0.4\,mA}\times100 = \mathbf{93.75\ \%}$$

v) Bandwidth of the amplifier is given as,

$$BW = \frac{f_r}{Q}$$

where
$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{1\ \mu H \times 220\ pF}} = \mathbf{10.73\ MHz}$$

$$\therefore \quad BW = \frac{10.73}{125} = \mathbf{85.84\ kHz}$$

vi) Worst case transistor power dissipation is given as,

$$P_{D(max)} = \frac{\left(V_{pp(max)}\right)^2}{40 r_c}$$

where
$$r_c = R_p \parallel R_L$$

$$= Q_L\ \omega_r\ L \parallel R_L$$

$$= \left(125 \times 2\pi \times 10.73 \times 10^6 \times 1 \times 10^{-6}\right) \parallel 10 \times 10^3$$

$$= 8427.3 \parallel 10 \times 10^3 = 4573.27\Omega$$

$$\therefore \quad P_{D(max)} = \frac{(2 \times 30)^2}{40 \times 4573.27} = \mathbf{19.68\ mW}$$

Example 3.11 : *If class C tuned amplifier has R_L = 6 kΩ and required tank circuit Q = 80. Calculate the values of L and C of the tank circuit. Assume V_{CC} = 20 V, resonant frequency = 5 MHz and worst case power dissipation = 20 mW.*

Solution : We know that,

$$P_{D\,max} = \frac{\left(V_{pp\,max}\right)^2}{40\ r_c} = \frac{\left(2\ V_{CC}\right)^2}{40\ r_c}$$

$$\therefore \quad r_c = \frac{\left(2\ V_{CC}\right)^2}{40 \times P_{D\,max}}$$

$$= \frac{(2 \times 20)^2}{40 \times 20\ mW} = \mathbf{2\ k\Omega}$$

We know that

$$r_c = R_p \parallel R_L$$

$$\therefore \quad \frac{1}{R_p} = \frac{1}{r_c} - \frac{1}{R_L}$$

$$= \frac{1}{2\,K} - \frac{1}{6\,K}$$

$$= 3.33 \times 10^{-4}$$

$$\therefore \quad R_p = \mathbf{3\ k\Omega}$$

We know that,

$$R_p = Q_L \times \omega_r \times L$$

$$= Q_L \times 2\pi \times f_r \times L$$

$$\therefore \quad L = \frac{R_p}{Q_L \times 2\pi \times f_r}$$

$$= \frac{3000}{80 \times 2\pi \times 5 \times 10^6} = \mathbf{1.19\ \mu H}$$

We know that

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$\therefore \quad C = \frac{1}{(2\pi)^2\, L\, f_r^2}$$

$$= \frac{1}{(2\pi)^2 \times 1.19 \times 10^{-6} \times (5 \times 10^6)^2} = \mathbf{851\ pF}$$

3.9.3 Application of Class C Tuned Amplifier

As an application of tuned amplifier we see the mixer or frequency converter circuit. Frequency conversion is the process of translating a modulated signal to a higher or lower frequency while still retaining all the originally transmitted information. Although modulation itself is a form of frequency translation, frequency conversion is often used before and after transmission or reception to provide some benefit.

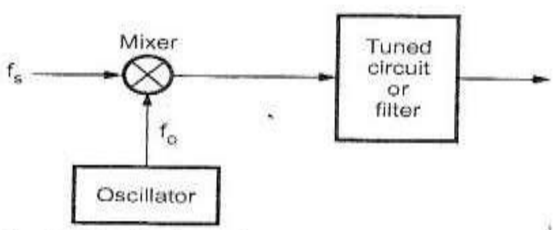


Fig. 3.33 Block schematic of mixer circuit

Frequency conversion is a form of AM. It is carried out by a mixer circuit. In some applications, the mixer is referred to as a converter. The function performed by the mixer is called heterodyning.

Fig. 3.33 shows the block schematic of mixer circuit. The mixer accepts two inputs : The signal f_s which is to be translated to another frequency and sine wave from the oscillator, f_o. The mixer, like an amplitude modulator, performs a mathematical multiplication of its two input signals and produces output signals : f_s , f_o , $f_o + f_s$ and $f_s - f_o$. Only one of these signals is the desired one. A tuned circuit or filter is normally used at the output of the mixer to select the desired signal.

The Fig. 3.34 shows the mixer circuit using class C tuned amplifier. Here, transistor is biased to operate as a class C amplifier so that the collector current does not vary linearly with variations in the base current. This results in analog multiplication which produces the sum and difference frequencies. As shown in the Fig. 3.34, both the incoming signal and oscillator signal are applied to the base of the transistor. The tuned circuit selects the sum or difference frequency.

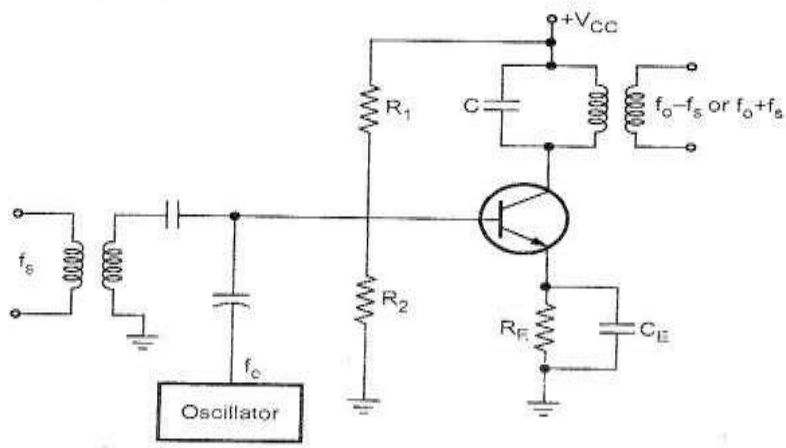


Fig. 3.34 Mixer circuit using class C turned amplifier

Applications of mixer or converter circuits

1. One of the most common applications for mixer is in radio receivers. The mixer is used to convert incoming signal to a lower frequency where it is easier to obtain the high gain and selectivity required.
2. Mixer circuits are used to translate signal frequency to some lower frequency or to some higher frequency. When it is used to translate signal to lower frequency it is called down converter. When it is used to translate signal to higher frequency, it is called up converter.

3.10 Stability of Tuned Amplifiers

In tuned RF amplifiers, transistors are used at the frequencies nearer to their unity gain bandwidths (i.e. f_T), to amplify a narrow band of high frequencies centred around a radio frequency. At this frequency, the inter junction capacitance between base and collector, C_{bc} of the transistor becomes dominant, i.e. its reactance becomes low enough to be considered, which is otherwise infinite to be neglected as open circuit. Being CE configuration capacitance C_{bc}, shown in the Fig. 3.35 come across input and output circuits of an amplifier. As reactance of C_{bc} at RF is low enough it provides the feedback path from collector to base. With this circuit condition, if some feedback signal manages to reach the input from output in a positive manner with proper phase shift, then there is possibility of circuit converted to an unstable one, generating its own oscillations and can stop working as an amplifier. This circuit will always oscillate if enough energy is fed back from the collector to the base in the correct phase to overcome circuit losses. Unfortunately, the conditions for best gain and selectivity are also those which promote oscillation. In order to prevent oscillations in tuned RF amplifiers it was necessary to reduce the stage gain to a level that ensured circuit stability. This could be accomplished in several ways such as lowering the Q of tune circuits; stagger tuning, loose coupling

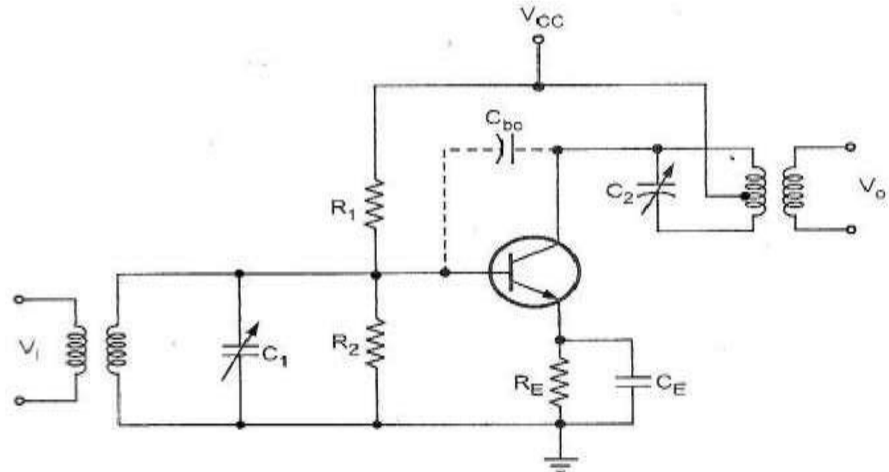


Fig. 3.35 Tuned RF stage

between the stages or inserting a 'loser' element into the circuit. While all these methods reduced gain, detuning and Q reduction had detrimental effects on selectivity. Instead of loosing the circuit performance to achieve stability, the professor L.A. Hazeltine introduced a circuit in which the troublesome effect of the collector to base capacitance of the transistor was neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance. He proved that the neutralization can be achieved by deliberately feding back a portion of the output signal to the input in such a way that it has the same amplitude as the unwanted feedback but the opposite phase. Later on many neutralizing circuits were introduced. Let us study some of these circuits.

3.10.1 Hazeltine Nèutralization

The Fig. 3.36 shows one variation of the Hazeltine circuit. In this circuit a small value of variable capacitance C_N is connected from the bottom of coil, point B, to the base. Therefore, the internal capacitance C_{bc}, shown dotted, feeds a signal from the top end of the coil, point A, to the transistor base and the C_N feeds a signal of equal magnitude but opposite polarity from the bottom of coil, point B, to the base. The neutralizing capacitor, C_N, can be adjusted correctly to completely nullify the signal fed through the C_{bc}.

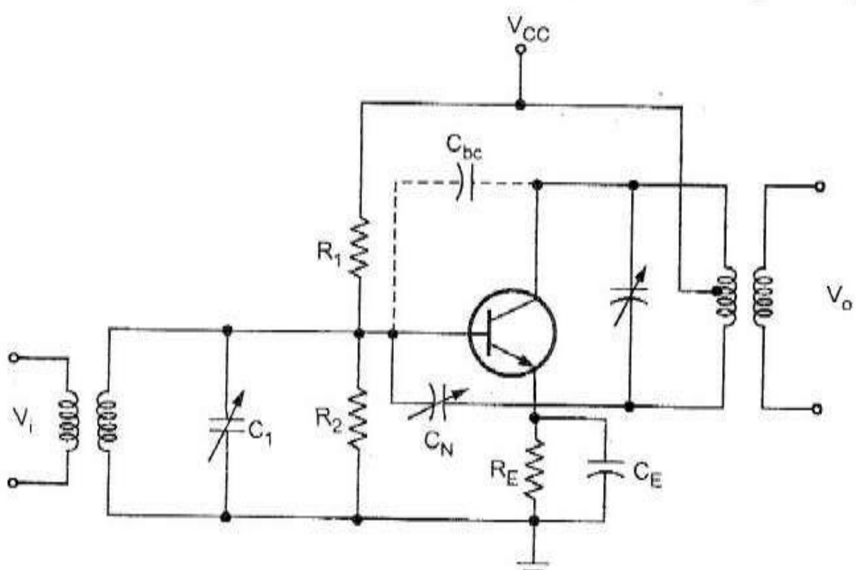


Fig. 3.36 Tuned RF amplifier with Hazeltine neutralization

3.10.2 Neutrodyne Neutralization

The Fig. 3.37 shows typical neutrodyne circuit. In this circuit the neutralization capacitor is connected from the lower end of the base coil of the next stage to the base of the transistor.

In principle, this circuit functions in the same manner as the Hazeltine neutralization circuit with the advantage that the neutralizing capacitor does not have the supply voltage across it.

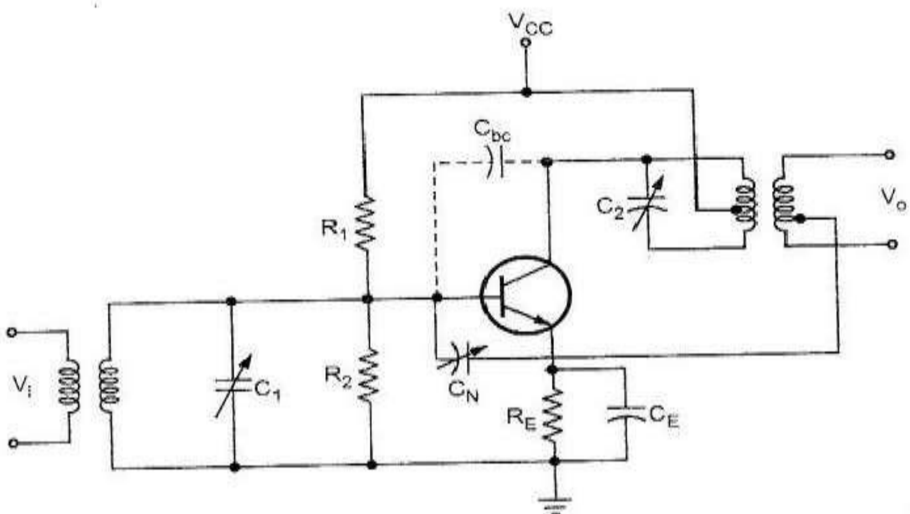


Fig. 3.37 Tuned RF amplifier with Neutrodyne neutralization

3.10.3 Neutralization using Coil

The Fig. 3.38 shows the neutralization of RF amplifier using coil. In this circuit, L part of the tuned circuit at the base of next stage is oriented for minimum coupling to the other windings. It is wound on a separate form and is mounted at right angles to the coupled windings. If the windings are properly polarized, the voltage across L due to the circulating current in the base circuit will have the proper phase to cancel the signal coupled through the base to collector, C_{bc} capacitance.

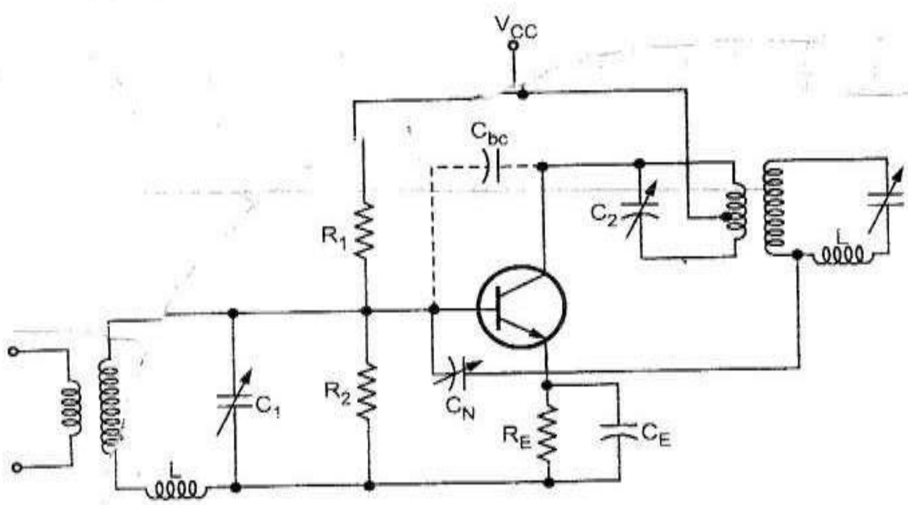


Fig. 3.38 Tuned RF amplifier using coil

3.10.4 Rice Neutralization

The Fig. 3.39 shows the Rice circuit of neutralization. It uses a centre tapped coil in the base circuit. With this arrangement the signal voltages at the ends of the tuned base coil are equal and out of phase.

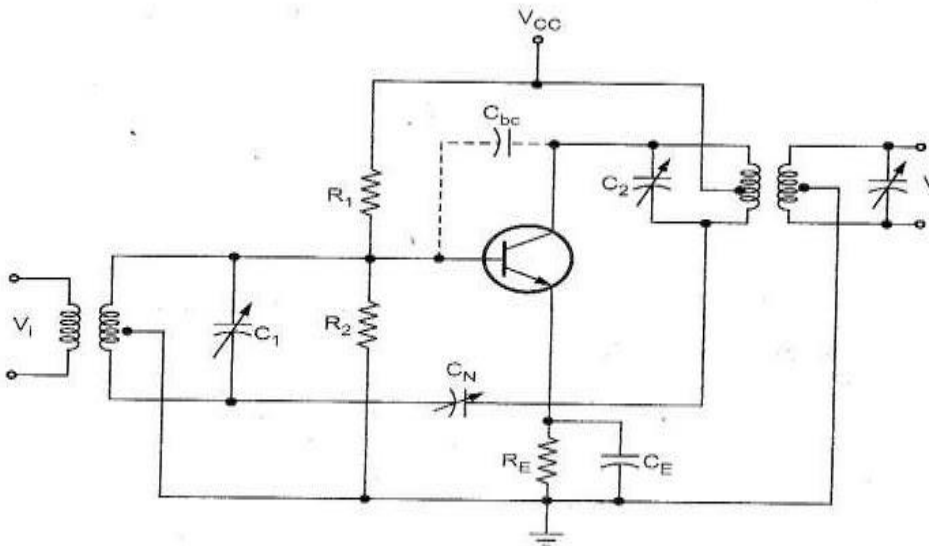


Fig. 3.39 Tuned RF amplifier using Rice neutralization

3.11 Advantages and Disadvantages of Tuned Amplifiers

Advantages :

1) They amplify defined frequencies.
2) Signal to noise ratio at output is good.
3) They are well suited for radio transmitters and receivers.
4) The band of frequencies over which amplification is required can be varied.

Disadvantages :

1) Since they use inductors and capacitors as tuning elements, the circuit is bulky and costly.
2) If the band of frequency is increased, design becomes complex.
3) They are not suitable to amplify audio frequencies.

3.12 Applications of Tuned Amplifiers

The important applications of tuned amplifiers are as follows :

1. Tuned amplifiers are used in radio receivers to amplify a particular band of frequencies for which the radio receiver is tuned.
2. Tuned class B and class C amplifiers are used as an output RF amplifiers in radio transmitters to increase the output efficiency and to reduce the harmonics.
3. Tuned amplifiers are used in active filters such as low pass, high pass and band pass to allow amplification of signal only in the desired narrow band.

TUTORIAL QUESTION BANK

ELECTRONIC CIRCUIT ANALYSIS

UNIT-I: SINGLE STAGE AND MULTISTAGE AMPLIFIERS

2 MARKS QUESTIONS:

1. List the classification of amplifiers
2. List the classification of amplifiers based on frequency of operation
3. What is the effect of bypass capacitor?
4. What is the phase shift between input and output of a CE Amplifier?
5. What is the effect of coupling capacitor?
6. Draw the frequency response of BJT amplifier.
7. What is a multistage amplifier?
8. Identify different types of couplings used in amplifiers.
9. Write the advantages of multistage amplifiers?
10. Draw the circuit of Transformer coupled amplifier?
11. What is cascade amplifier? Write its advantages?
12. Write the advantages of transformer coupling?
13. List out the applications of cascade amplifier?

10 MARKS QUESTIONS:

1. Explain the effect of coupling and bypass capacitors on amplifier at low frequencies.
2. Explain the different types of couplings. When two identical stages are cascaded obtain the voltage gain, current gain and power gain.
3. Draw the circuit of common collector amplifier and explain its characteristics.
4. Draw and explain the circuit of cascade amplifier and mention its advantages.
5. Explain RC Coupled CE transistor stages and derive the expression for gain.
6. With a neat diagram analyze Darlington pair amplifier.
7. Explain the operation of direct and transformer coupled amplifiers.
8. Draw the circuit diagram of two stage RC coupled amplifier. Explain the operation and calculate the mid frequency range and low frequency range.
9. Design a single stage emitter follower having R_i=500KΩ and R_o=20Ω. Assume h_{fe}=50, h_{ie}=1KΩ, h_{oe}=25µA/V.
10. Discuss the classification of amplifiers based on frequency range and type of coupling, power delivered and signals handled.

UNIT-II: HIGH FREQUENCY RESPONSE OF TRANSISTOR

2 MARKS QUESTIONS:

1. State Miller's theorem.
2. What is the relationship between f_T and f_β? Discuss the significance of f_T.
3. Draw simplified high frequency model of CE amplifier.
4. Write the hybrid-π conductance equations of common emitter transistor.
5. How does gm and C_e vary with $|I_C|$, V_{CE} and T.
6. Define the gain bandwidth product of common emitter amplifier in terms of high frequency parameters.

7. Show that in Hybrid – π model, the diffusion capacitance is proportional to the emitter bias current.
8. Define fβ, f_T and f_{α}.
9. Write the expression for upper 3-dB frequency of a single stage CE amplifier.
10. Define hybrid –π parameters.
11. Write the expression for current gain for a CE amplifier with resistive load.
12. Write the expression for hybrid π model parameters g_m, g_{ce} and r_{ce}.

10 MARKS QUESTIONS:

1. Explain about hybrid π capacitances and briefly discuss miller's theorem.
2. Derive the expressions for hybrid π model parameters g_m, g_{ce} and r_{ce}.
3. Explain why the 3-dB frequency for current gain is not the same as f_H for voltage gain.
4. Derive the expression for the CE short-circuits current gain Ai with resistive load.
5. Draw the hybrid-π equivalent of a CE transistor valid for high frequency and explain the significance of each parameter.
6. Prove that (i) $h_{fe}=g_m * r_{b'e}$ for a Hybrid -π model of CE amplifier.
7. How does a C_e and C_c vary with | I_c | and | V_{CE} |.
8. How does gm vary with | I_c | and | V_{CE} |, T.

UNIT-III: FEEDBACK AMPLIFIERS AND OSCILLATORS

2 MARKS QUESTIONS:

1. What is feedback and what are feedback amplifiers.
2. What is the condition of generating oscillations?
3. What is meant by positive and negative feedback.
4. What are the advantages and disadvantages of negative feedback.
5. Mention different types of negative feedback amplifiers.
6. What is Barkhausen criterion
7. What is Oscillator circuit and classify different types.
8. Define Piezo-electric effect.
9. Draw the equivalent circuit of crystal oscillator.
10. State the frequency for RC phase shift oscillator
11. What is the minimum value of hfe for the oscillations in transistorized RC Phase shift oscillator.
12. What is the frequency of LC oscillator and classify LC oscillators.

10 MARKS QUESTIONS:

1. Draw the circuit diagram of voltage series feedback amplifier and derive the expressions for A_v, R_i and R_o.
2. Draw the circuit diagram of voltage shunt feedback amplifier and derive the expressions for A_v, R_i and R_o.
3. Draw the circuit diagram of current series feedback amplifier and derive the expressions for A_v, R_i and R_o.
4. Draw the circuit diagram of current shunt feedback amplifier and derive the expressions for A_v, R_i and R_o.
5. Write the advantages of positive and negative feedback amplifiers.
6. Explain the basic principle of generation of oscillations in LC tank circuits. What are the

considerations to be made in the case of practical L.C. Oscillator Circuits?

7. Draw the circuit and explain the principle of operation of RC phase-shift oscillator circuit. What is the frequency range of generation of oscillations? Derive the expression for the frequency of oscillations.
8. Draw the basic circuit of LC oscillator and derive the expression for condition of oscillations.
9. Discuss about the amplitude and frequency stability of oscillator.
10. Explain about crystal oscillator with a neat sketch.
11. Derive the expression for the frequency of Hartely oscillators.
12. Derive the expression for the frequency of Colpitts oscillators.
13. Derive the expression for the frequency of wien bridge oscillators.

UNIT-IV: POWER AMPLIFIERS

2 MARKS QUESTIONS:

1. Mention the efficiency of Class B Power amplifier.
2. Draw the circuit of Transformer coupled Class A Power amplifier.
3. Classify large signal amplifiers based on its operating point. Distinguish these amplifiers in terms of the conversion efficiency.
4. Derive the expression for the output current in push -pull amplifier with base current as ib = Ibm coswt.
5. What are the drawbacks of transformer coupled power amplifiers?
6. Define the conversion efficiency of class A Power amplifier.
7. State the advantages of push pull class B power amplifier over class B Power amplifier.
8. Compare various power amplifiers with respect to conduction angle, efficiency and distortion.
9. List the advantages of complementary-symmetry configuration over push pull configuration.
10. What is a harmonic distortion? How even harmonics is eliminated using push pull circuit.
11. Explain the different types of heat sinks.
12. Compare Class C and Class D power amplifiers.

10 MARKS QUESTIONS:

1. Compare various types of Power amplifiers.
2. Derive the expression for maximum collector power dissipation $P_{c\,(max)}$ of class B power amplifier.
3. What are the advantages and disadvantages of push pull power amplifier. Prove class B has maximum conversion efficiency of 78.5%.
4. Distinguish between small signal and large signal amplifiers. How are the power amplifiers classified? Describe their characteristics.
5. Derive the general expression for the output power in the case of a class A power amplifier. Draw the circuit and explain the movement of operating point on the load line for a given input signal.
6. Discuss the concept of Power transistor heat sinking.
7. Derive the expressions for maximum. Theoretical efficiency 'for
   (a) Transformer coupled and (b) Series fed amplifier. What are their advantages and disadvantages?

UNIT-V: TUNED AMPLIFIERS

2 MARKS QUESTIONS:

1. If 5-stages of single tuned amplifier are cascaded with each circuit resonant frequency of 25KHz. Find the overall band width.
2. Mention the salient features of tuned amplifiers.
3. Give the reasons why parallel resonance circuits are used in tuned amplifiers?
4. Write the expression for voltage gain for a capacitive coupled single tuned amplifier and also gain at resonance?
5. Classify tuned amplifier based on the input signal applied?
6. Define a tuned amplifier. State how its frequency response is different from an un tuned amplifier?
7. List out the applications of Tuned amplifiers.
8. Draw the capacitive coupled tuned amplifier.
9. What is staggered tuning.
10. What are the advantages of double tuning?

10 MARKS QUESTIONS:

1. What is a Tuned amplifier and explain the various methods of classification of tuned amplifiers.
2. Draw the circuit diagram of single tuned capacitive coupled amplifier and explain its operation and derive the expression for gain.
3. Derive the expression for 3db bandwidth of single tuned capacitive coupled amplifier
4. Derive the expression for Q factor of single tuned inductively coupled amplifier
5. Define Q factor and explain in detail the cascading of single tuned amplifiers on bandwidth.
6. Explain the operation and applications of Staggered Tuned amplifiers.
7. Derive the expression for 3db bandwidth in terms of Q factor and resonant frequency of double tuned capacitive coupled amplifier