UNIT I

LAQ'S

1. BASIC COMPUTER ORGANIZATION /BLOCK DIAGRAM/COMPUTER COMPONENTS
2. INSTRUCTION FORMAT BASED ON INTERNAL ORGANIZATION
    - Single accumulator organization.
    - General register organization.
    - Stack organization.
3. INSTRUCTION FORMATS (0,1,2,3 ADDRESS)
4. ADDRESSING MODES WITH NUMERIC EXAMPLES
5. WRITE SHORT NOTES ON SUBROUTINES

SAQ'S

1. FUNCTIONS OF CPU
2. CPU OPERATIONS
3. INPUT AND OUTPUT DEVICES
4. MEMORY(PRIMARY & SECONDARY)
5. TYPES OF RAMS
6. PROGRAM COUNTER(PC)
7. LIST OUT 4 FUNCTIONS OF CPU
8. ENLIST /LIST OUT PROGRAM CONTROL INSTRUCTIONS
9. WRITE SHORT NOTES /ENLIST CONDITONAL BRANCH INSTRUCTIONS
10. ENLIST SUBROUTINE INSTRUCTIONS/ENLIST STACK INSTRUCTIONS
11. WHAT IS INTERRUPT AND LIST OUT TYPES OF INTERRUPTS

UNIT II

LAQ'S

1. I/O BUS INTERFACE MODEULES WITH NEAT SKETCH
2. ISOLATED VERSUS MEMORY-MAPPED I/O
3. ASYNCHRONOUS DATA TRANSFER(STROBE AND HANDSHAKING)
4. write short notes on synchronous and asynchronous data transfer
5. Asynchronous Communication Interface(UART) with a block diagram
6. write short notes on MODES OF TRANSFER(LONG EACH AGAIN)
    - Programmed I/O
    - Interrupt-initiated I/O
    - Direct memory access (DMA) with block diagram
7. write short notes on DMA transfer
8. Input-output Processor (IOP)
9. INTEL 8089 IOP block diagram

SAQ'S

1. Input-output Processor (IOP)
2. synchronous and asynchronous data transfer
3. difference between peripheral and memory mapped IO
4. DMA

UNIT III

PS:for this unit preparation i request all the students to refer content from slides which i have shared in Google classroom(ID:isd25we)

LAQ'S

1. Memory Hierarchy (PYRAMID) TOP DOWN AND BOTTOM UP
2. Main Memory,
3. RAM, ROM Organization With Sketches
4. Memory Address Map
5. ASSOCIATIVE MEMORY
    - Definaton 2M
    - Uses 2M
    - Hardware Structure LAQ
    - Math Logic LAQ
    - Read And Write Operations LAQ
6. Write Short Notes On Cache Memory
7. Mapping Techniques With Examples(EACH ONE LAQ)
    - Associative Mapping
    - Direct Mapping
    - Set-Associative Mapping
8. Virtual Memory Organization
9. ADDRESS SPACE AND MEMORY SPACE

SAQ'S

1. Cache Organization Levels
2. Data Cache,
3. Instruction Cache,
4. Miss And Hit Ratio,
5. Access Time
6. Memory Connection To CPU

UNIT IV

1. 8086 CPU Pin Diagram LAQ
2. Special functions of general purpose registers 2M/5M
3. Segment register 2M/5M
4. concept of pipelining 2M
5. 8086 Flag register 2M/5M
6. Addressing modes of 8086 LAQ

UNIT V

1. 8086-Instructionsets LAQ
2. searching program 5M
3. sorting(ascending and descending)5M Each
4. evaluation of arithmetic expressions 2M

NOTE: all the students must and should read the questions marked in RED color to score good marks

**********ALL THE VERY BEST PREPARE WELL**********

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