**DDVL ASSIGNMENT-1**

1. What is module? What are the components of a module?
2. Explain the levels of abstuctions in verilog HDL.
3. What is instantiation?
4. Write a verilog HDL code for 4-bit parallel adder in structural modelling and also write its test bench.
5. Write a verilog HDL code for 4:1 mux in gate level modelling and also write its test bench.
6. Write a verilog HDL code for 3x8 decoder in gate level and dataflow modelling and also write its test benct.
7. Write a verilog HDL code for BCD adder in structural modelling.