

seq -10
 *moore fsm
state diagram*

verilog codes

```
module moore_10(a, clk, rst, y);
```

```
input a, clk, rst;
```

```
output y;
```

```
reg [1:0] state;
```

```
parameter A = a'b00,
```

```
B = a'b01,
```

```
C = a'b10;
```

```
always @ (posedge clk, posedge rst)
```

```
if (rst)
```

```
state <= A;
```

```
else
```

```
case(state)
```

```
A: if (a)
```

```
state <= B;
```

else

state \leftarrow A;

B: if (x)

state \leftarrow B;

else

state \leftarrow C;

C: if (x)

state \leftarrow B;

else

state \leftarrow A;

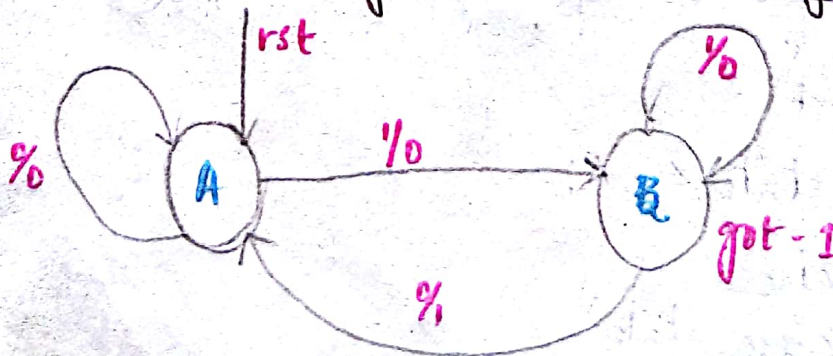
default: state \leftarrow A;

endcase

assign y = (state == C);

endmodule

* Mealy FSM state-diagram *



verilog code :

```
module mealy_10(x, clk, rst, y);  
input x, clk, rst;  
output y;  
reg y;  
reg state;  
parameter A = 1'b0,  
          B = 1'b1;  
always @ (posedge clk, posedge rst)  
if (rst)  
    state ← A;  
else  
    case (state)  
A: if (x)  
    begin  
        state ← B;  
        y ← 0;  
    end  
else  
    begin  
        state ← A;  
    end  
end  
end
```

$y \leftarrow 0;$

end.

B: if (x)

begin

state \leftarrow B;

$y \leftarrow 0;$

end

else

begin

state \leftarrow A;

$y \leftarrow 1;$

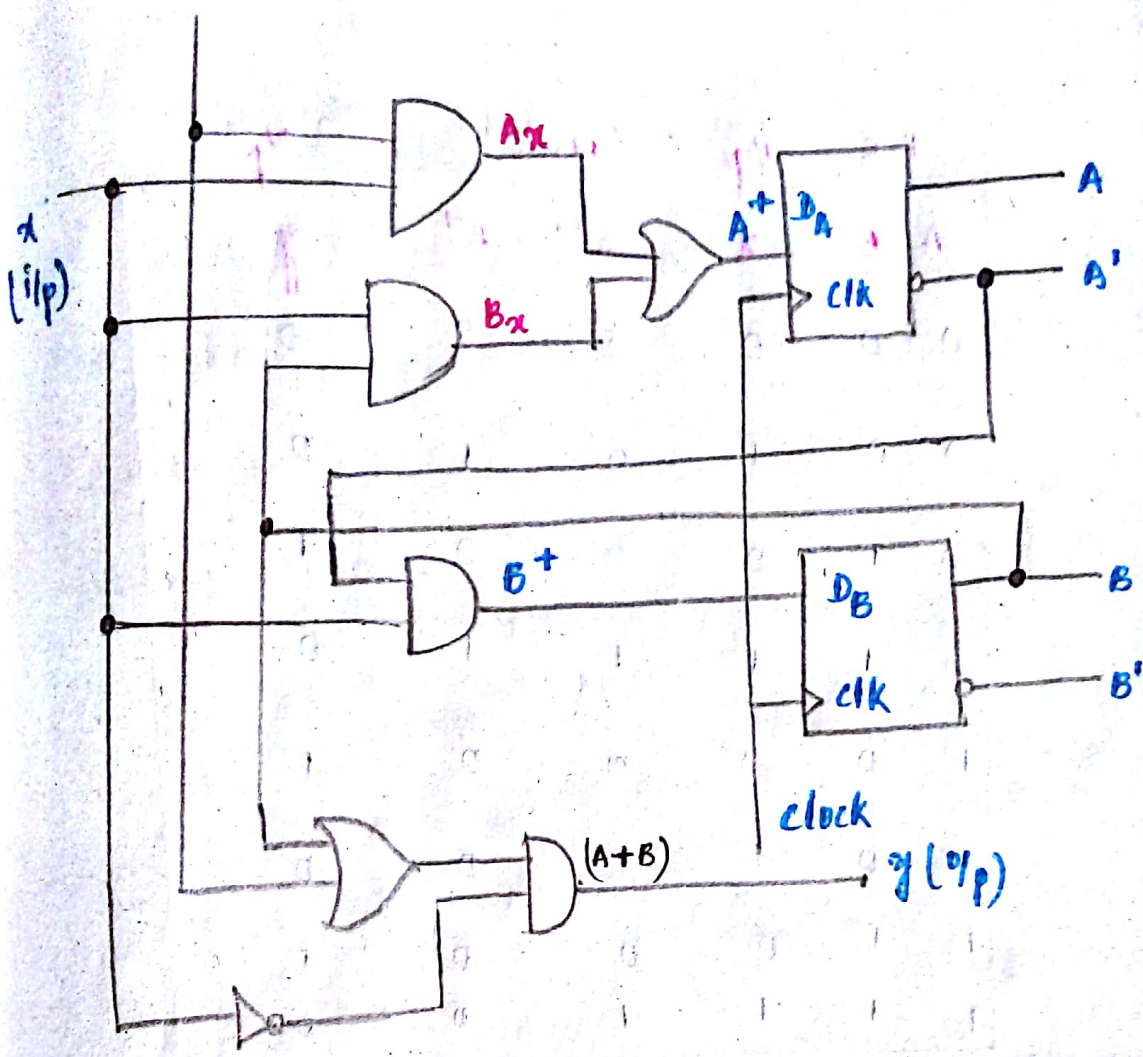
end

endcase

endmodule

* Analysis of clocked seq. circuit *
(synchronous. seq. circuit):

D-F/F !



where,

$A, B \longrightarrow$ P.S
 $A^+, B^+ \longrightarrow$ N.S

④ state eqⁿ and o/p eqⁿs :

Flip-Flop eqⁿs

$$D_A = A^+ = Ax + Bx \longrightarrow \text{state eqⁿs}$$

$$D_B = B^+ = \bar{A}x$$

o/p eqⁿ

$$y(o/p) = [A+B]\bar{x}$$

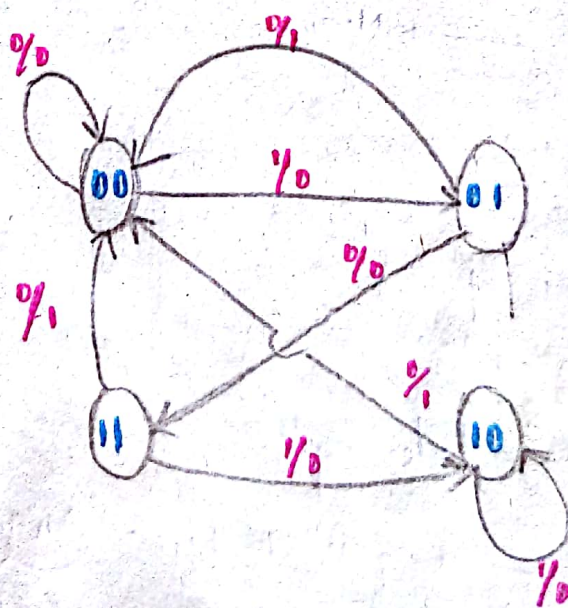
$$A^+ = D_A = Ax + Bx ; B^+ = D_B = \bar{A}x$$

for D-F/F, $Q_{n+1} = D$
 char. eq.

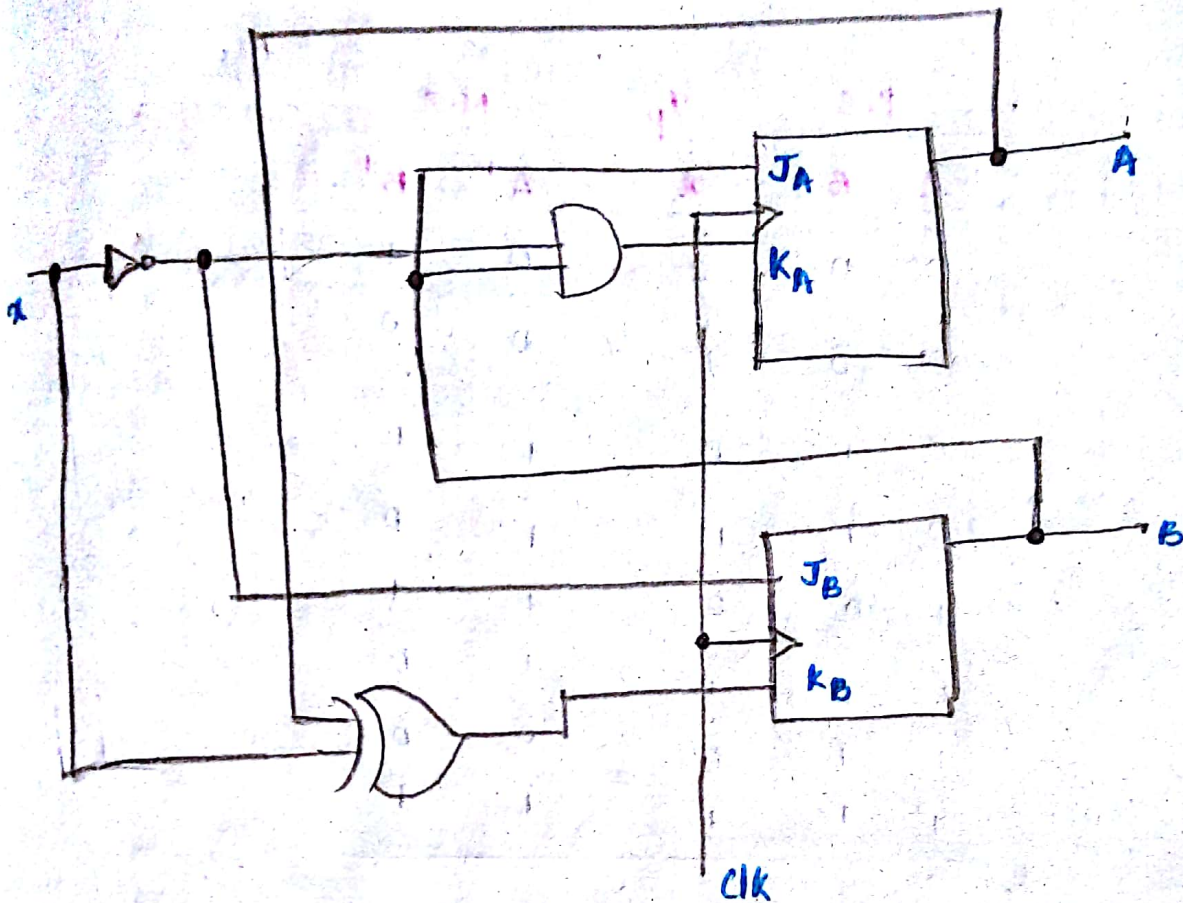
* state table :

P.S		i/p	N.S		o/p
A	B	x	A'	B'	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

* state diagram :



* Analysis with JK-FF *



④ Flip-Flop eqⁿ's :

$$J_A = B, \quad K_A = B\bar{x}$$

$$J_B = \bar{x}, \quad K_B = A \oplus x$$

④ state eqⁿ's and qp eqⁿ's :

$$(\because Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n)$$

$$A^+ = J_A \bar{A} + \bar{K}_A A = B\bar{A} + (\bar{B}x)A = \bar{A}B + A\bar{B} + Ax$$

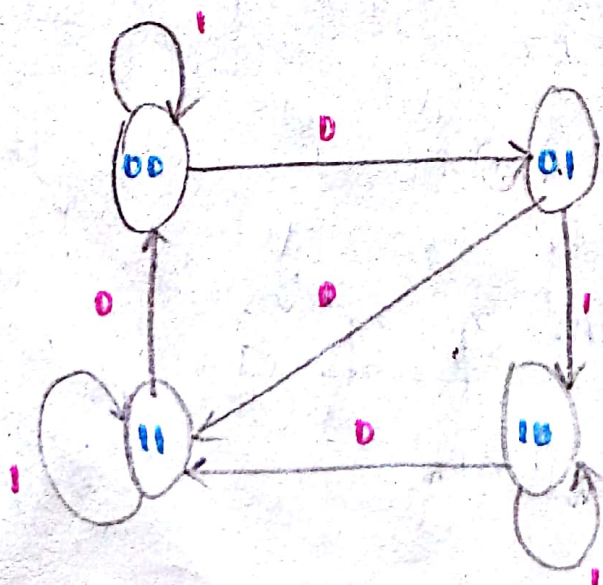
$$B^+ = J_B \bar{B} + \bar{K}_B B = \bar{x}\bar{B} + \overline{(A \oplus x)}B$$

$$= \bar{B}\bar{x} + ABx + \bar{A}B\bar{x}$$

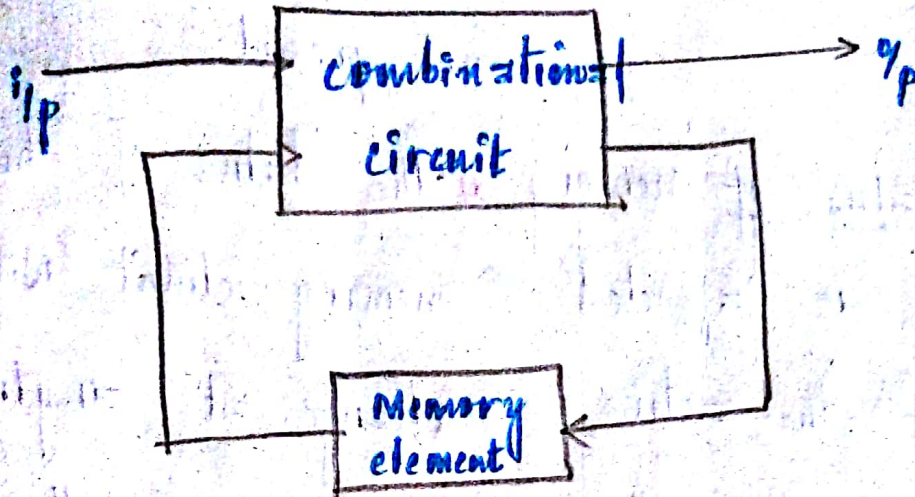
* state table :

P.S		i/p	N.S	
A	B		A ⁺	B ⁺
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

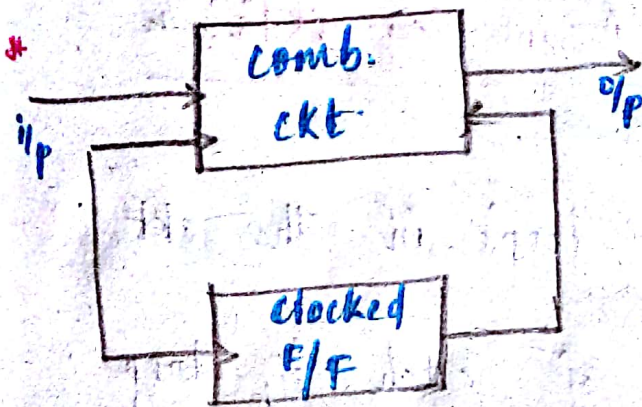
* state - diagram :



Seq. ckt. Block dia:



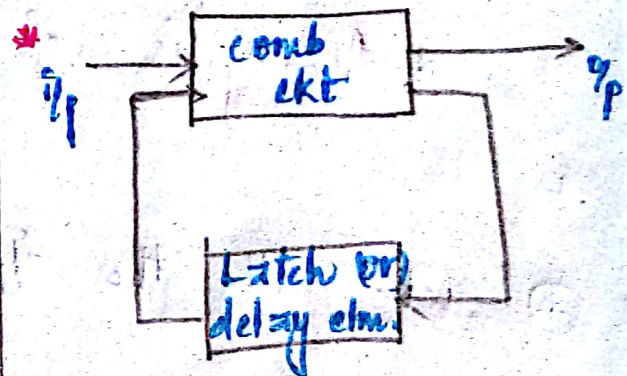
Syn: Seq ckt.



* These ckt's are easy to design

* A clocked F/F acts as a memory element.

Asyn seq ckt



* These ckt's are difficult to design

* Latch (or) time delay element is used as a memory elmt.

* These are slow.

* These are fast
as the clock is
not present.

* The status of memory
element is affected
only at the active
edge of clk, if the
i/p is changed.

* The status of the
memory element will
change at anytime
as soon as the
i/p is changed.

* Analysis of Asyn Seq ckt's: *

* Det. all the f/b loop's in the ckt

* Designate the o/p of each f/b loop
with var. (Y_i) and its corresponding
i/p with (X_i) for $i = 1 \dots k$ where,

$(k) \rightarrow$ no. of f/b loop's in the ckt.

* Derive the Boolean fun of all (y 's) as a fun of ext. ip's and (y 's).

* plot each y -fun in a map using y -var. for the row's and the ext. ip for column's.

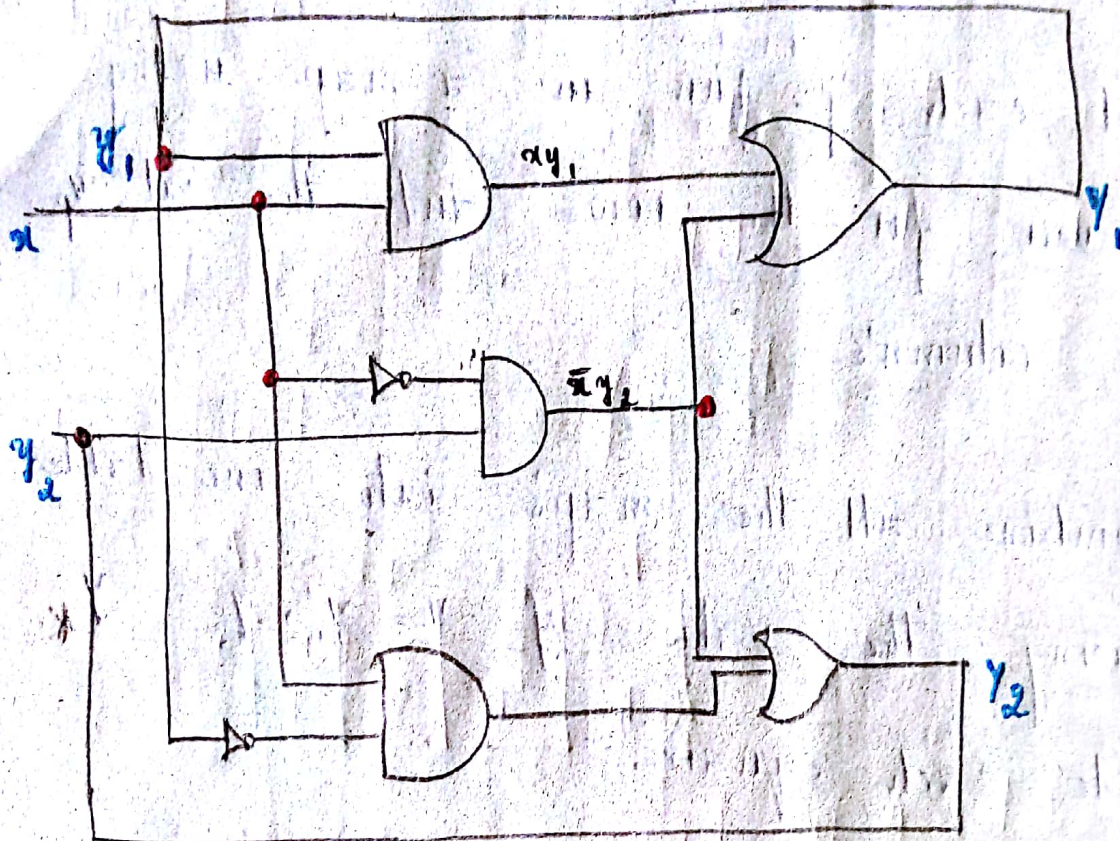
* Combine all the map's into one table showing the value of $y = y_1, y_2, \dots, y_k$ inside each square.

* Circle those value's of (y) in each square that are = the value of $y = y_1, y_2, \dots, y_k$ in the same row

* Draw the flow-table.

Example of an Asyn seq circuit:

-①



soln:

* There are 2 feed back loops.

$$* y_1 = xy_1 + \bar{y}_1 y_2$$

$$y_2 = xy_1 + \bar{y}_2 y_2$$

* k-map:

		y_1, y_2				
		00	01	11	10	
0	\bar{x}	0 ^a	1 ^b	1 ^c	0 ^d	→ y_1
1	x	0 ^e	0 ^f	1 ^g	0 ^h	

x	$y_1 y_2$	00	01	11	10
0		0 ¹	1 ⁴	1 ³	0 ²
1		1 ⁴	1 ⁵	0 ⁷	0 ⁶

→ y_2

Transition table:

- combining (y_1 and y_2) maps, we get the tr. table

x	$y_1 y_2$	00	01	11	10
0		00	11	11	00
1		01	01	10	10

(or)

- tr. table is obtained by combining the binary values in the corresponding maps of (y 's).

- Tr. table indicates the values of ...

$Y = y_1, y_2$ inside each square

- For a state to be stable, sec var must match the excitation table var

(i.e., the values of (y) must be same

as that of $\dots y = y_1, y_2 \dots$

* Flow Table:

- In a fn. table, if the states are named by letter symbols, then, it is called as a flow table.

x	y_1, y_2	a	b	c	d
0	a	a	c	c	a
1	b	b	d	d	d

- The flow table consists of 4 - states with one i/p

* primitive flow-table:

In a flow-table, if each row consists of only one stable state, then it is called as a primitive flow-table.

Example:

	$x_1 x_2$	00	01	11	10
a		a, 0	a, 0	a, 0	b, 0
b		a, 0	a, 0	b, 1	b, 0

→ a states with 2 i/p's and 1 o/p

Solⁿ:

	$x_1 x_2$	00	01	11	10
a		a	a	a	b
b		a	a	b	b

	$x_1 x_2$	00	01	11	10
a		0	0	0	0
b		0	0	1	0

	$x_1 x_2$	00	01	11	10
0		0	0	0	1
1		0	0	1	1

map for y:

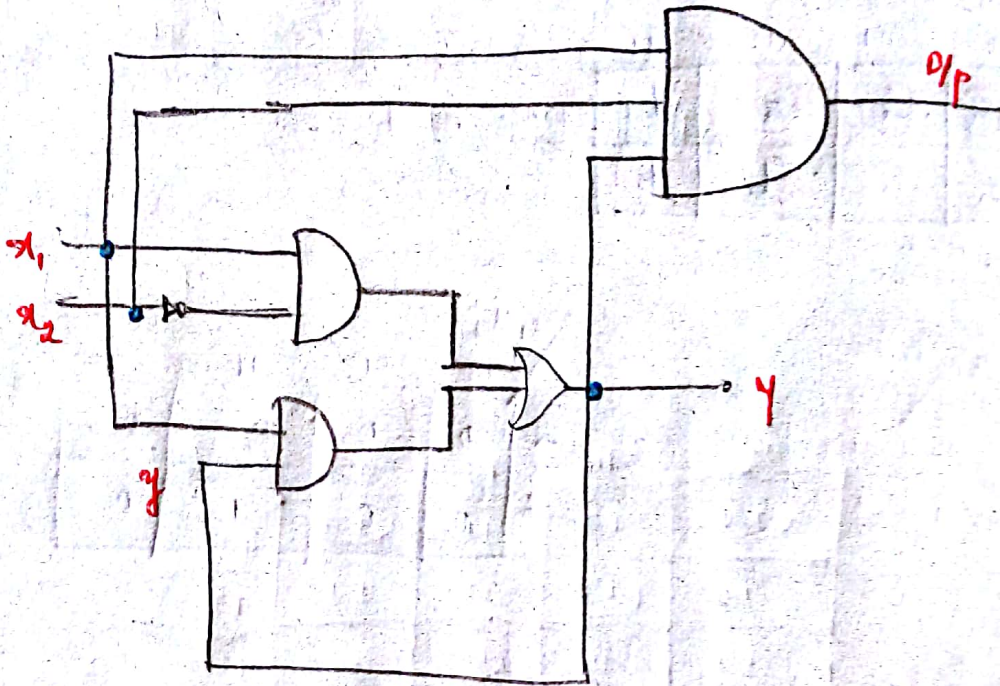
	$x_1 x_2$	00	01	11	10
0		0	0	0	0
1		0	0	1	0

map for o/p:

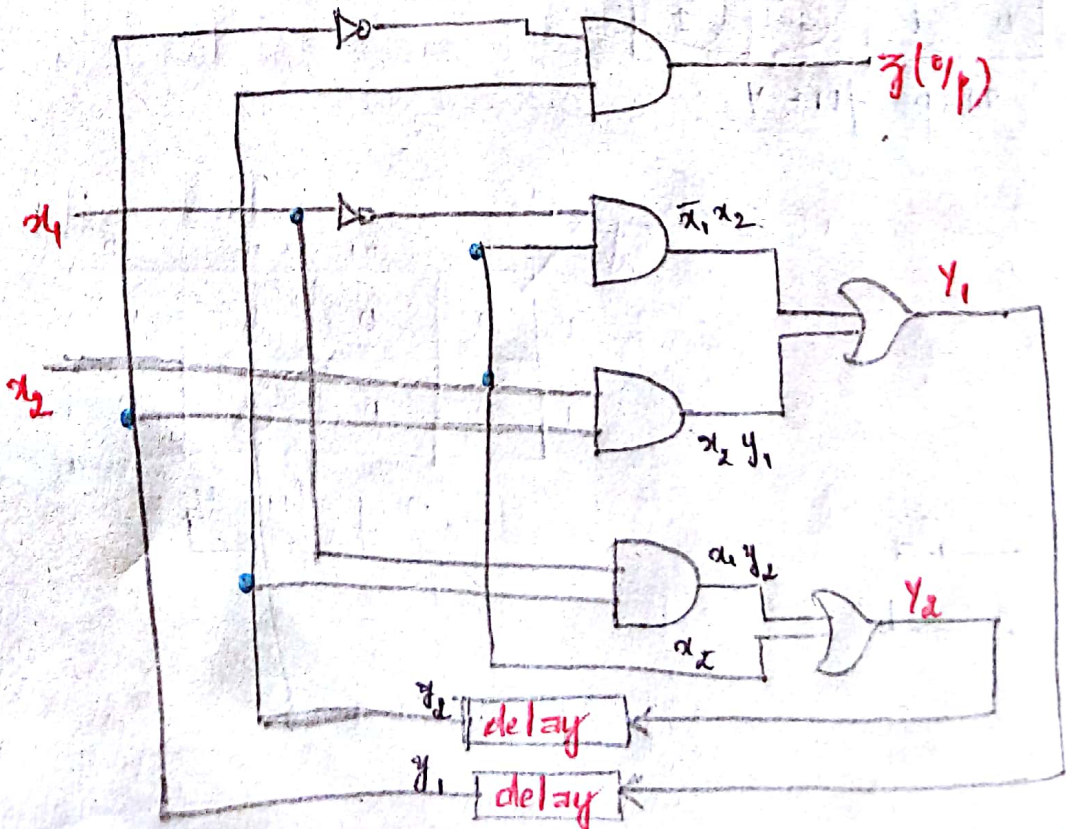
0 → a
1 → b

$$Y = x_1 y + x_1 \bar{x}_2$$

$$\text{output} = y \text{ } x_1 \text{ } x_n$$



Example - (3) :



④ Analyze the above asyn - seq ckt and obtain the s. table and timing dia:

Sol:

* no. of feed back's = 2

$$* Y_1 = \bar{x}_1 x_2 + x_2 y_1$$

$$Y_2 = x_1 y_2 + x_2$$

$$\bar{y} = \bar{y}_1 y_2$$

* K-map:

$y_1 y_2$	$x_1 x_2$ 00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	0	1	1	0
10	0	1	1	0

map for (Y_1)

$y_1 y_2$	$x_1 x_2$ 00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	0	1	1	1
10	0	1	1	0

map for (Y_2)

y_1, y_2 \ x_1, x_2	00	01	11	10
00	1	0	0	0
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

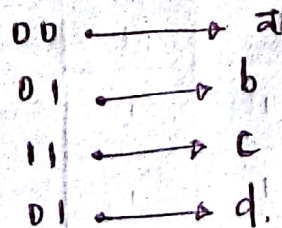
map - for $z(y)$

* In table:

y_1, y_2 \ x_1, x_2	00	01	11	10
00	00	11	01	00
01	00	11	01	01
11	00	11	11	01
10	00	11	11	00

0 led states are stable - states.

* Flow-table:



y_1, y_2 / x_1, x_2

	00	01	11	10
a	a	c	b	a
b	a	c	b	b
c	a	c	c	b
d	a	c	c	a

* state table:

P.S	00	01	11	10	%p
a	a	c	b	a	0
b	a	c	b	b	1
c	a	c	c	b	0
d	a	c	c	a	0