Electronic Devices and Circuits

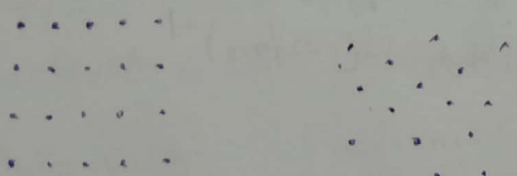
Structure of Solids:-

Solids are Crystaline in structure, It means that Solid Consists of atoms or molecules which are arranged in periodic manner. There is always some basic arrangement of atomes, which is repealed throughout the entire solid meterial. Arrangement of atoms within a solid is called crystal lattice. Such solids are Called Crystalline Solids.

But There are other Solidmeterials which donot have Crystalline structure Such Crystalline Solid meterials are also called non Crystalline or Amorphous Solids.

All metals and SemiConductors (Si & Ge) are Crystalline meterials.

While wood, plastic, paper are Examples of Amorphous Solid meterials.



Crystalline Amorphous.

Classification of Solidmeterials:-

Basically solid meterials are classified in to 3-types.

a) Conductors
b) Insulators.
c) SemiConductors.

a) **Conductors:-** Conductors are those meterials, which are good Conductors of electricity. This is due to, that in Conductors there are large no. of mobile charge carriers, or free electrons which Carry electrical current.

Example of Conductors :- Copper, Silver, Aluminium.

When a constant electric field is applied (E) to a conductor electrons are accelerated and velocity would be increase indefinitely with time. But due to the collision of electrons, electrons lose energy and steady state (condition) reached; where a finite amount of drift velocity V_d is attained.

V_d is proportional to Electric field

$$V_d = \mu E$$

μ = mobility of electrons. (m^2/Volt-sec)

If Concentration of electrons is 'n' per Cubic meter, The Current density J is

$$J = nqV_d.$$

$$J = nq\mu E \quad (\because V_d = \mu E)$$

$$\boxed{J = \sigma E} \quad (\because \sigma = nq\mu)$$

'σ' = Conductivity of Conductor $(\Omega/m)^{-1}$

$(\because J \propto E)$

(2) Insulators :- Insulators are those meterials which are bad Conductors of electricity. This is due to, they have no charge Carriers & free electrons to Carrey electric ~~field~~ current.

Ex:- glass, rubber, quartz.

(3) Semiconductors :- Semiconductors are the meterials, whose Conductivities lie b/w Conductors and insulators. They have poor Conductivity than Conductors and higher than insulators.

Ex:- Si, Ge. Silicon, Germanium.

Structure of An Atom:-

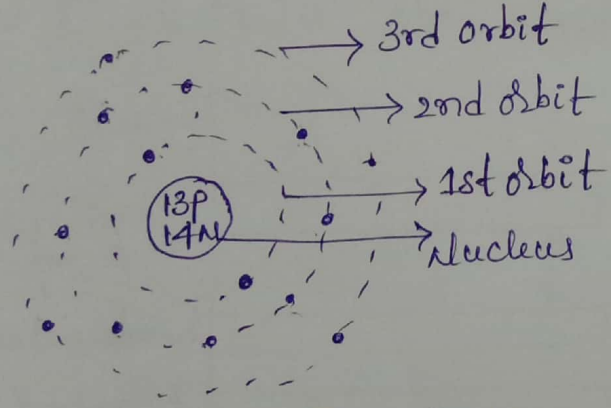
An atom Consists of a Central portion which is Called the nucleus. A no. of Smaller particles Called electrons moves in elliptical orbits about the nucleus. The no. of protons or electrons present in its an atom is Called its atomic number.

Ex:- Z=14 for Si. All electrons of an atom do not move in the same orbit. All electrons are arranged in different orbits or shells.

$(2n^2)$ n=1,2,3 she

1. Ex:- Aluminium Atom. → Atomic number → 13, Al(13)
i.e Al has 13 protons & 14 neutrons in its nucleus.

2. Si. atomic number → 14. i.e it has 14 protons & 14 neutron in its nucleus.



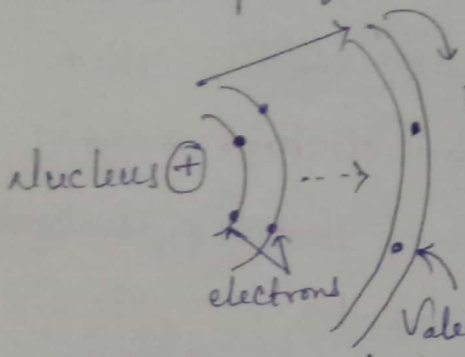
Atomic Structure of Al.

The outermost shell is Called the Valence shell. and The $e^{\ominus}$ in this shell are called Valence electrons.

Each shell has an energy level associated with it.

(*) Closer shell of the Nucleus is tightly bound the Nucleus and posseses lower energy level. While the energy level of Valence shell is heighest. i.e Valence electrons loosely bound to the nucleus as having Energy level.

The Concept of Energy level is shown fig.



Energy level increases from 1st shell to Valence shell as the distance from the nucleus increases.

Concept of Energy level.

* The energy band theory:- Now the Valence e⁻ possess highest energy level. When such electrons from the Covalent bonds, due to the Coupling b/w Valence electrons The energy levels associated with valence electrons merge into each other. This merging forms an energy bands.

The three energy bands are,

1. Valence band
2. Conduction band
3. Forbidden band (or) gap.

1. Valence band:- The energy band formed due to the merging of energy levels associated with the valence electrons i.e electrons in the last shell, is called valence band.

2. Conduction band:- In normal conditions, these valence electrons from the Covalent bonds are not free. But when certain energy is imparted to them, they became free.

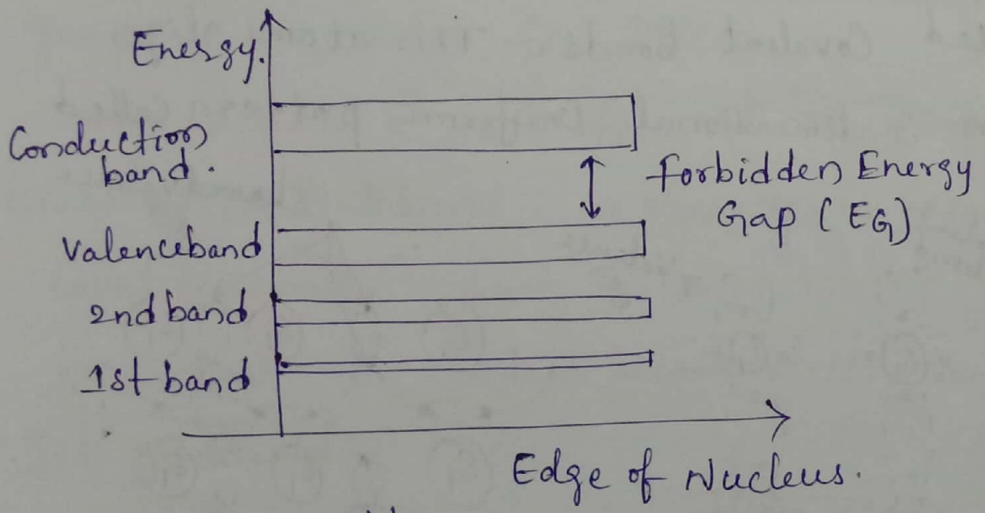
The energy band formed due to merging of energy levels associated with the free electrons is called Conduction band.

3) Forbidden ~~energy~~ gap (or) band :-

under normal conditions, the valence band is empty. But when energy is imparted the valence electrons jump from Valence band to Conduction band.

While jumping from valence band to C.B electrons have to Cross an energy gap.

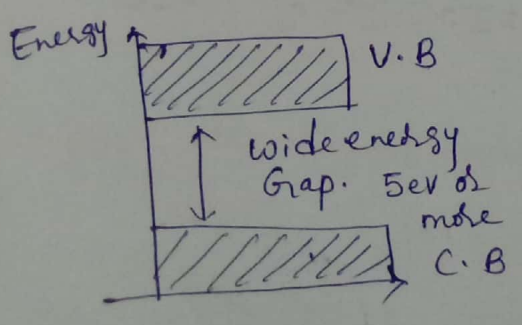
The energy Gap which is present seperating the Conduction band and valence band is called forbidden band (or) Forbidden gap. (E_G). The electrons can't exist in F.G.



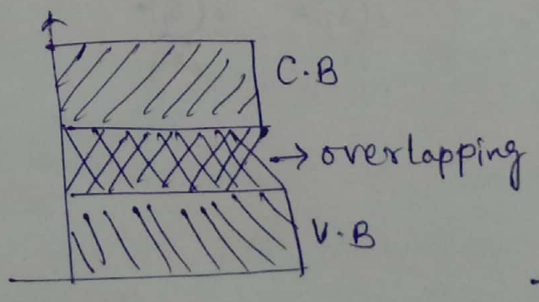
The Graphical Representation of Energy bands in a Solid is called Energy band diagram

Units :- eV.

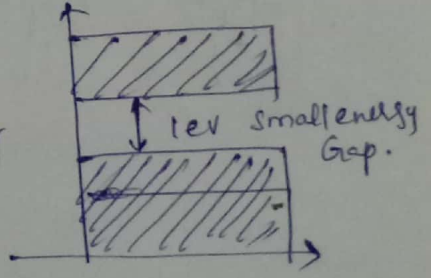
Energy band diagrams :-



a) Insulators.



(b) Metals.



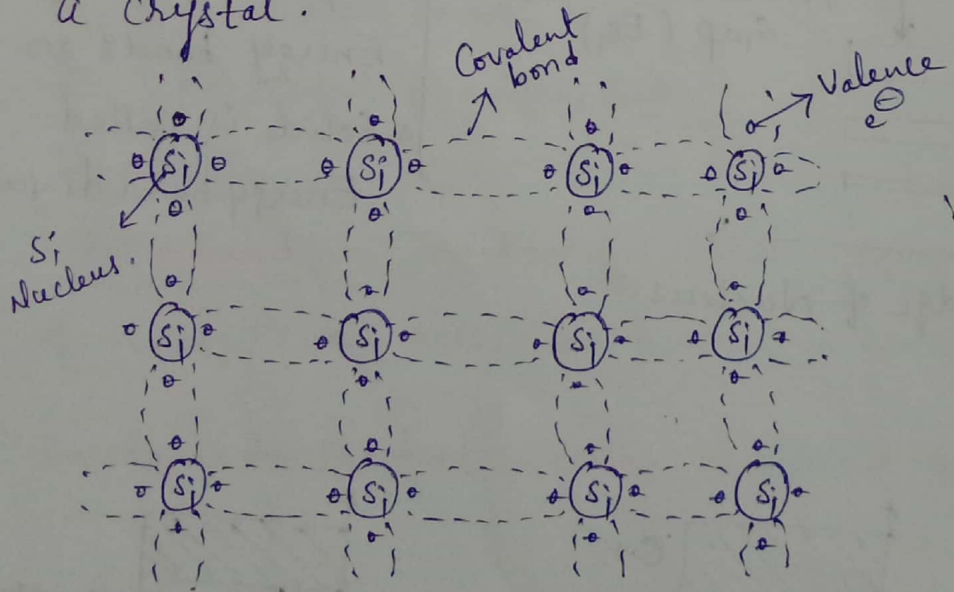
(c) Semiconductors.

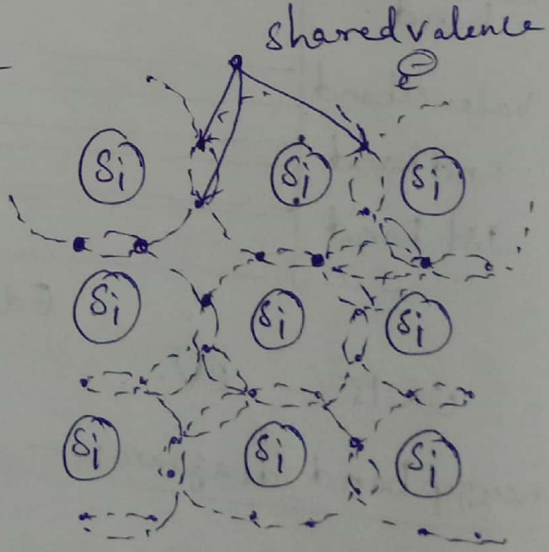
Semiconductors:- 2 types.

1. Intrinsic Semiconductor (pure)
2. Extensic Semiconductor

1. **Intrinsic semiconductor:-** A Semiconductor in its pure form called an intrinsic semiconductor.

Consider an intrinsic semiconductor meterial silicon. An outer most shell of an atom is capable of holding eight electrons. It is said to be completely filled & stable. But 'Si' outermost shell consists of only 4 electrons. Each of these four electrons form a bond with another valence electron of neighbouring atoms. This is nothing but sharing of electron Such bonds are called Covalent bonds. This atoms align themselves to form 3 dimensional uniform pattern called a crystal.





how the outermost shell of all the atoms is completely filled. and valence electrons are tightly bound to the parent atoms. No. of free electrons available at absolute zero temperature. Hence such an intrinsic semiconductor behaves as a perfect insulator at absolute zero temperature.

(4) Charge carriers in intrinsic semiconductor :-

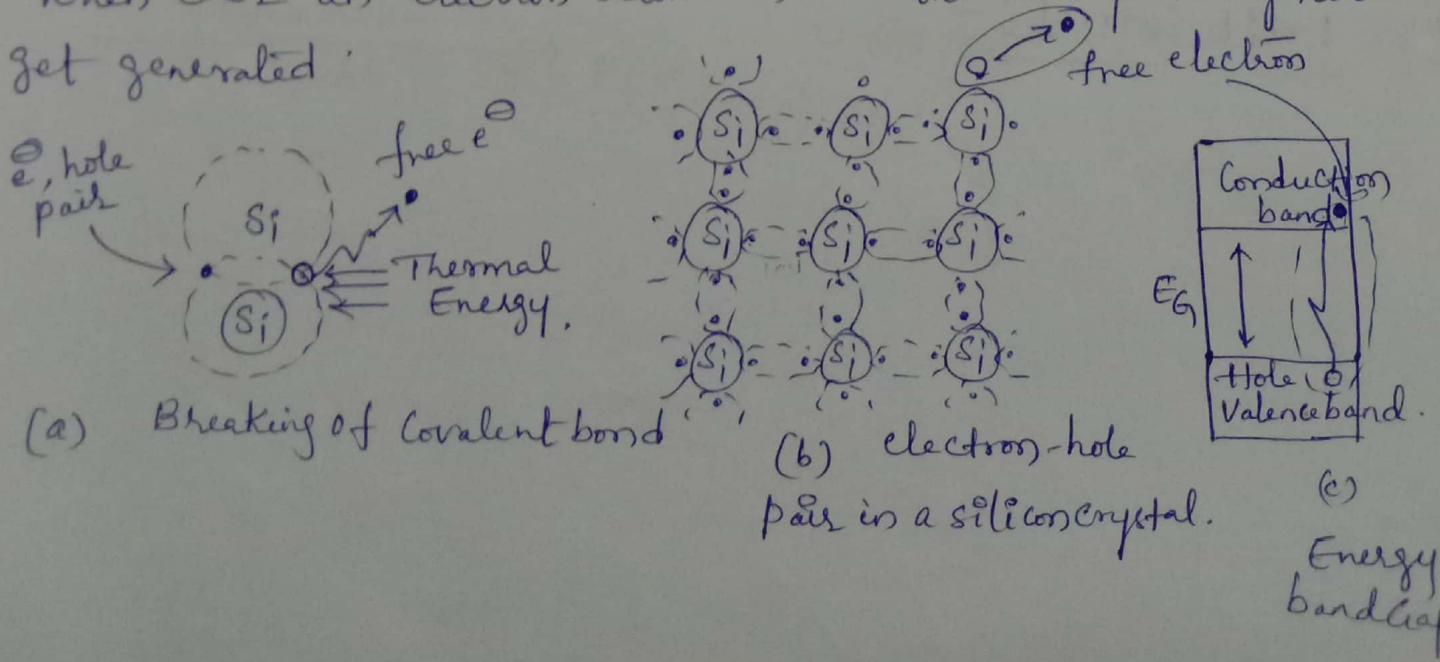
Intrinsic semiconductors behaves as a perfect insulator, at zero temperature.

At Rooms temperature, The no. of valence $e^{\ominus}$ absorbs the thermal energy, due to which they break the covalent bond and drift into conduction band. Such $e^{\ominus}$ is called free $e^{\ominus}$.

The energy required to break a covalent bond is 0.72eV for germanium, 1.1ev for Silicon.

When valence $e^{\ominus}$ drift from valence to conduction band by breaking covalent bond, a vacancy is created in the broken covalent bond. Such vacancy is called hole.

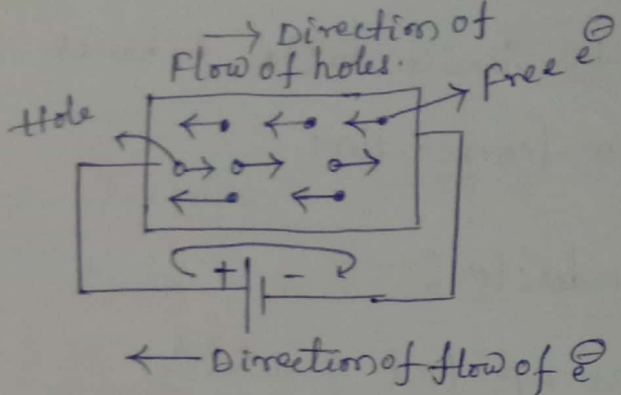
When ever an election become free, the corresponding hole get generated.



(a) Breaking of covalent bond (b) electron-hole pair in a silicon crystal. (c) Energy band diagram.

(*) Conduction in intrinsic Semiconductors:-

Total Current = Electron current + Hole current



We have seen two types of charge carriers electrons and holes present in intrinsic semiconductor. Let us consider A battery is connected across an intrinsic semiconductor The free electrons negatively charged experience a force towards the positive terminal of the battery while the holes as positively charged experience a force towards Negative terminal of the battery.

Key:- The direction of current flows from positive to negative terminal of the battery is referred as the conventional current direction.

(*) Drift Current:-

Carrier Concentration in an intrinsic Semiconductor and Fermilevel

In a pure or intrinsic Semiconductor the electron hole pairs are generated due to thermal generation. The no. of electrons and holes are always equal in number.

In energy band diagram, the probability that the energy level is occupied by an electron is given by Fermi-Dirac probability function. Denoted as F(E), It is given by the expression

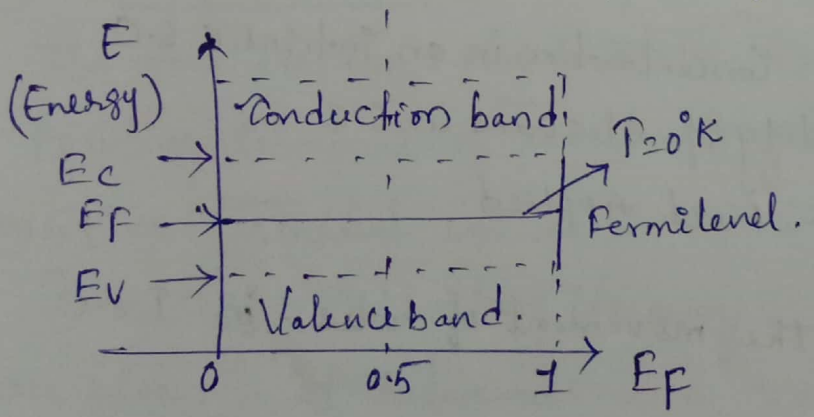
$$F(E) = \frac{1}{1 + e^{(E - E_f)/KT}}$$

K = Boltzmann's const. in eV/°K

T = Temperature in °K

E_f = Fermilevel (or) characteristic energy for crystal in eV.

E = Energy level occupied by an electron in eV.



Thus in energy band Diagram the Fermilevel for the intrinsic Semiconductor lies at the Centre of the forbidden energy band.

(4) Conductivity and mobility for intrinsic S.C:-

I.S.C behaves as Insulator at (0K), But at roomtemperature Because 0K The ∞. of Valence band remains full, The Conducti band empty no. free charge carriers are available for Conduction But room temperature (300k) The thermal energy is Sufficient to create a large no. of electron-hole pairs. Now if electric field is applied the Current flows the Semiconductor. The Current flows in a Semiconductor due to the movement of electrons in one direction and Holes in opposite direction.

In a metal the Current density is

$$J = q n \mu E$$

The Current density in intrinsic Semiconductor due to movement of electrons $J_n = q n \mu_n E$

where q = charge on an electron

n = Electron Concentration in an intrinsic S.C

μ_n = Mobility of electrons in S.C

E = Electric field Applied.

By The Current density due to the movement of holes in I.S.C

$$J_p = q p \mu_p E$$

q = charge on a hole.

p = Hole Concentration

μ_p = mobility of holes

E = Electric field.

Total Current density $J = J_n + J_p$.

$\therefore J = q n \mu_n E + q p \mu_p E$

$J = qE(n\mu_n + p\mu_p)$

$\boxed{J = \sigma E}$ $\quad (\because \sigma = n\mu_n + p\mu_p)$

$\because \sigma$ = Conductivity of Semiconductor.

But intrinsic semiconductor no. of $e^{\ominus}$ = holes. $\Rightarrow n = p = n_i$

$J = qE(n_i\mu_n + n_i\mu_p)$

$J = q(\mu_n + \mu_p) n_i E$.

$\because \boxed{J = \sigma E} \Rightarrow \boxed{\sigma = q n_i (\mu_n + \mu_p)}$ //.

Hence Conductivity of intrinsic S.C is depends on intrinsic Concentration (n_i), (μ_n) mobility of electrons, (μ_p) mobility of holes.

(*) Drift Current:- when a voltage is applied to a semiconductor the free electrons try to move in a straight line towards the positive terminal of the battery. The electrons moving towards positive terminal collide with the atoms of semiconductor and Connecting wires along its way. Each time the electron strikes an atom, it rebounds in a random direction. But still the applied voltage make the electron drift towards the positive terminal. This drift Causes Current flow in a semiconductor, under the influence of electric field (applied voltage). This Current produced due to drifting of free electrons called drift Current. and velocity with which electrons drift is called drift velocity.

Extrinsic Semiconductor:-

Intrinsic (or) pure Semiconductors have small conductivity at room temperature. Therefore not that much use. ∴ By adding some amount of impurity atoms to a pure semiconductor we can improve the conductivity is called extrinsic Semiconductor.

This process of adding impurity atoms to a pure semiconductor is called doping. Hence the conductivity is increased by ~~adding~~ the doping process.

Depending on the types of impurities, the two types of extrinsic semiconductors are

1. N-type.
2. P-type.

(*) Types of impurities:- 2 types.

① Donor impurity (pentavalent impurity) → Creates N-type S.C.
② Acceptor impurity (Trivalent impurity).

1. Pentavalent impurity:- The impurity material having five valence electrons is called pentavalent ~~impurity~~ atoms. When it is added to an intrinsic Semiconductor, it is called donor doping. as each impurity atom donates one free electron to an intrinsic material. Such an impurity is called donor impurity.

Ex:- Arsenic, Bismuth, phosphorous. Etc.

This creates large no. of free electrons called called N-type Semiconductor.

(2) Trivalent impurity:- Another type of impurity used is trivalent impurity atom. Which has only three valence electrons. Such an impurity is called Acceptor impurity.

When this is added to intrinsic Semiconductor, it creates more holes and ready to accept an electron. Hence the doping is called Acceptor doping.

Ex:- Gallium, indium, boron

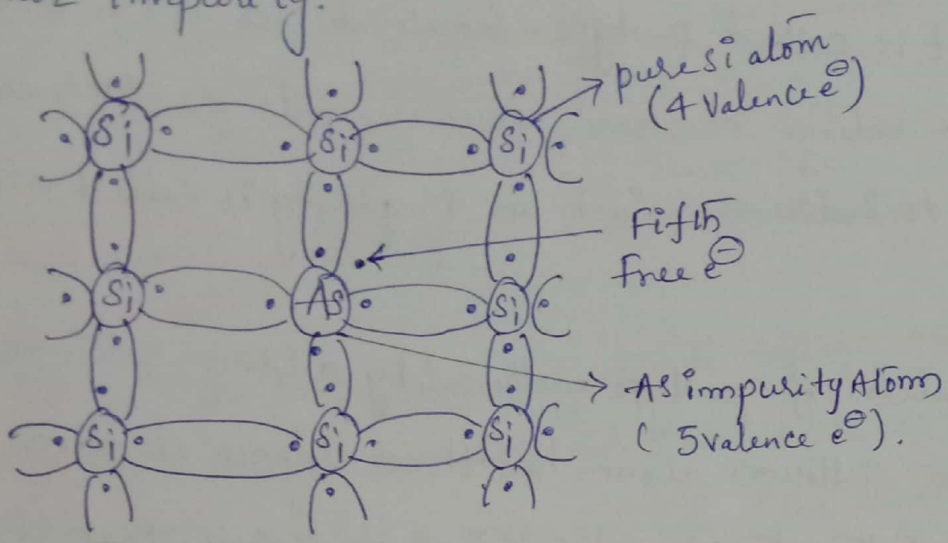
The resulting Extrinsic Semiconductor with large no. of holes is called p-type semiconductor.

(*) 1. N-type Semiconductor:-

When a small Amount of pentavalent impurity is added to a pure Semiconductor, it is called N-type Semiconductor. The pentavalent impurity has 5 Valence electrons. These elements are phosphorous, Antimony, Bismuth. Such an impurity is called donor impurity.

Let us Consider Formation of N-type material by adding Arsenic (As) into Silicon (Si). The Arsenic atom has 5 Valence electrons. An Arsenic Atom fits in Silicon Crystal in such a way, that its four valence $e^{\ominus}$ Covalent bond with Adjacent Silicon atoms. The fifth $e^{\ominus}$ has no chance of formation of Covalent bond. This spare $e^{\ominus}$ enters into the Conduction band as free $e^{\ominus}$. That means each Arsenic atom added to Si atom gives one free electron.

free $e^{\ominus}$ Having negative charges, The material is known as N-type material and impurity donates free electron called donor impurity.

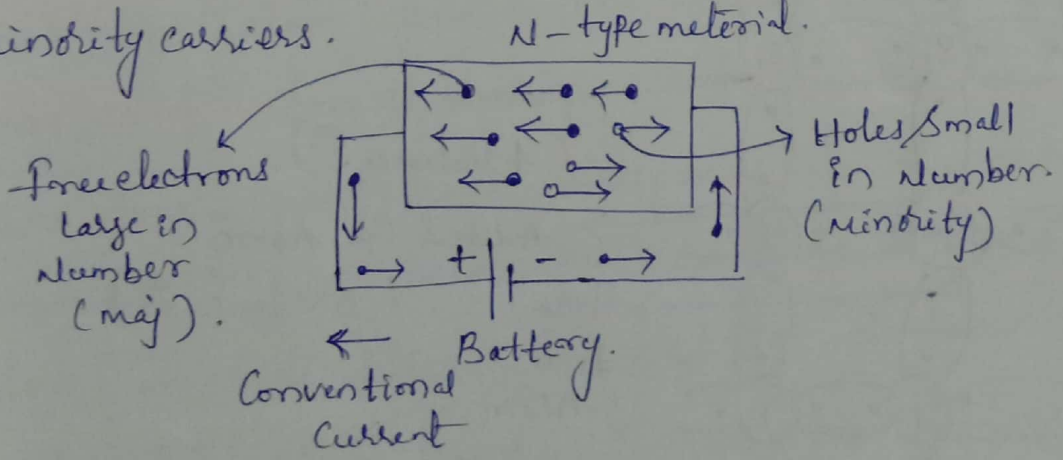


N-type material formation

(*) Conduction in N-type semiconductor :-

When a External DC voltage is applied to N-type semiconductor the free electrons move in a direction of positive terminal of Voltage applied. This Constitutes a current. Thus the conduction is predominately by free electrons. The holes are less in number hence $e^{\ominus}$ current is dominant over the hole current.

Hence in N-type semiconductors free electrons are called majority Carriers while The holes which are small in no. of called minority carriers.

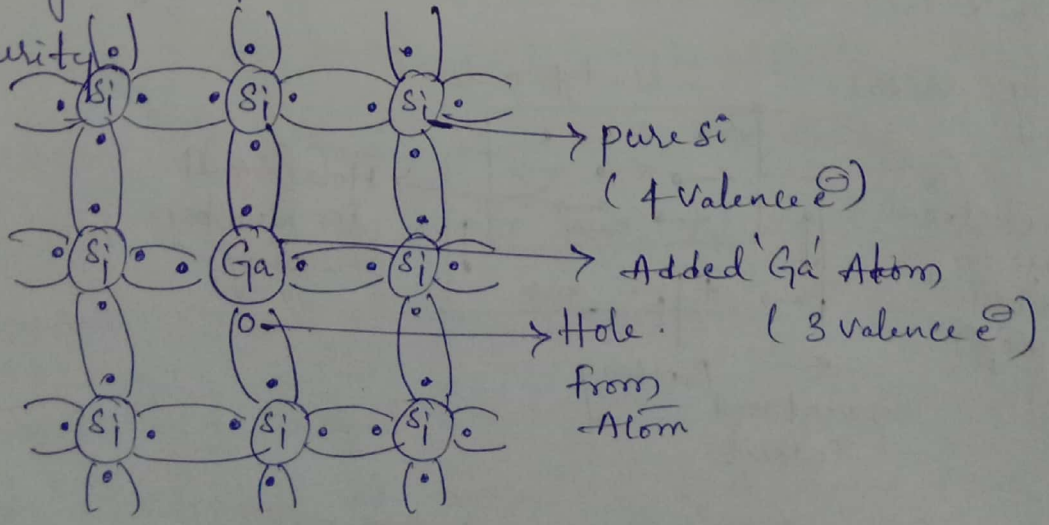


Current Conduction in N-type Material.

2) P-type Semiconductor :-

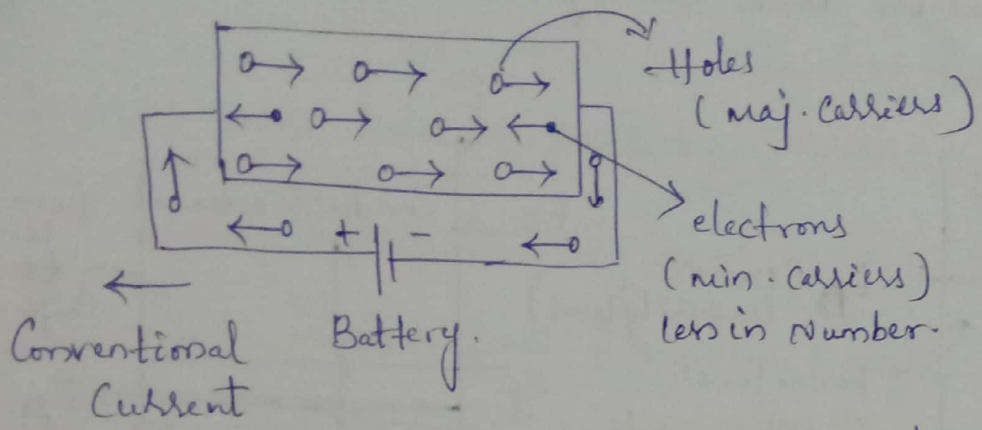
When a small Amount of trivalent impurity is added to a pure Semiconductor, it is called p-type Semiconductor. The trivalent impurity has three Valence electrons. These elements are such as gallium, boron, or indium. Such an impurity is called acceptor impurity.

Consider the formation of p-type material by adding gallium (Ga) into Silicon (Si) The gallium atom has three Valence electrons. So gallium atom fits into the silicon in such a way that its three Valence electrons form Covalent bonds with the three adjacent Silicon atoms. Being short of on electron The Covalent bond in the Valence shell is incomplete. the resulting vacancy is called a hole. That means each gallium atom added to Silicon atom gives one hole. As holes are treated by positively charged, the material is known as p-type material. This indicates that a hole created due to added impurity is ready to accept an election and hence called acceptor impurity.



P-type material formation.

Conduction in p-type Semiconductor:-



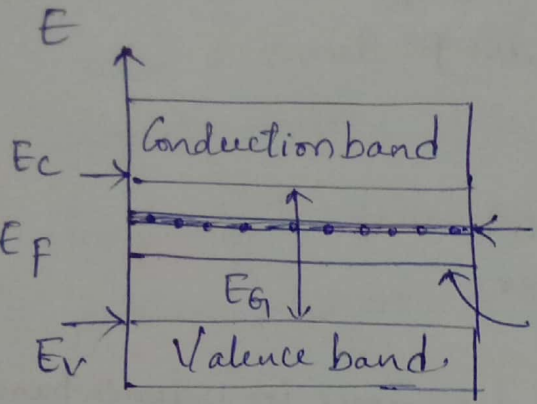
If p-type material is subjected to voltage holes move in valence band and are mainly responsible for the conduction. So Current Conduction is due to holes in p-type material. The electrons also present in Conduction band but are very less in Number. ∵ Holes are maj, & are minority in p-type.

(*) Fermilevel in Extrinsic Semiconductor:-

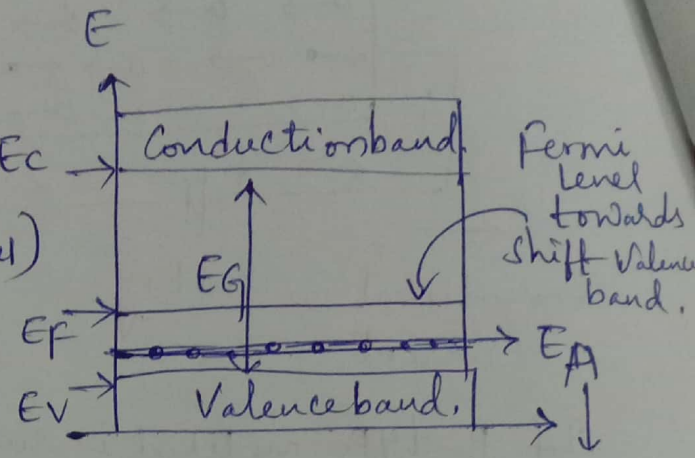
When the impurities are added to the intrinsic Semiconductor, the allowable energy levels are introduced and material becomes extrinsic.

In N-type Semiconductor, A donor impurity is added, Each donor atom donates one free electron and there are large no. of free electrons available in the Conduction band. The donor energy level corresponds to the donor impurity Added is just below the Conduction band. The donor level is indicated as E_D and its distance is 0.01 eV below the Conduction band in Si. As this distance is very small. Atmost all the extra electrons from donor impurity atom to jump into Conduction band.

So in N-type material gets shifted towards the conduction band. But Below the donor energy.



(a) N-type material.



(b) P-type material. (Acceptor Energy level

In P-type material, acceptor impurity added, due to this large no. of holes gets generated in Valence band. The acceptor energy level corresponds to acceptor impurity gets ~~created in the Valence~~ introduces which is indicated as E_A. and its very close to ~~the acceptor energy level~~. The Valence band just above it. The electrons from Valence band jump to acceptor energy level leaving behind the holes in Valence band. This shifts the fermi level E_f towards the Valence band.

[∵ probability is indicated by fermi level E_f]
carriers.

④ Conductivity of Extrinsic Semiconductor:-

Extrinsic S.C are 2 types. Let expression for the conductivity of N-type & P-type.

1. N-type
2. P-type

Conductivity of N-type Material:-

In N-type material, the free electrons are majority Carriers, while holes are minority Carriers.

n_n = Concentration of free electrons in n-type.

P_n = Concentration of holes in P-type.

N_D = Concentration of donor atoms.

Basic Equation of Conductivity, in N-type.

$$\sigma_n = (n_n \mu_n + P_n \mu_p) e \qquad (e = q)$$

∵ But $P_n << n_n$ (Holes are minority)

$$\boxed{\sigma_n = n_n \mu_n e}$$

Thus as $N_D >> n_i \Rightarrow n_n \cong N_D$. (∵ Concentration of $e^{\ominus}$ Controlled by Donor atom.)

$$\boxed{\sigma_n \cong N_D \mu_n e}$$

(2) Conductivity of P-type Material:-

In P-type, majority Carriers are holes; electrons are min.

n_p = Concentration of free electrons in P type

P_p = Concentration of holes in P-type.

N_A = Concentration of Acceptor atoms.

Basic Equation of Conductivity, in P-type.

$$\sigma_p = (n_p \mu_n + P_p \mu_p) e$$

∵ But $n_p << P_p$ ($e^{\ominus}$ are min)

$$\boxed{\sigma_p = P_p \mu_p e}$$

(∵ Concentration of holes Controlled by Acceptor Atoms)

Thus as $N_A \cong P_p$.

$$\boxed{\sigma_p = N_A \cdot \mu_p \cdot e}$$

⑦ Carrier Concentrations in Extrinsic Semiconductor:-

Let us obtain the Concentrations of minority and majority Carriers in n-type and p-type materials using Law of mass action.

i) N-type material:

For N-type material it is seen that, $n_n = N_D$.

According to law of mass action

$$n_n \times p_n = n_i^2$$

$(\because n_n = N_D)$

$$N_D \cdot p_n = n_i^2$$

$$p_n = \frac{n_i^2}{N_D}$$

→ The no. of holes (min) Concentration obtained.

ii) P-type material:-

For P-type material it is seen that, $p_p = N_A$

According to law of mass action

$$n_p \times p_p = n_i^2$$

$$n_p \times N_A = n_i^2$$

$$n_p = \frac{n_i^2}{N_A}$$

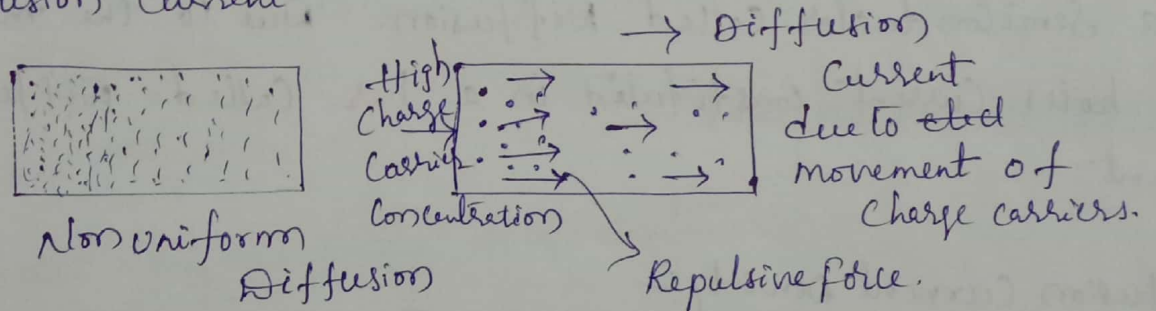
→ The no. of electrons (min) Concentration obtained.

⑧ Diffusion Current:-

This Current which is due to the transport of charges occuring because of nonuniform Concentration of charged particles in a Semiconductor.

nsider a piece of Semiconductor, which is non uniformely oped. due to non uniform doping one type of charge carriers occurs at one end of the piece of semiconductor.

The charge carriers either electrons or holes. of one type of impurity is used. They have same same polarity and hence experience a forces of repulsion b/w them. The result is that there is a tendency of charge carriers to move gradually i.e to diffuse from high ~~Concentration~~ region of high Carries density to the low Carrier density This proces is called diffusion. This movement of charge carriers under the proces of diffusion constitutes a current called diffusion current.



(a) Non uniform Diffusion

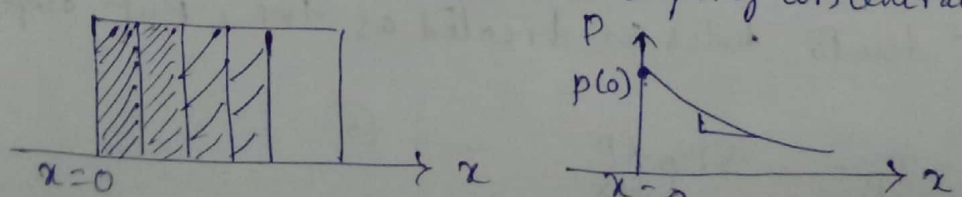
(b) proces of diffusion.

Diffusion Current

→ A diffusion current ~~exists~~ is possible only in case of Non uniformly doped Semiconductors. While drift current is possible in Semiconductors & conductors.

* Concentration Gradient:-

Consider a p-type semiconductor, which is Non uniformly doped. As 'x' increases the doping concentration decreases.



To form p-type S.C, acceptor impurity is added which creates holes as majority charged particles.

Let 'p' be the Concentration of holes.,

Concentration of holes at $x=0$ is $p=p(0)$ and is maximum and heavily doped at $x=0$. As x decreases, Concentration of holes decreases.

The slope of the graph can be observed, The ratio of Change in Concentration to change in distance. It is called Change of Concentration (or) Concentration gradient.

Slope of Graph = Concentration Gradient = $\frac{dp}{dx}$.

However holes move from Higher Concentration to lower Concentration. Such movement of holes due to the Concentration gradient in a Semiconductor called Diffusion. Due to the movement of holes Current constituted in a bar Called Diffusion Current.

* Diffusion Current Density:-

Consider p-type semiconductor

A diffusion Current density is $\propto$ to Concentration gradient which is responsible for the Diffusion & Diffusion Current.

$$J_p \propto \frac{dp}{dx} \quad \text{---} \quad (1)$$

J_p = Diff'n Current Density due to holes.

$$J_p = q D_p \frac{dp}{dx} \quad \text{---} \quad (2)$$

Where D_p = Diff'n Const for holes. (m^2/sec)

Note:- Current due to holes is treated as +ve, But slope is -ve.

$$\therefore J_p = -qD_p \frac{dp}{dx} \quad \text{---} \quad (3)$$

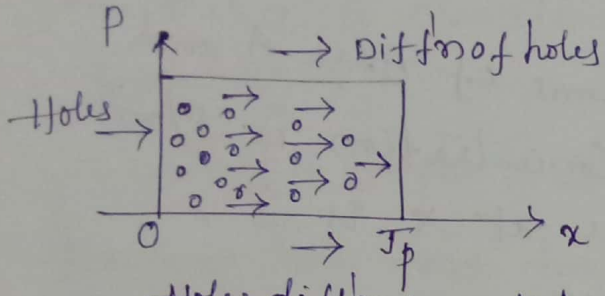
In case of N-type, Diffusion Current due to $e^{\ominus}$.

The Current due to $e^{\ominus}$ is in opposite direction to the Conventional Current. mathematically -ve. also Concentration Gradient -ve.

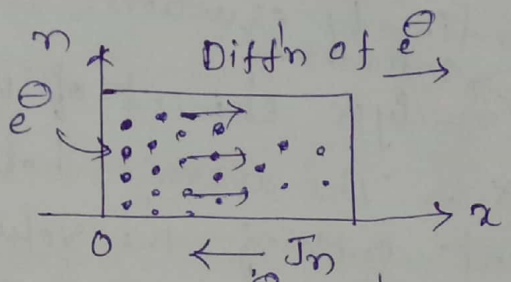
∵ Diffusion Current density

$$J_n = +qD_n \frac{dn}{dx} \quad \text{---} \quad (4)$$

D_n = Diff'n Const due to electrons. (cm^2/sec).



Holes diff'n Current density



$e^{\ominus}$ diff'n Current density.

Problem:- (1)

The mobility of free electrons and holes in pure Germanium are 3800 and 1800 $cm^2/V-s$ respectively. The corresponding values for pure Silicon are 1300 and 500 $cm^2/V-s$ respectively. Determine the values of intrinsic Conductivity for both Germanium and Silicon. Assume $n_i = 2.5 \times 10^{13}\ cm^{-3}$ for Germanium and $n_i = 1.5 \times 10^{10}\ cm^{-3}$ for Silicon at room temperature.

Sol:- (1) The intrinsic Conductivity for Ge.

$$\sigma_i = q n_i (\mu_n + \mu_p)$$

$$= 1.6 \times 10^{-19} \times (2.5 \times 10^{13}) [3800 + 1800]$$

$$\sigma_i = 0.0224\ S/cm$$

(2) The intrinsic Conductivity for Si

$$\sigma_i = q n_i (\mu_n + \mu_p)$$

$$= (1.6 \times 10^{-19})(1.5 \times 10^{10})(1300 + 500)$$

$$\sigma_i = 4.32 \times 10^{-6}\ S/cm$$

Junction Diode:-

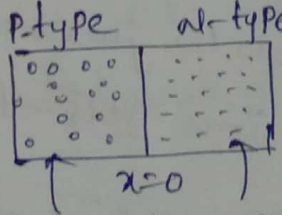
Introduction to PN Diode Junction:-

Earlier we have seen that the two types of extrinsic Semiconductor N-type and P-type. In N-type the majority charge carriers are electrons, holes are minority charge carriers. In P-type The holes are majority charge carriers and electrons are minority charge carriers.

These two types of material namely P-type and N-type are chemically combined with a special fabrication technique to form a P-n junction. Such a Semiconductor P-n junction forms a popular electronic device called diode.

Open Circuited P-n Junction:-

fig. shows the P-n junction at $x=0$, with uniform doping in each region. Both types of charge carriers, majority as well as minority exist in each region. Assuming thermal equilibrium.

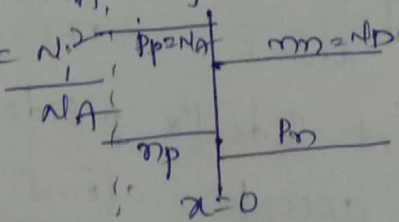


As the two regions are at thermal equilibrium, we can write

On P-Side:- P_p: maj Carriers Concentration $= N_A$, Uniform Doping.

n_p: Min charge " " $= \frac{n_i^2}{N_A}$

$\therefore (n_p << P_p)$



On N-Side:- n_n = maj Charge Carrier Concentration $= N_D$

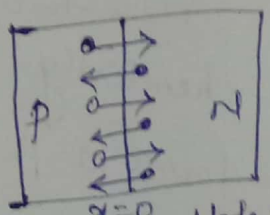
P_n = Min Charge Carrier Concentration $= \frac{n_i^2}{N_D}$

$\therefore (P_n << n_n)$

⊛ Formation of Depletion Region:-

There exist a concentration gradient near the junction. There are large no. of holes on p-side, small no. of holes on n-side, near the junction. Thus holes starts moving from p-side to N-side i.e from High Concentration area to low Concentration area. This is nothing but diffusion of holes from p-side to N-side.

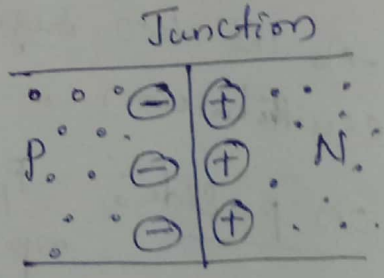
Ily The electrons on N-side start diffusing across the junction into the p-region.



As holes enter the N-region, they find no. of donor atoms. The holes recombine with the donor atom. As donor atoms accepts the additional holes they become positively charged immobile ions. This happends immediately when holes cross the junction, Hence no. of +vely charged immobile ions gets formed near the junction on N-side

Ily The atoms on p-side are acceptor atoms. The electrons diffusing from N-side to p side recombine with acceptor atoms on p-side.

As acceptor atoms accept additional electrons, they become Negatively Charged immobile ions. So large no. of immobile ions gets formed nearer the junction.



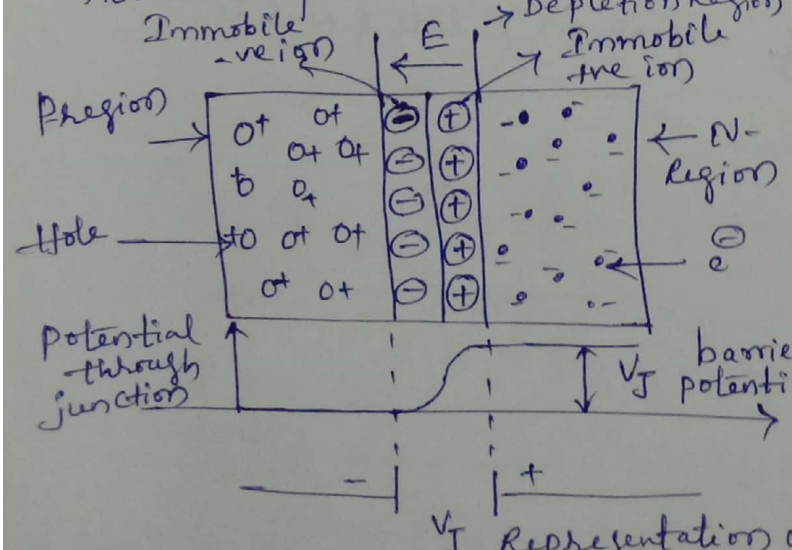
Formation of immobile ions.

Thus in thermal equilibrium, near the junction there exist a wall of negative immobile charges on P-side, positive immobile charges on N-side. In this region there are no mobile charge carriers. Such region is depleted of the free mobile charge carriers and hence called depletion region (or) Depletion layer. Also called space charge region. It acts as barrier.

(*) Barrier potential :-

The opposite charges existing near the junction creates a potential difference (voltage) across the junction. The electric field b/w the charges is responsible to produce potential difference across the junction. The potential difference has a fixed polarity and acts as a barrier to the flow of electrons and holes. across the junction. Hence this potential is called barrier potential, junction potential or built in potential barrier of a p-n junction.

The barrier potential is approximately 0.7V for Si, 0.3V for Ge.



Open Circuited PN Junction

Barrier potential Depends on

i) Type of S.C used.
ii) The Concentration of donor impurity on N-side
iii) The Concentration of Acceptor impurity used on P-side.
iv) Intrinsic Concentration of basic S.C
v) The temperature.

④ Expression for barrier potential :-

Let us derive the expression for the barrier potential

It is known that the change in Concentration, induces the Voltage and is given by

$$V_{21} = V_T \ln\left(\frac{P_1}{P_2}\right) \quad \text{— ①}$$

At the junction There is abrupt change in the Concentrations of holes from P_p to P_n

So $P_1 = P_p \simeq N_A$ & $P_2 = P_n$ — ②

② in ①

$$V_J = V_T \ln\left(\frac{N_A}{P_n}\right) \quad \text{— ③} \quad (V_J = \text{potential barrier})$$

But according to Law of mass Action

$$n_n \times P_n = n_i^2$$

$$P_n = \frac{n_i^2}{n_n} \qquad \because n_n = N_D.$$

$$P_n = \frac{n_i^2}{N_D} \quad \text{— ④}$$

④ in ③

$$V_J = V_T \ln\left(\frac{N_A}{n_i^2/N_D}\right) \Rightarrow \boxed{V_J = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)} \;//$$

The above eqn tells, Junction potential depends on Volt equivalent temperature, & doping on P-side & N-side i.e N_A, N_D.

⊕ Band Structure of P-N Junction:-

It is known that the fermilevel in n-type meterial lies just below the Conduction band, while p-type meterial, it just above the Valence band. When p-N junction is formed, the diffusion starts. The charges get adjusted so as to equalise the fermilevel in the two parts of P-N junction.

This is similar to adjustment of water levels in two tanks of unequal levels, when connected to each other. The charges flow p to n and n to p side till, the fermilevel on the two sides get lined up.

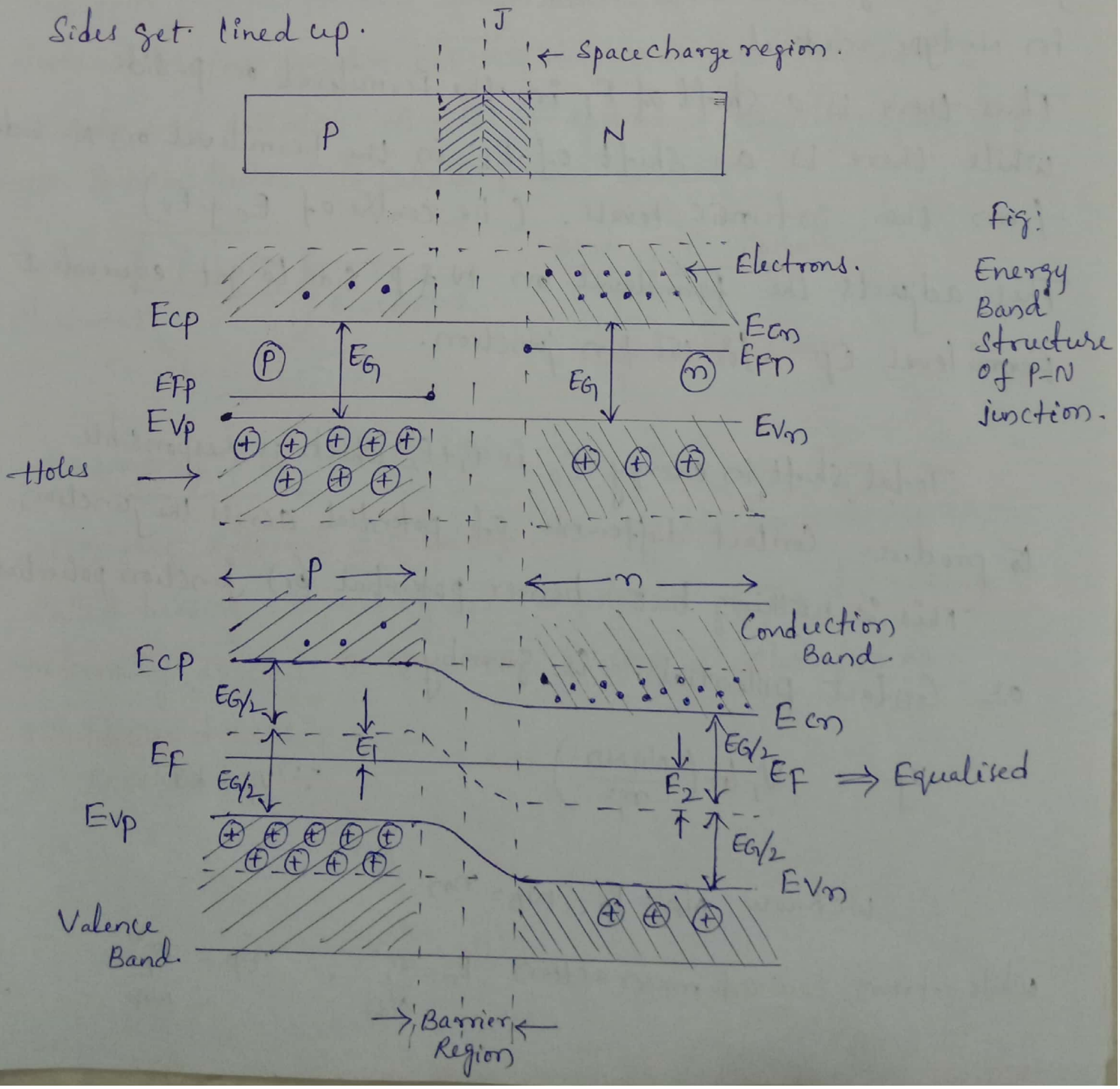


Fig: Energy Band structure of P-N junction.

The transfer of charges and energy band structure showing equalisation of Fermilevels in p and n regions is shown in fig.

→ In p-region, the fermilevel E_{Fp} is near E_{vp} just above edge of Valenceband. In N-region The fermilevel E_{Fn} is near E_{cn}. just below edge of Conduction band. And there is Difference b/w levels of E_{Fn} and E_{Fp}. The transport of charges, The edge of Conduction band E_{cp} in the p-type meterial becomes higher than E_{cn} in the N-type meterial.

Hy The edge of Valence band E_{vp} in p-type is heighes than E_{vn} in N-type meterial.

Thus there is a shift of E_1 in the Fermilevel on p-side while there is a shift of E_2 in the Fermilevel on N-side from their intrinsic levels. (i.e centre of E_c & E_v)

This adjusts the fermilevel on N & p side to get equivalent Fermi level E_F for the p-n junction.

Total shift in energy E_0 is $E_1 + E_2$ which is responsible to produce Contact difference of potential across the junction

This is nothing but barrier potential (or) junction potential or Contact potential. is, given by

$$V_J = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \qquad \because V_T = kT$$

$\therefore$ we know $N_A = P_p$, $N_D = n_n$

while from law of mass action $P_n = \frac{n_i^2}{N_D}$, $n_p = \frac{n_i^2}{N_A}$

Using in the Equation V_J

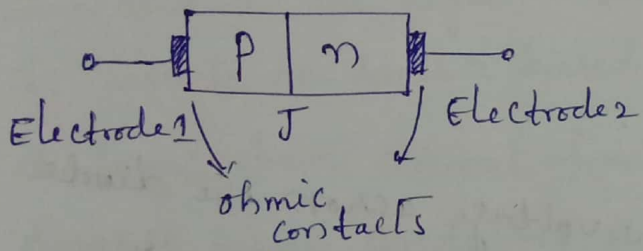
$$V_J = V_T \ln\left(\frac{p_p \cdot n_i^2 / p_n}{n_i^2}\right)$$

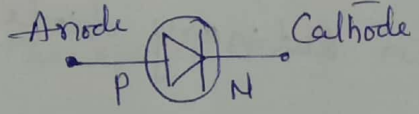
$$\boxed{V_J = V_T \ln\left(\frac{p_{p0}}{p_{n0}}\right) = V_T \ln\left(\frac{n_{n0}}{n_{p0}}\right)}$$

∵ This is the alternative expression for V_J, where '0' indicates the thermal equilibrium condition.

(*) The p-n Junction Diode:-

The p-n junction forms a semiconductor device called p-n junction diode. The p-n junction has two terminals. Called electrodes Anode and Cathode. A metal is applied to heavily doped n & p type semiconductor is called ohmic Contact.





Symbol of a diode.

(*) Biasing of p-n junction diode:-

Applying External d.c Voltage to any electronic device is Called biasing. Depending on the polarities of the d.C Voltage externally applied to it, the biasing is classified as

1. forward bias
2. Reverse bias.

① forward bias:-

An External d.c voltage is connected in such a way that P-region is connected to positive of d.C voltage and n-region is connected to the -ve of the d.c voltage.

⊛ Zener diode:-

When the reverse voltage is reaches the breakdown voltage in Normal P-n junction diode, the current through the ~~diode~~ junction and power dissipated at the junction will be high. Such an operation is destructive and diode gets damaged. whereas diode can be designed with adequate power dissipation capabilities to operate in the breakdown region. one such a diode is known as zener diode. Zener diode is a heavily doped than ordinary diode.

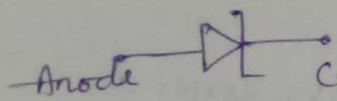
Applications:- Voltage regulator

under reverse bias condition, the voltage across the diode remains constant although the current through the diode is increases. The voltage across zener diode serves as reference voltage. Hence diode can be used as a voltage regulator.

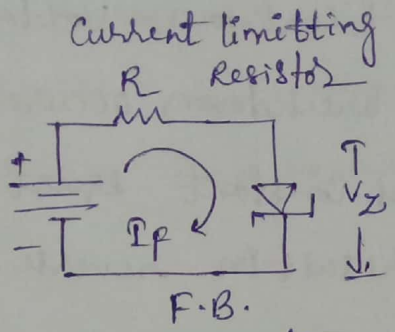
If it is required to provide const voltage over a range across load resistance R_L, whereas input voltage may be varying a range. Zener diode is reverse biased, as long as input voltage does not fall below V_Z. Hence the voltage across diode const & Hence the load voltage will be const.

* Zener diode:- Zener diode is a reverse biased heavily doped p-n junction diode, which operates in the breakdown region.

Circuit symbol:-



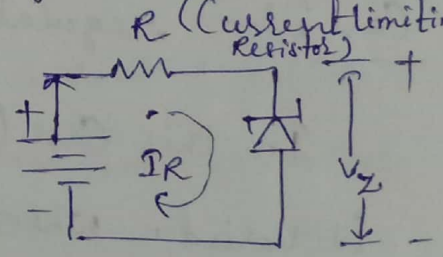
*F. Biasing of a zener diode:-



When the Anode of the zener diode is connected to the positive terminal of d.c source and the cathode is connected to the negative terminal. The zener diode is said to be F.B.
In F.B zener diode behaves as identical to a F.B biasing diode. So, zener diode is not generally used in F.B condition.

* Reverse biasing of zener diode:-

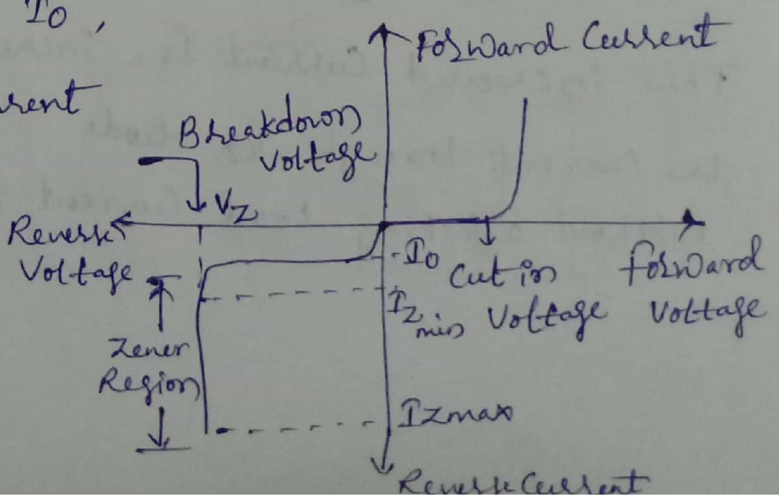
When cathode is connected to the positive terminal and Anode is connected to the negative terminal of d.c source. Then zener diode is said to be reverse biased. The operation of zener diode is different from normal from p-n diode. Zener diode in the reverse biased condition is used as a voltage Regulator.



* V-I characteristics of zener diode:-

Reverse characteristics:-

As we increase the reverse voltage, initially a small reverse current I_O, which is in μA will flow. This current will flow due to minority charge carriers.



-At a certain value of a reverse voltage, the reverse current will increase suddenly and sharply. This is an indication breakdown as occured. This break down voltage is called zener breakdown voltage denoted by V_Z.

After breakdown occures, the voltage at across zener diode remains constant equal to V_Z. Any increase in source voltage will result in reverse zener current.

Application of zener diode :- voltage regulator.

Voltage regulator is a circuit whoose function is to maintain a constant d.c output voltage inspite of the a.c input voltage fluctiations or changes in load resistances values.

* Zener diode shunt regulator :- shunt regulator because the zener diode is connected in parallel or shunt with the load.

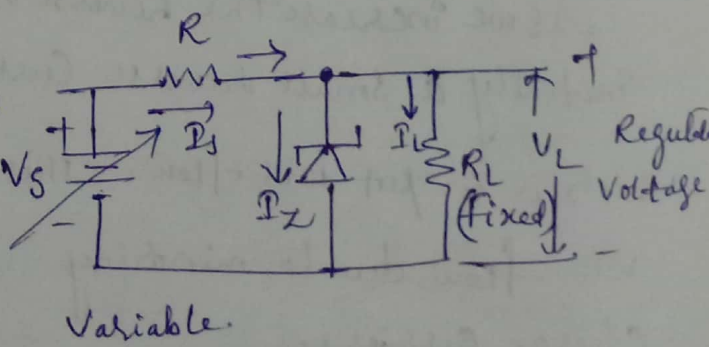
To Explain working, we will consider 2 cases.

Case I :- regulation when i/p voltage is varied :-

In this case load resistor R_L is kept fixed & i/p voltage V_S is varied. When i/p voltage V_S ↑, the i/p current I_S ↑.

$\therefore I_S = I_Z + I_L$.

This increased current I_S, increases the current through I_Z diode without affecting load current I_L.

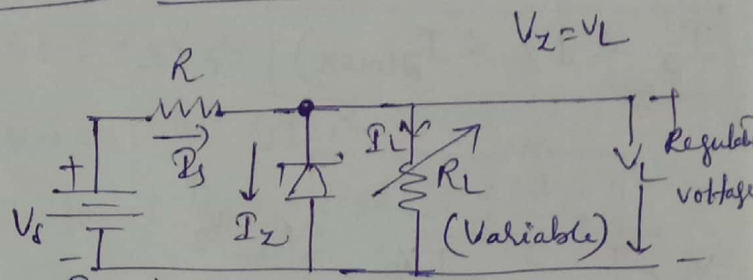


I/p voltage is varied.

Due to increase in input current I_s, the voltage drop across series resistance R_S also increases and Hence keeping the load voltage V_L const.

Now when the i/p voltage is decreases, i/p current also decreases. Due to this current through diode decreases. Also voltage drop across series resistance is reduced. Hence load voltage V_L, and Load current I_L remains const.

Case(ii):- Regulation when load resistance is Varied Varied :-



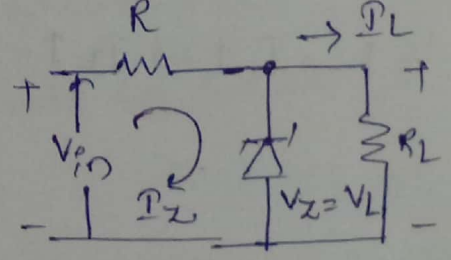
load resistance is Varied.

In this condition i/p voltage V_S is fixed & load resistance is varied when load resistance $R_L \downarrow$, load current $I_L \uparrow$. This cause zener current to decrease. Due to this i/p current & voltage drop across series resistance const. Therefore load voltage V_L is also const.

Now when $R_L \uparrow$, load current decreases $\downarrow$. due to this zener current increases $\uparrow$. This again keeps the values of i/p current & voltage drop across series resistance as a const. Therefore load voltage remains const.

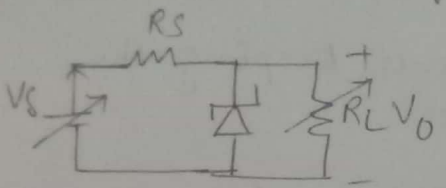
Ex:- line regulation:-

If $I_{Zmin} = 5\,mA$, $V_Z = 6.8\,V$.
$I_{Zmax} = 50\,mA$, $R_S = 1K\Omega$ Then



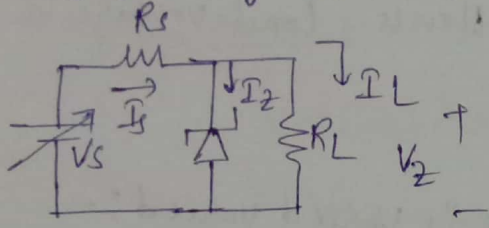
Load and line regulation :-

o/p voltage to be maintained Const irrespective of changing V_S & R_L.

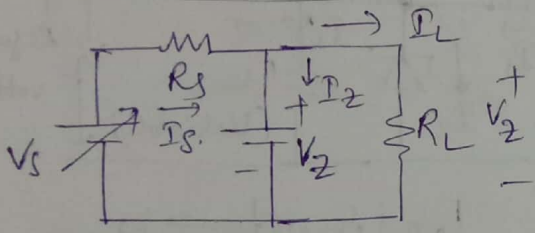


Line regulation

Here V_S ↕ changing, R_L fixed.



$$\boxed{I_{Z_{min}} < I_Z < I_{Z(max)} \Rightarrow V_Z}$$



$$\updownarrow I_S = \frac{\updownarrow V_S - V_Z}{R_S}$$

When V_S changes, I_S also changes.

$$\boxed{\frac{V_{S\,min} - V_Z}{R_S} \; I_S < \frac{V_{S\,max} - V_Z}{R_S}}$$

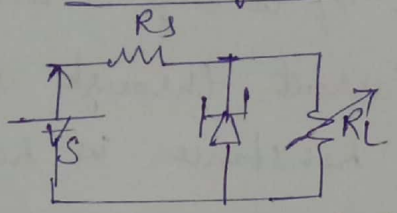
$$\updownarrow I_S = \updownarrow I_L + \underbrace{I_Z}_{\text{fixed}}$$

$$I_{S\,min} = I_{Z\,min} + I_L$$

$$I_{S\,max} = I_{Z\,max} + I_L$$

$V_S \uparrow \rightarrow I_S \uparrow \rightarrow I_Z \uparrow \rightarrow I_L$ (fixed).

Load regulation

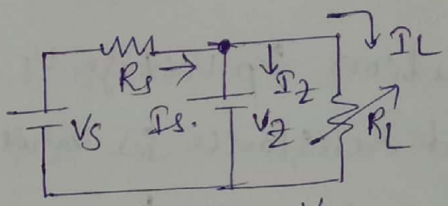


V_S - fixed
R_L ↕ - varied.

The Zener current I_Z in b/w always

$$\boxed{I_{Z(min)} < I_Z < I_{Z(max)} \Rightarrow V_Z \text{ Const.}}$$

When I_Z in this limit V_Z is const.



$$I_S = \frac{V_S - V_Z}{R_S}$$

When V_S fixed, I_S fixed. $\Rightarrow I_S = I_Z + I_L$

But $\updownarrow I_L = \frac{V_Z}{R_L}$ ↕.

When R_L is changing.

I_L also changes.

When I_L ↕, I_Z ↕ changes.

$$I_S(\text{Fixed}) = I_{Z\,max} + I_{L\,min} \Rightarrow \frac{V_Z}{R_{L\,max}}$$

($R_L \uparrow$)

$$I_S(\text{Fixed}) = I_{Z\,min} + I_{L\,max} \Rightarrow \frac{V_Z}{R_{L\,min}}$$

$R_L \uparrow \rightarrow I_L \downarrow \rightarrow I_Z \uparrow \rightarrow I_S$ (fixed).

For min Current,

Voltage across $R_s = V_R \Rightarrow 5mA \times 1k\Omega = 5V$

$\therefore V_{in} - V_R - V_Z = 0$

$V_R = V_{in} - V_Z$

$V_{in} = V_R + V_Z = 5V + 6.8V = 11.8V$

For max Current:

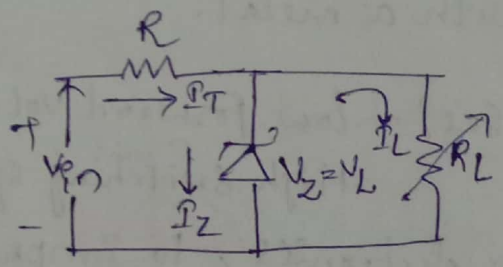
Voltage across R is $V_R = 50mA \times 1k\Omega = 50V$

$\therefore V_{in} = V_R + V_Z$

$= 50V + 6.8V = 56.8V$

This shows, the zener diode used in ckt can regulate i/p voltage from 11.8V to 56.8V & maintains approximately 6.8V o/p.

② Load regulation:-



Ex:- If $I_{Z\,min} = 5mA$

$I_{Z\,max} = 50mA$

$V_Z = 10$ & $V_{in} = 20V$. Then at no load

$R_L = \infty$ & $I_L = 0$

$\therefore$ To limit max current to 50mA (I_{Zmax}).

$$R_{(min)} = \frac{V_{in} - V_Z}{I_{Zmax}} = \frac{20-10}{50mA} = 200\Omega.$$

As you know $I_{Z(min)} = 5mA$, max load current $(50-5) = 45mA$ shows zener diode maintain o/p voltage const for current from 0mA to 45mA.

limitations:- of zener Regulators.

i) exp The o/p voltage of zener regulator is equal to V_Z This is Const voltage, Therefore, These voltages cannot be made adjustable. (regulators)

(ii) Large power dissipated in the series resistor R.

(iii) Corresponding to large changes in the load current, There will be a large change in the zener current. This will result in a large power wastage.

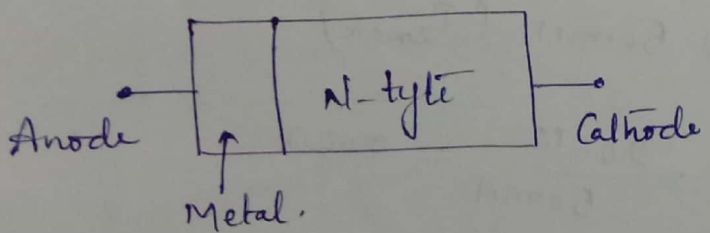
④ Schottky diode:- Hot Carriers diode.

It is a Semiconductor diode formed by junction of a Semiconductor with a metal.

Uses:- low forward voltage (V_F)
High switching speed.

In electronics, to improve the speed we use schottky diode.

Structure:- A metal get combined with S.C, It is a unipolar device.



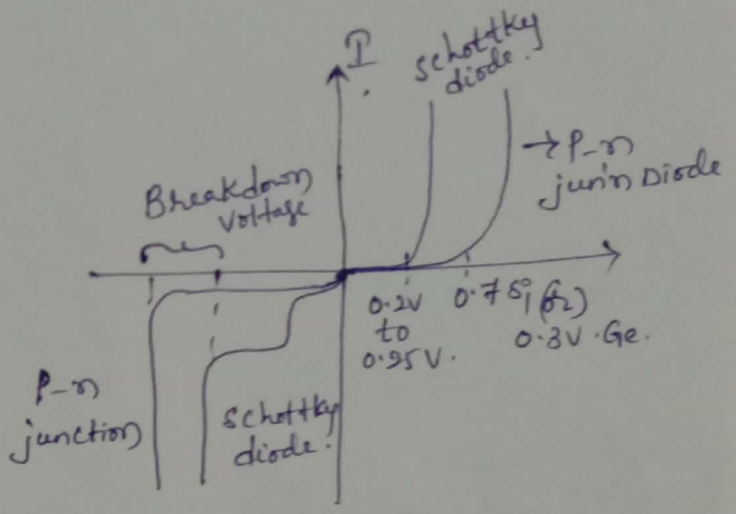
→ When a N-type S.C is join with a metal, there will be no depletion region due to only one type of carriers. So there is no depletion region.

→ Due to unipolar device, $e^{\ominus}$ are majority charge carriers.

→ Usually we can use metal as gold, platinum, Crome, or tungsten.

The main advantage is it has very less Reverse recovery time. due to this we can use schottkey diode in fast switching Applications. because there is no space charge region, it comes to reversebias the schottkey, it will not require Extra Efforts.

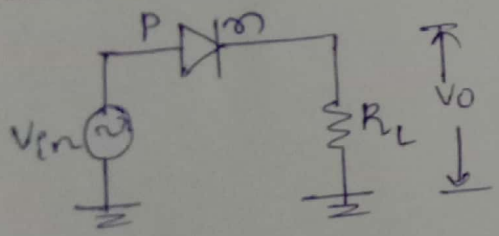
V-I characteristics:-



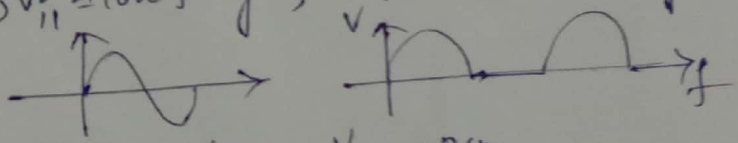
It can be used to rectify high freley sln. 300 GHz.

Ex:- Rectification of high freley signals:-

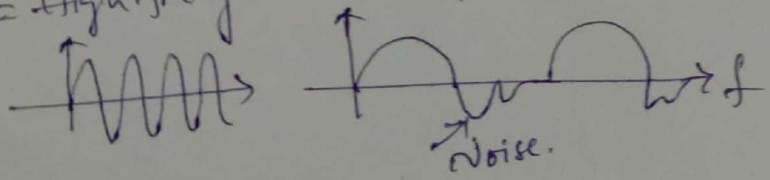
Normal Diode rectification:



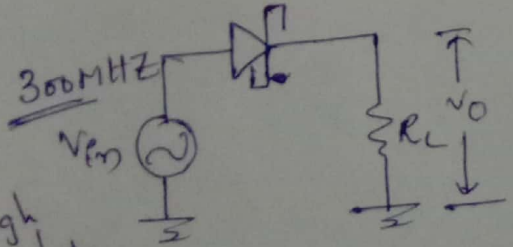
When V_{i1} = low freley ; V_{O1} = at low freley

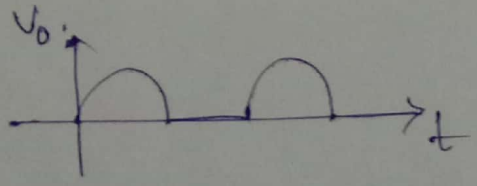


V_{i2} = High freley. V_{O2} = O/p.



Schottky Diode rectification:





If we take Normal diode, it take Sometime due to charege storage at junction for reverse recovery time. In Case of Schottky diode there is no depletion region near junction due to this it switches very fastly.