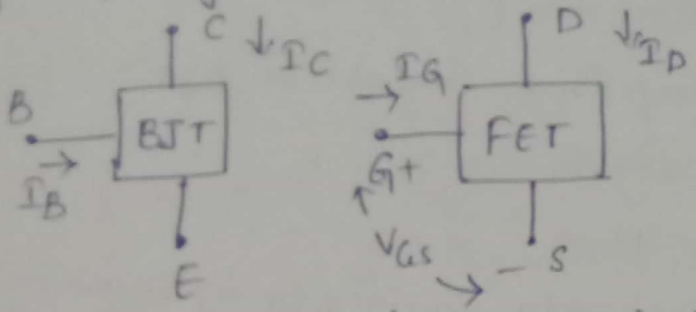
Introduction about FET :-

By comparing with BJT's ; FET's are.



Both are 3 terminal devices, Drain (D), Gate (G) and Source (S).

① BJT is a current Controlled device. $I_C = \beta I_B$.

② FET is a voltage Controlled device.

$I_C = f(I_B)$ — ①

$I_D = f(V_{GS})$ — ②

In Both the Cases, output Current Controlled by input parameters.

② BJT → Bipolar Device i.e $e^{\ominus}$ & holes.

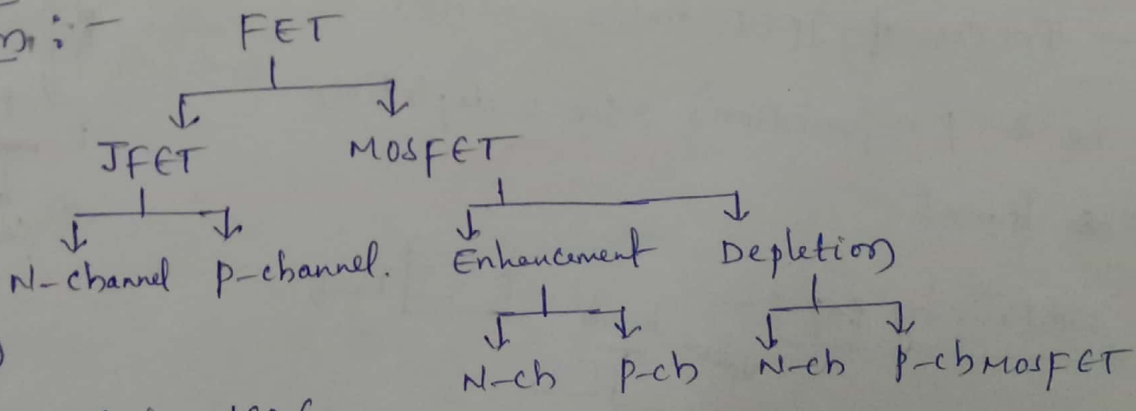
FET → unipolar Device i.e it depends on either $e^{\ominus}$ or holes.

③ N-channel and p-channel. FET like npn & pnp

↳ depends on $e^{\ominus}$ ↳ depends on holes.

④ FET can be used for Amplification & switching.

⑤ Classification :-



⑥ History (FET)

By. Julius Edger lilienfeld — 1926

By Oskar Heil in — 1934.

⑦ History (MOSFET)

By D. Kahng — 1959. (Better than JFET)

(8) "Field-Effect"

An Electric field is developed by the charges present, And this E.f Controls the Conduction path of the output ckt.

(9) FET :- has high input impedance Compare to BJT's.

FET's are More temperature stable " " "

FET's are smaller than " "

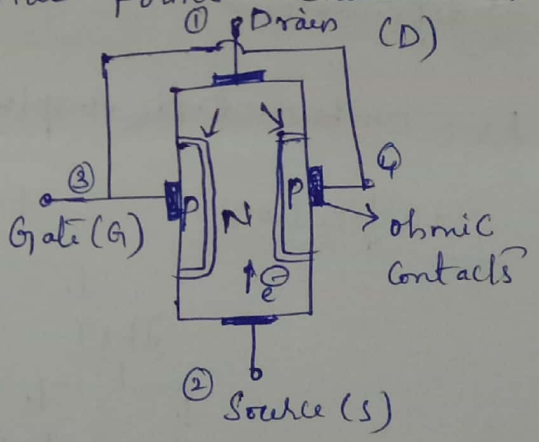
Sensitivity :- BJT's are more Sensitivity by Compare with FET.

(2) Construction and working of JFET :-

1) N-channel JFET.

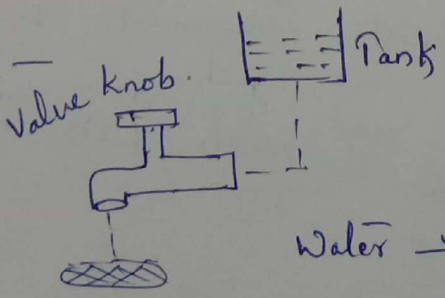
Major part of JFET is N-type meterial, and it is Forming a channel b/w 2 ptype meterials. bcoz of this reason it is called N-channel JFET. i.e N-type meterial Forms a channel b/w 2 P-type meterials.

By P-channel JFET has P-type meterial Forms a channel b/w 2 N-type meterials.



→ In Case of JFET has 2 junction i.e 2-p-n junction's ; i.e 2 depletions are formed.

Working by tap :-



Cause of Water flow → here e⊖ flow, Applied Voltage b/w Drain & Source.

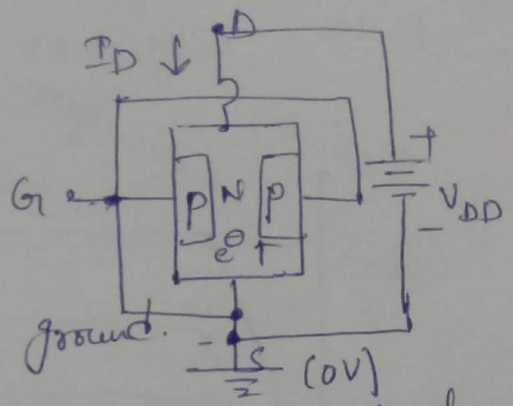
Spigot → as Source.

Valve knob → as Gate Controlled the movement of e⊖ in N-channel.

Sink → Drain ∴ i.e e⊖ going towards Drain.

Continuation of working of JFET :- ($V_{GS}=0V$, $V_{DS}>0V$)

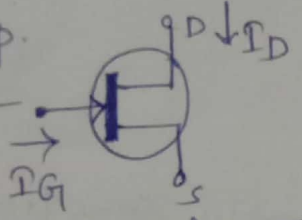
Case i : $V_{GS}=0V$
Case ii : $V_{GS}<0V$
} $V_{DS}>0V$.



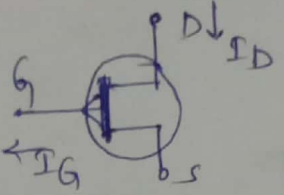
→ i.e potential at gate and source is zero.
When $V_{GS}=0V$, So source is connected to ground.

→ $V_{DS}=V_{DD}$ i.e a +ve voltage, The conventional current I_D developed when we connect V_{DS} as V_{DD}, The width of the depletion layer increased from top.

Symbol:-



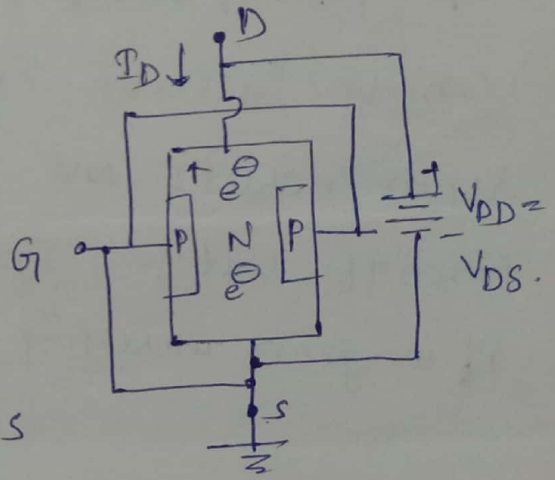
N-channel JFET



P-channel JFET

Pinchoff Voltage:-

i) $V_{GS}=0V \Rightarrow V_G - V_S$.
ii) $V_{DS}=V_{DD}$ i.e $>0V$



electrons ⊖ drift the drain current, when V_{DS} is applied.

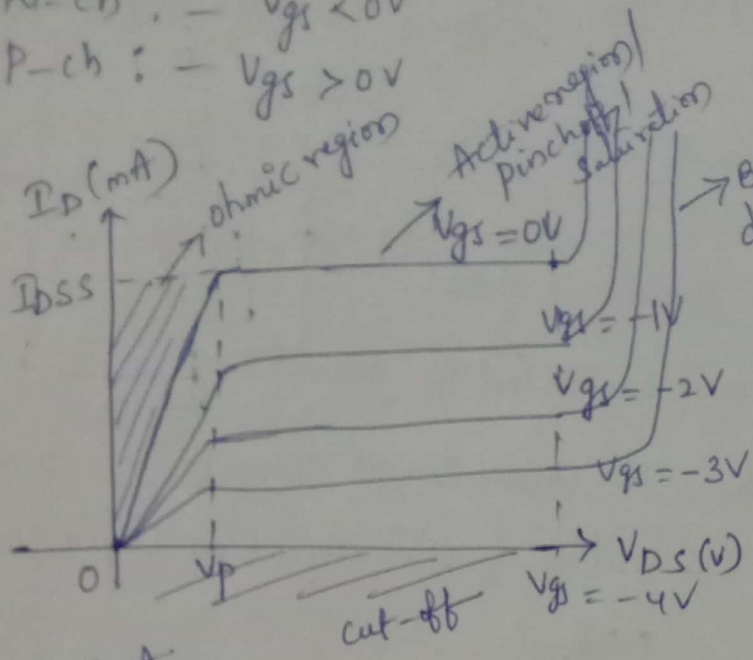
Output drain Characteristics

For CE TxR : I_C Vs V_{CE}
↓ o/p current ↓ o/p voltage
for diff values of I_B (Controlling Current)

In case of JFET : I_D Vs V_{DS}
↓ o/p current ↓ o/p voltage
for diff values of V_{GS} (i/p voltage)
↓ Controlling voltage.

N-ch :- $V_{gs} < 0V$

P-ch :- $V_{gs} > 0V$



$I_D \propto V_{DS}$

ohm's law

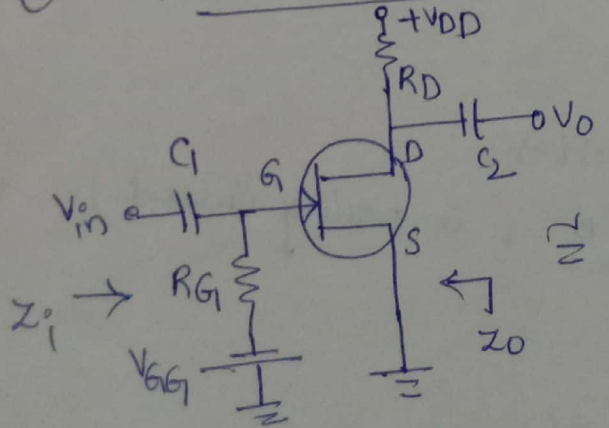
$I_{DSS} \rightarrow$ 8mA $\rightarrow V_{gs} = 0$; $|V_{ds}| > |V_p|$

V_p – pinchoff voltage = –4V

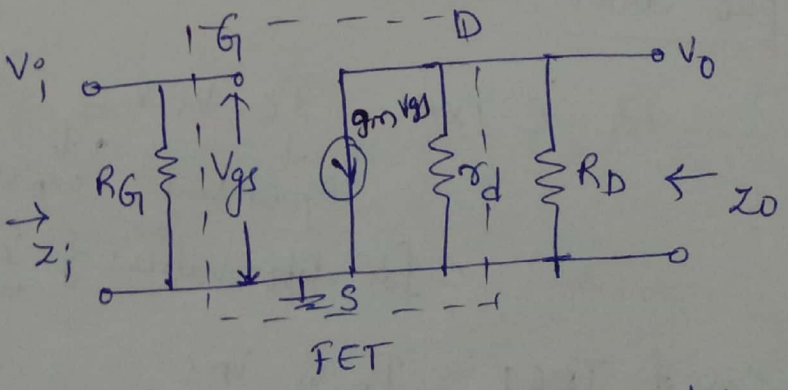
When V_{DS} increases, I_D increases linearly. after some time Depletion region increases, and I_D becomes constant. at this point it is pinchoff voltage. If V_{gs} is –ve, pinch off occurs earlyarly. If we goon increasing V_{DS}, breakdown occur.

① FET Common Source Amplifiers

① FET with fixed bias :



V_{GG} provide Reversebias



Equivalent Small Sln model.

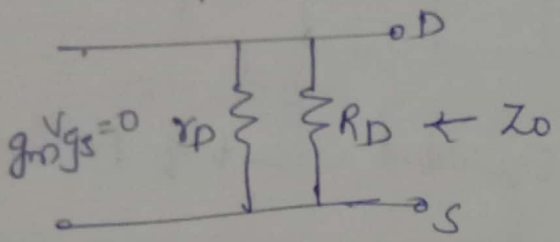
① Input impedance (Z_i)

$Z_i = R_G$

② Output impedance (Z_o) / $V_i = 0$

i.e $V_{gs} = 0$ & hence $g_m \cdot V_{gs} = 0$

from o/p ckt



$Z_o = R_D \| r_D$ if $r_D >> R_D$

$Z_o = R_D$.

③ Voltage Gain (A_V) :- $A_V = \frac{V_o}{V_i} = \frac{V_{ds}}{V_{gs}}$.

$\because V_o = -g_m \cdot V_{gs} (r_d \| R_D)$ (loop eq'n)

we know that $V_i = V_{gs}$.

$V_o = -g_m \cdot V_i (r_d \| R_D)$

$A_V \Rightarrow \frac{V_o}{V_i} \Rightarrow \frac{-g_m \cdot V_i (r_d \| R_D)}{V_i}$

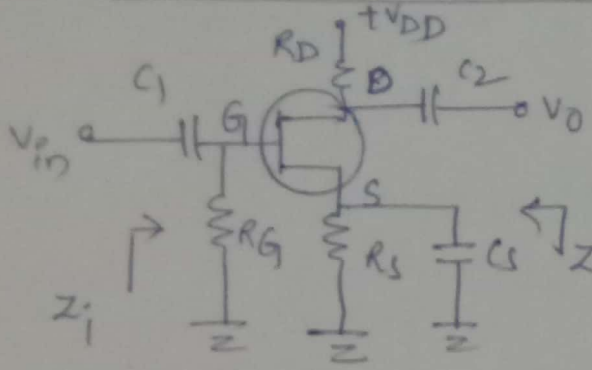
$A_V \Rightarrow -g_m (r_d \| R_D)$

if $r_d >> R_D$

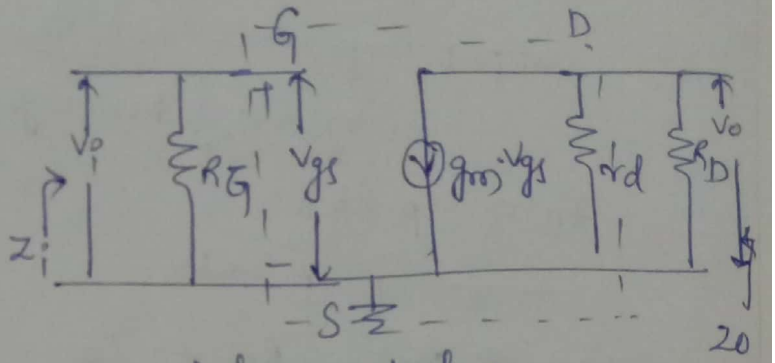
$$\boxed{A_V = -g_m \cdot R_D}$$

'-ve sign indicates phase difference b/w I/p & o/p.

2) FET with Self bias (Common Source Amplifier)



JFET Amplifier with self bias



Equivalent Circuit of FET Amp.

→ Provides self biasing to ckt

1) Input impedance (Z_i) = R_G

2) output impedance (Z_o) = $r_d \| R_D$ ($\because V_{gs} = 0$ i.e $V_i = 0$)
like Fixed bias ckt

if $r_d \gg R_D$

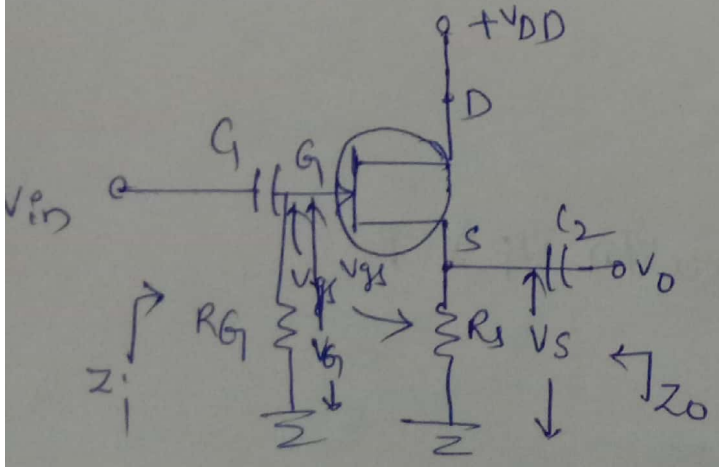
$Z_o = R_D$.

3) Voltage Gain (A_v) = $-g_m \cdot (r_d \| R_D)$

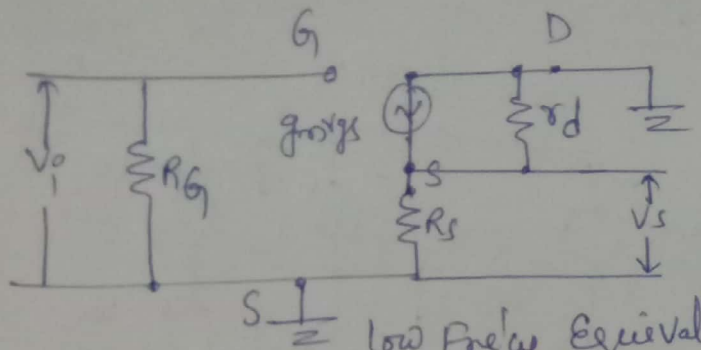
$A_v = -g_m \cdot R_D$ (if $r_d \gg R_D$) (Same values will get in self bias also)

=

II) FET Common Drain Amplifier :— (Source follower)

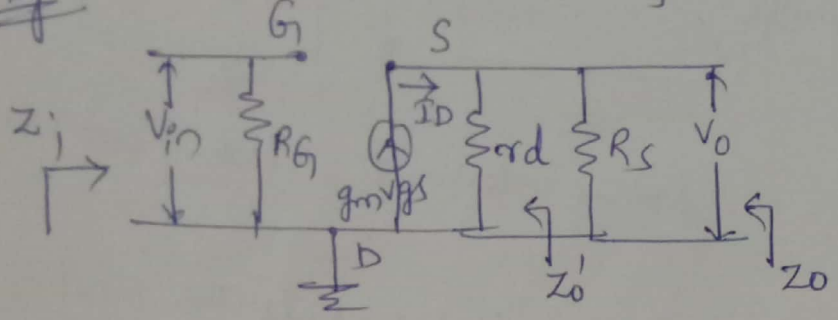


$V_S = V_G + V_{GS}$ Here V_{gs} Const. when V_g Varies Source Voltage V_S Varies Called Source follower.



low Freq Equivalent model.

14



① Input impedance :- Z_i

$Z_i = R_G$.

② output impedance :- Z_0

$Z_0 = Z_0' \| R_S$

$Z_0' = \left.\frac{V_0}{I_d}\right|_{V_i=0}$

Applying KVL to o/p side

$V_i' + V_{gs} - V_0 = 0$ — ① $(\because V_i = 0)$

$V_{gs} = V_0 \Rightarrow$ i.e $V_0 = V_{gs}$.

from the fig : $I_D = g_m \cdot V_{gs}$.

as $V_{gs} = V_0$

$I_D = g_m \cdot V_0$

$\frac{I_D}{V_0} = g_m$

$Z_0' = \frac{1}{g_m}$

$\boxed{Z_0 = \frac{1}{g_m} \| R_S}$

③ Voltage Gain $(A_V) = \frac{V_0}{V_i}$

from fig $V_0 = -I_d (r_d \| R_S)$

$I_d = g_m \cdot V_{gs}$

$V_0 = -g_m V_{gs} (r_d \| R_S)$ — ②

from eq'n ①

$V_i' = -V_{gs} + V_0$

$V_i' = -V_{gs} + [-g_m \cdot V_{gs} (r_d \| R_d)]$ — ③

$A_V = \frac{-g_m \cdot V_{gs} (r_d \| R_D)}{-V_{gs} (1 + g_m (r_d \| R_D))}$

$A_V = \frac{g_m (r_d \| R_D)}{1 + g_m (r_d \| R_D)}$

$\boxed{A_V = \frac{g_m \cdot R_D}{1 + g_m \cdot R_D}}$ (if $r_d \gg R_D$)