UNIT - IV

10/10/2017

LOGICAL FAMILIES

TTL LOGIC

The digital IC technology has rapidly advanced from small scale Integration (SSI) through Medium scale Integration (MSI), Large scale Integration (LSI), Very large scale Integration through Ultra Large scale Integration. The technology is entering into Giant scale Integration in which millions of Gate equivalent circuits are integrated on a single chip. The use of IC's reduced the overall size of a digital system, the cost of systems are also reduced. The reliability has improved because the number of external interconnections from one device to another has reduced. The power consumption of digital systems also reduced greatly.

IC's have limitations. It cannot handle very large voltages or currents and also electrical

devices like inductors, Transformers & large capacitors cannot readily implemented on chips. IC's are fabricated using various technologies such as TTL (Transistor-Translator logic), ECL (Emitter coupled logic, IIL (Injected Integrated logic) which uses Bipolar Transistor. and next technology is MOS (Metaloxide semiconductor) logic & CMOS logic which use MOSFET's.

Digital IC specification terminology:-

(1) Threshold voltage:

It is defined as the voltage at the input of a gate which causes a change in the state of the output from one logic level to the other.

(2) Propagation Delay:

It is defined as the time taken by a pulse to propagate from input to output.

(3) Power Desipation:

The power desipation of a logic gate is the

power required by the gate to operate with 50 %. duty cycle at a specified frequency. and it is expressed in mW. (milli watts).

(4) Fan-in :-

Fain-in of a logic gate is defined as the no. of inputs that the gate is designed to handle.

(5) Fan-out :-

It is defined as the maximum no. of similar gates that the output of the gate can drive without impairing its normal operation.

(6) Noise Margin :-

It is the maximum noise signal expressed in volts that can be added to the input signal of a digital circuit without causing an undesirable change in the circuit output.

(7) Speed Power Product :-

It is the product of the propagation delay(ns) and the average over dessipation (mW) of a logic gate

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Manufacturer's Designations for IC's:

Each Manufacturer uses a spefic code and assigns a specific time members to the IC's produced. for example: 741. An internally compensated op-amp originally manufactured by fair child is sdd as μA741. Here μA represents the identifying initials used by fair child. The codes used by the well known manufactures of linear IC's are

1) Fair child - μA, μAF (codes) Ex: μA 741
2) National Semiconductor - LM, LH, LF, TBA → LM741
3) Motorola - MC, MFC → MC1741
4) RCA - CA, CD → CA3741
5) Texas Instruments - SN → SN52741
6) Signetics - N/s, NE/SE → N5741
7) Burr-Brown - BB

A number of manufacturers also produce popular IC's of the other manufacturer's. for easy use, they usually britain the original type member of the IC along with their identifying initials Ex: Fair child's original μA741 is also manufactured by other manufacturer's as follows.

Last 3 digits in each manufacturer's designation are 741 as shown in above example. All these op-amps have the same specification. Since a number of manufacturers produced the same IC. Some Linear ICs are available in different classes such as A, C, E, S and SC.

For example 741A, 741A, 741C, 741E, 741S and 741SC are different versions of the same op-amp. The main difference of these op-amps are

741 → Military grade op-amp. (operating temperature range is −55°C to 125°C)

741C → commercial trade op-amp (operating temperature range is 0°C to 70/75°C)

741A → Improved version of 741. } Better electrical specifications

741E → Improved version of 741E }

741S → Military grade op-amp with higher slew-rate.

741SC → commercial grade op-amp with higher slew rate.

Packages :-

There are three packages available

(1) The Metal can (TO) package

(2) The Dual-in-line package (DIP)

(3) Flat package (or) Flat pack.

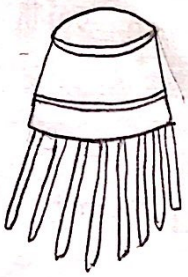
Op-amp packages contain 1, 2 or 4 op-amps.

Typical packages have 8-terminals, 10 terminals and 14 terminals.

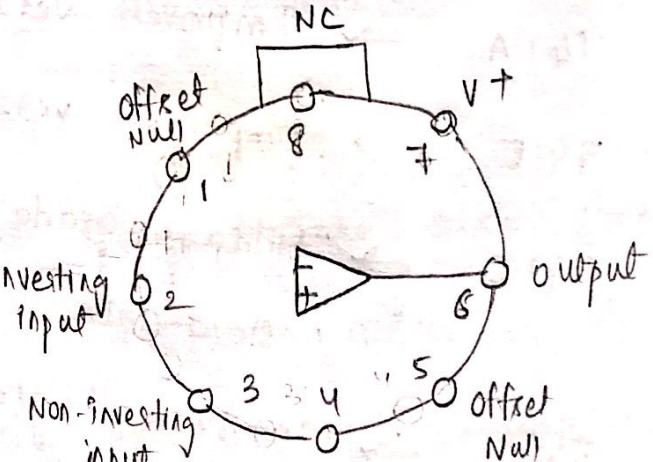
(8-terminals → metal can package; 10 terminals → DIP; 14 terminals → DIP & Flat pack)

The widely used μA741 is a single op-amp and is available as 8 pin can, 8 pin DIP, 10 pin flat pack or 14 pin DIP.

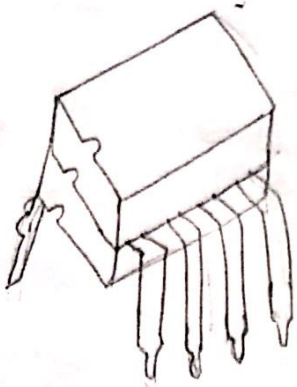
Various IC packages of μA741 op-amp along with connection Diagrams :-



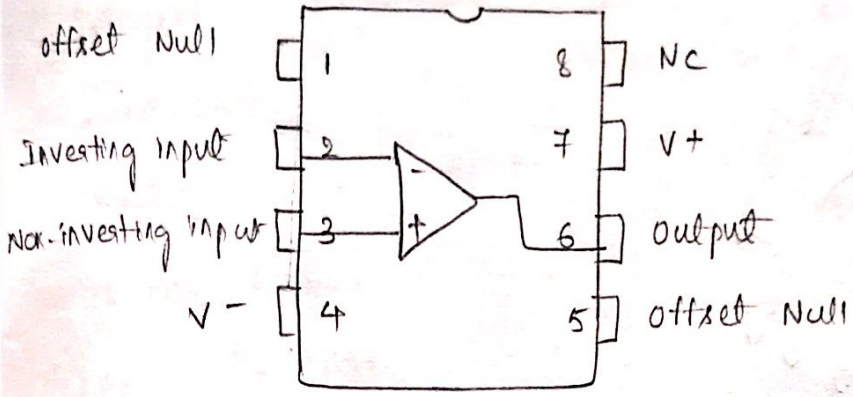
TO-5 Style package with straight leads



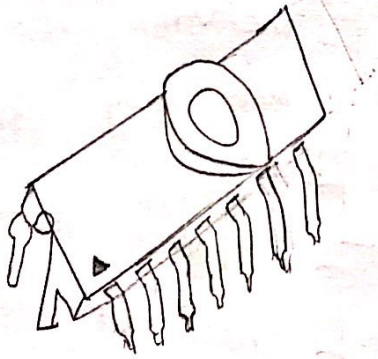
8-pin Metal can



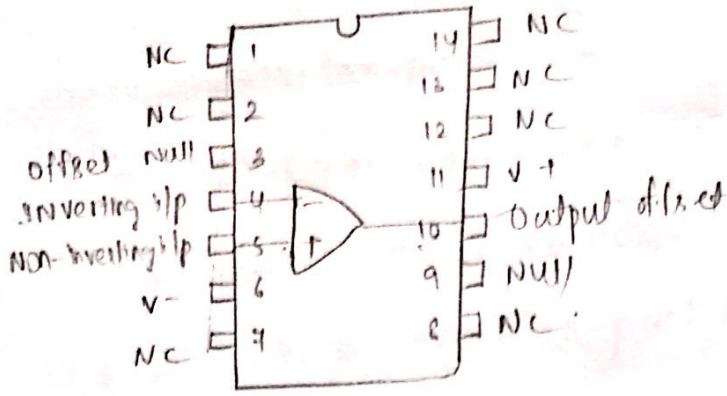
DUAL - IN - LINE PLASTIC PACKAGE



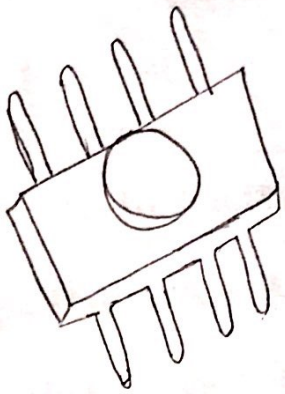
8-pin Mini DIP.



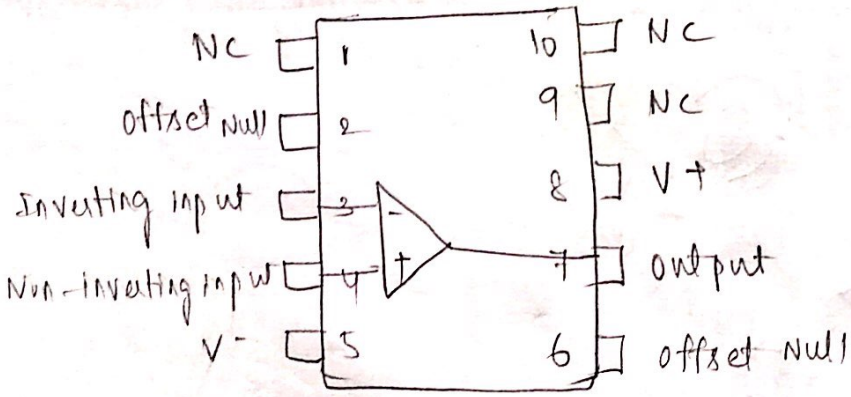
Dual - in line welded - seal ceramic package



Ceramic flat Package:



10 - PIN FLAT PACK



Logic families:- 12/10/2017

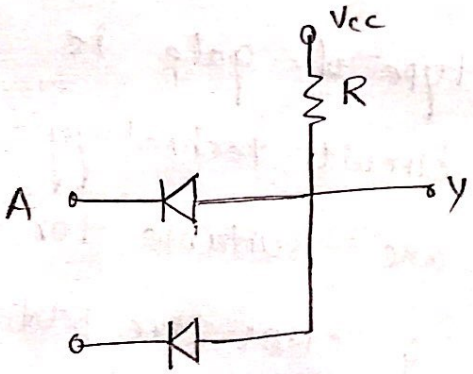
Many Logic families have been developed. They are Resistor Transistor logic (RTL), Direct coupled trasistor logic (DCTL), Diode Transistor logic (DTL), High Threshold logic (HTL), Transistor Transistor logic (TTL), Emitter coupled logic (ECL), Integrated Injection Logic (IIL), Metaloxide semiconductor logic (MOS). and complementary metaloxide semiconductor logic (CMOS). Out of these RTL, DCTL, DTL and HTL are absolute. The logic families TTL, ECL, IIL, MOS & CMOS are currently in use.

Basic function of any type of gate is always the same of the circuit technology used. The TTL and CMOS are suitable for SSI and MSI, The MOS & CMOS are particularly suitable for LSI. The IIL is mainly suitable for VLSI & ULSI. The ECL is mainly used in superfast computers.

comparision of Logic families.

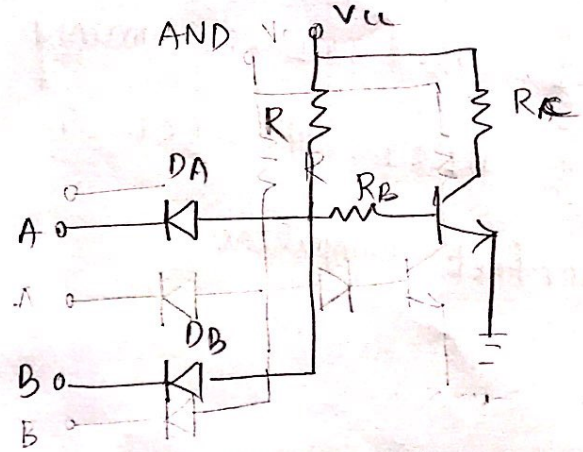
Logic family	Propagation delay time (ns)	Power-dissipation per gate (mW)	Noise margin (V)	fan-in	fan-out	cost
TTL	9	10	0.4	8	10	Low
ECL	1	50	0.25	5	10	High
MOS	50	0.1	1.5	10	10	Low
CMOS	<50	0.01	5	10	50	Low.
IIL	1	0.1	0.35	5	8	Very low

Diode Transistor :-



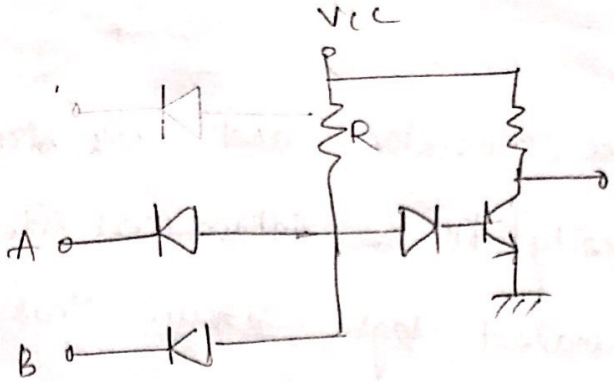
A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

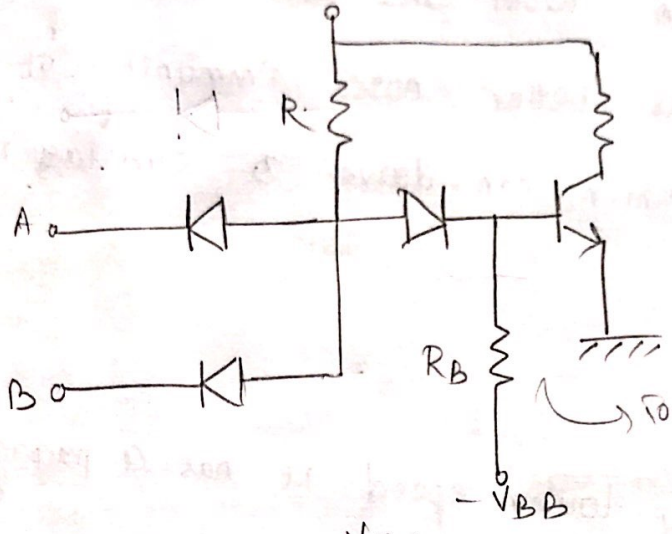
AND

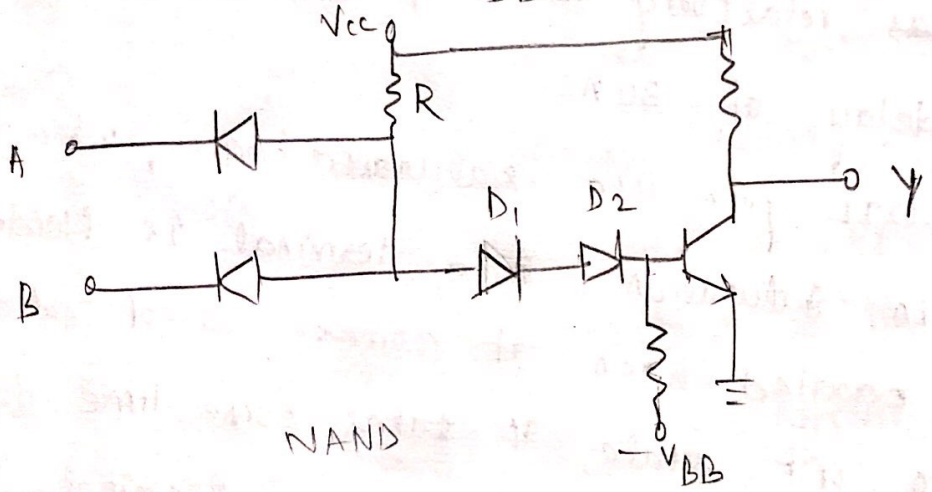


NAND Gate

Here we are getting Transistor as ON, so the output is '0'.







A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

DTL circuit has diodes as input network and Transistor as switching device. That's why this circuit is known as Diode Transistor logic.

Features :-

⇒ It consists of Diodes, Resistors and Transistors. It was the next family to be introduced after RTL. It is a saturated logic circuit that is it operates between cutoff and saturation region. Comparatively it has better noise immunity. It has a fan-out of 5 which can drive 5 similar DTL logic circuits.

Disadvantages :-

⇒ It has relatively lower speed. It has a propagation delay of 30 ns.

⇒ As DTL gate use saturated logic, when transistor in saturation Base terminal is flooded with carried when it comes out of saturation ie, to OFF state it takes some time for the carriers to leave the Base terminal. This is why there is a propagation delay in DTL circuits.

DTL NOR :-

A	B	V_o
0	0	1
0	1	0
1	0	0
1	1	0

Transistor - Transistor Logic (TTL) :-

The TTL family is so named because of its dependance on transistor alone to perform basic logic operations. It is the most popular logic family and widely used Bipolar digital IC family. The TTL uses transistors operating in saturated mode. It is the fastest of the saturated logic families. The basic TTL logic circuit is the NAND gate. Good speed, low manufacturing cost and the availability in SSI and MSI are its merits.

For standard TTL '0' volts to 0.8 volts is treated as logic '0' and 2 V to 5V is treated as logic '1'. Signals in 0.8 v to 2 v range

Should not be applied as input

Features:-

(1) It is the saturated logic.

(2) The Fan-out of 10 with high speed, easy interface.

(3) It uses multi emitter transistor at input which eliminates the need of input diodes like DTL.

(4) The no. of emitters will be equal to the number of input terminals and it is limited to 8. ie. Fan-out is '10'.

(5) we don't need the diodes at input which reduces the silicon chip area. The output structure can be classified as totem pole, open collector and tristate structure.

(6) It has high switching speed. In some case it is upto 125 MHz.

(7) It has small propagation delay above 9 ns.

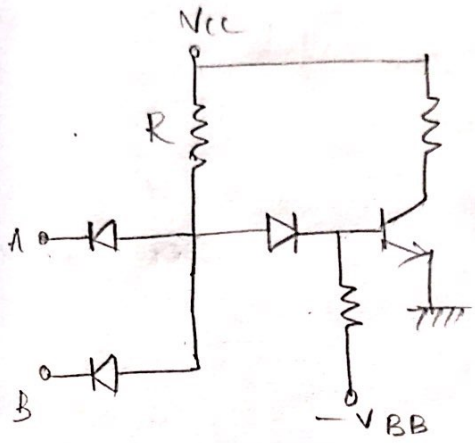
TTL IC is usually have 4 digits with 74 or 54 series. 74 series is the mostly used in digital IC. Ex: 7406, 7432, 7408, 7400.

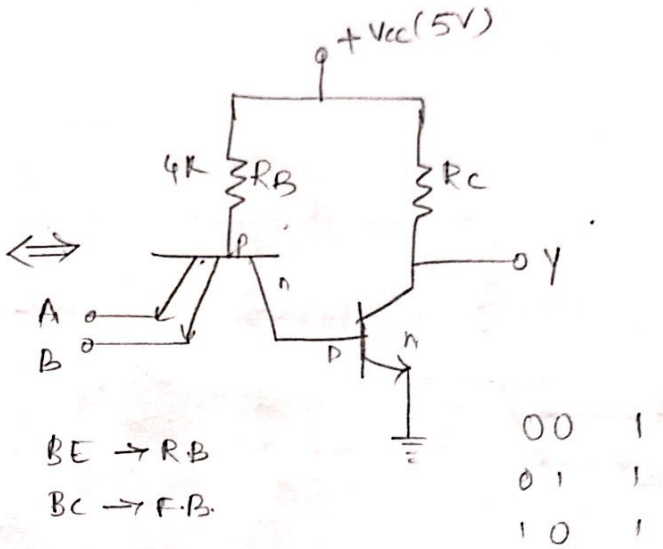
Disadvantages:-

(1) It has less noise immunity i.e. 0.4 V.

(2) It has high power consumption i.e. nearly 10 mW.

(3) There is internally generated noise spikes in TTL Totem pole circuit.

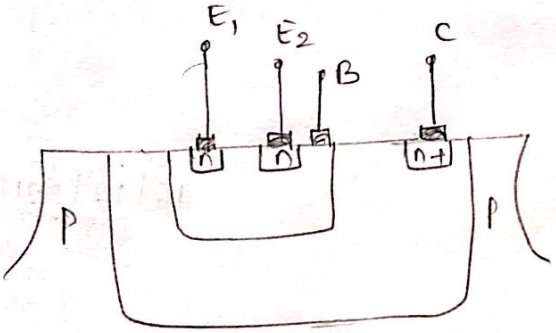




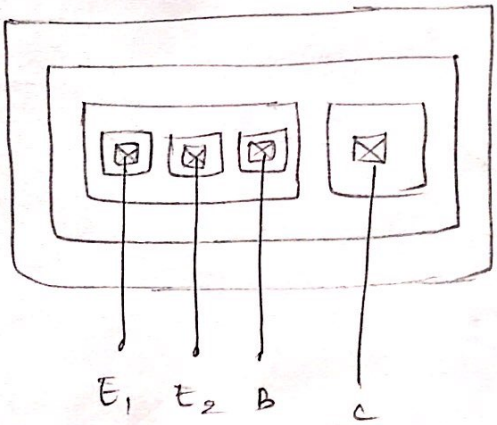
BE → R.B

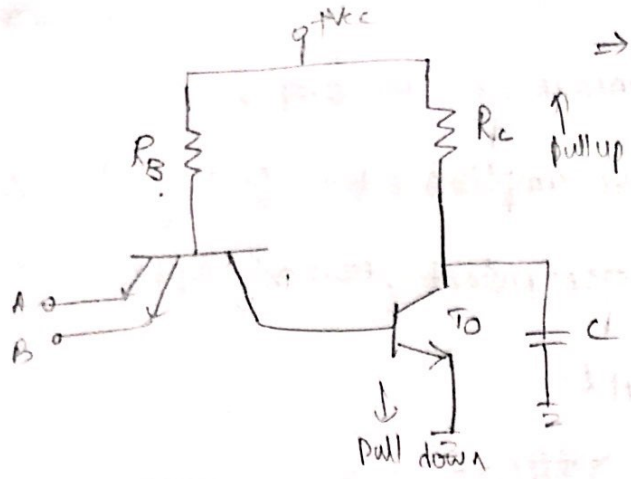
BC → F.B.

0 0	1
0 1	1
1 0	1
1 1	0



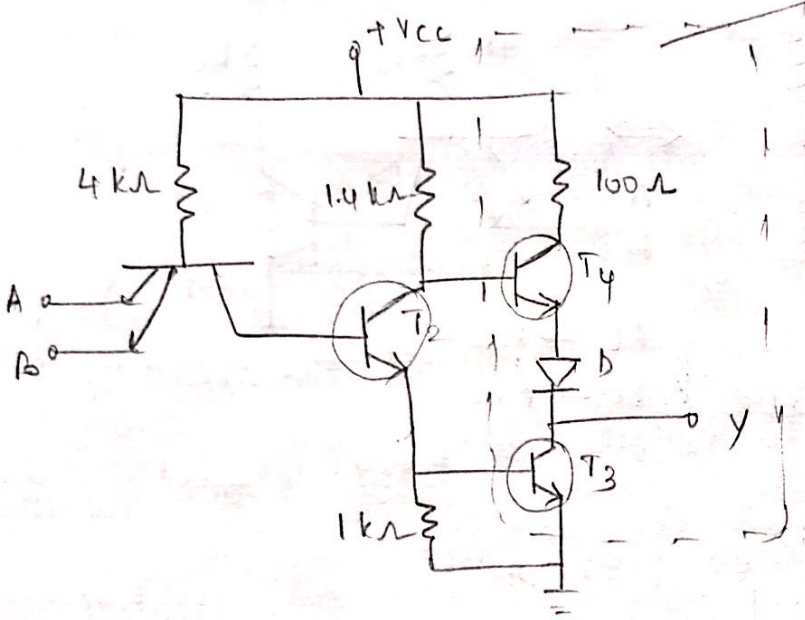
Top view





⇒ when T_0 is OFF, R_C is low

⇒ T_0 is ON, R_C is high

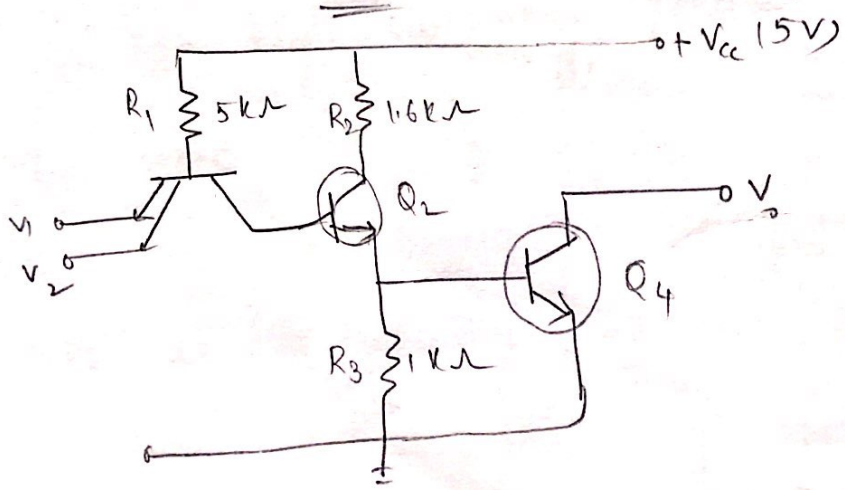


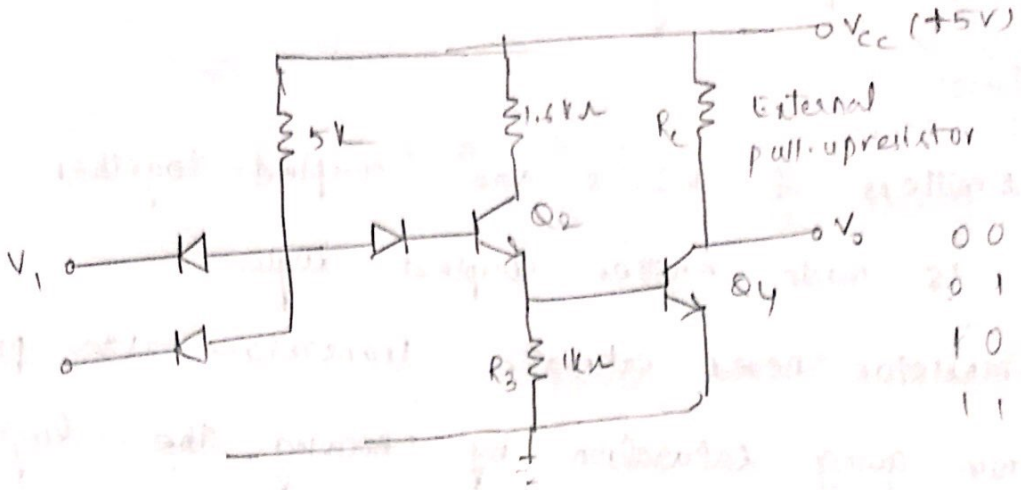
A	B	Y	
0	0	1	T_2, T_3 OFF, T_4 ON
0	1	1	
1	0	1	
1	1	0	T_2, T_3 ON, T_4 OFF

16/10/2017

Open collector TTL logic:-

NAND Gate

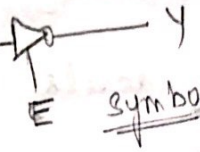




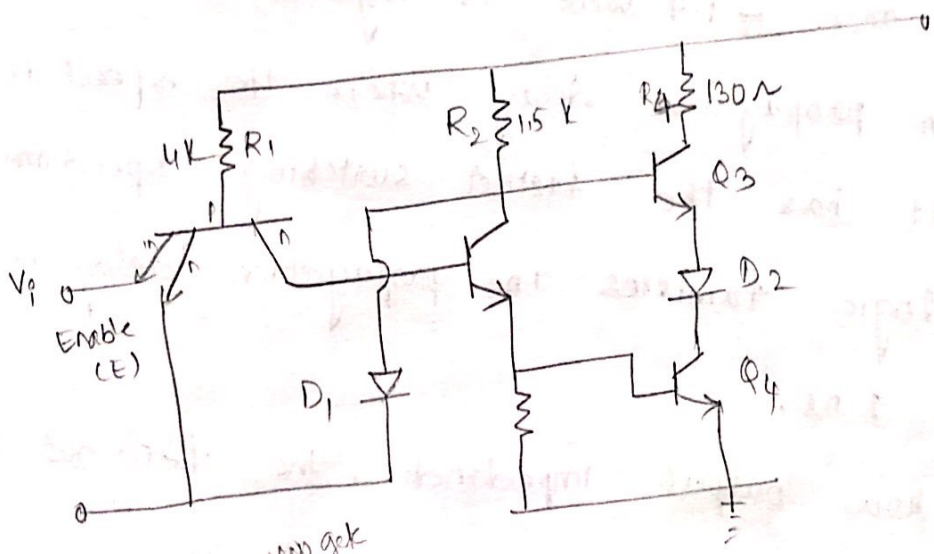
0	0	1
0	1	1
1	0	1
1	1	0

Notes in Text book:

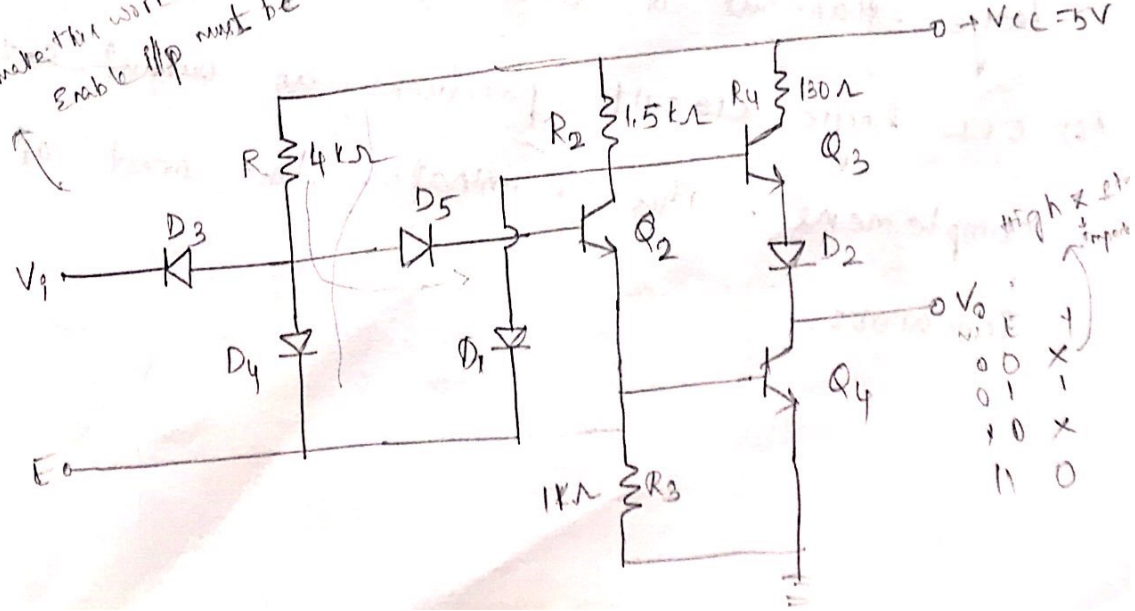
Tri-state TTL Logic:-



symbol



To make this work as NAND gate Enable i/p must be 1



high if all i/p

E	Y
0	X
0	1
1	X
1	0

Emitter coupled Logic (ECL):-

Features:-

(1) Emitters of BJT's are coupled together. Hence it is made emitter coupled - logic.

(2) Transistor never saturate, transistors are prevented from going saturation by choosing the logic levels close to one another storage delay in ECL circuit is eliminated.

(3) The Logic levels are normally -0.8 volts is logic 1 and -1.7 volts is logic '0'.

(4) Minimum propagation delay where the speed is high. It has the fastest switching speed among other logic families. The propagation delay is around 1 ns.

(5) Due to low output impedance, the fan-out is large. Fan-out of ECL is around 25.

(6) ECL logic ciacuit produces an output and its complement. This eliminates the need of Inverators.

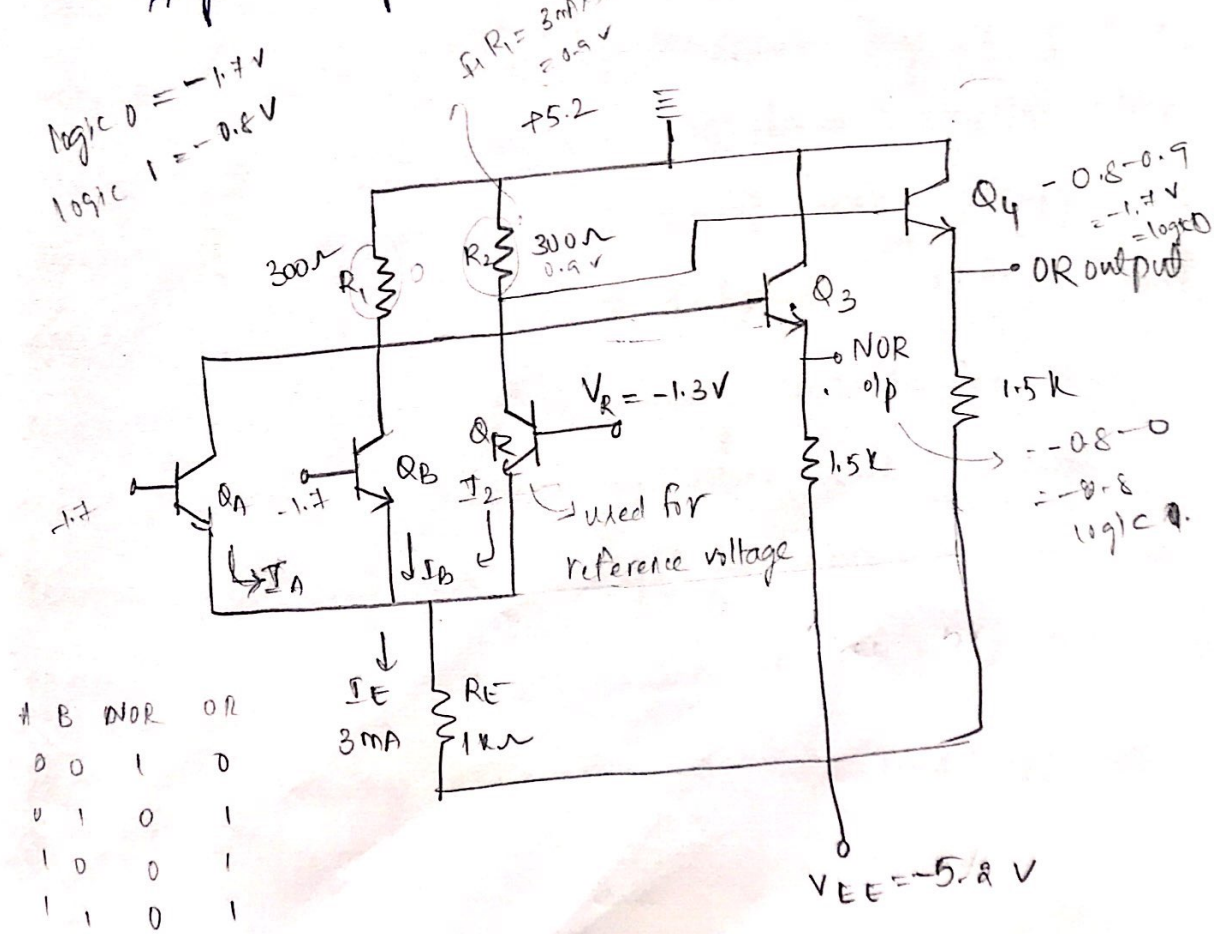
Disadvantages :-

(1) Having logic levels close to each other. It has low noise margin. around 0.25 volts. So ECL circuits are not suitable for heavy industrial environment.

(2) It requires relatively large silicon area and high cost.

(3) High power dessipation around 40 milliwatts.

(4) The ECL input and output are not electrically compatable for direct connection in any other logic family due to negative supply voltage and logic levels.



A	B	NOR	OR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1