UNIT-V

MOS LOGIC:-

Compared to Bipolar logic families, MOS families are simple and inexpensive to fabricate and it requires much less power have a better noise margin. A Greater supply voltage range. A higher fan-out and require much less chip-area, but they are slower in operating speed, for mos logic it is about 50ns and noise margin is 1.5V for +5volts supply and power dessipation is 0.1 mwatts and fan-out is 50. The propagation delay associated with MOS gates is large ie, 50nsec, because of their high output resistance, which is above 100kΩ and capacitance loading presented by the driven gates. The MOS logic is the simplest to fabricate and occupies very small space. because it requires only one element an N-MOS or P-MOS transistor. It doesn't require other elements like resistors and diodes which occupy large space because of its ease of fabrication and lower power dissipation per gate, it is ideally suitable for LSI, VLSI, OLSI for dedicated applications such as large memories, calculating chips, large microprocessor etc. The operating speed of MOS is lower than that of TTL, So they are hardly used in SSI and MSI applications.

The greater packing density of MOS IC's results in higher reliability because of its reduction in the no. of external connection. because of its very high impedance present at input of MOSFET, the MOS logic families are more succeptable to static charge damage. CMOS family is less succeptible to static charge damages.

There are 2 General types of MOSFET's.

(1) Depletion.

(2) Enhancement type

The MOS digital IC's use E-MOSFET. The MOSFETs are of N-MOSFET & P-MOSFET type. most modern MOSFET circuitry is constructed using N-MOS devices because they operate at about the 3 times the speed of their p-mos counter parts and also have twice the packing density of P-MOS. Both NMOS & P-MOS have greater packing density than that of CMOS. The CMOS family has the greatest complexity and lowest packing density of all MOS families, but it process the important advantages of high speed and much lower power dessipation. CMOS can be operated at high voltage resulting improved noise margin.

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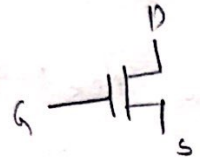
MOSFET

It has three regions

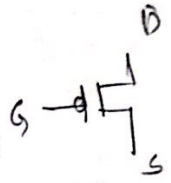
(1) cutoff ($V_{GS} < V_{DS}$) i.e. when $V_{GS} \simeq 0$

(2) Non saturation ($V_{DS} < V_{GS} - V_t$)
or
Triode region.

(3) saturation or active (or) constant ($V_{DS} \geq V_{GS} - V_t$)



NMOS



PMOS

Expression for Drain current in saturation.

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_t)^2$$

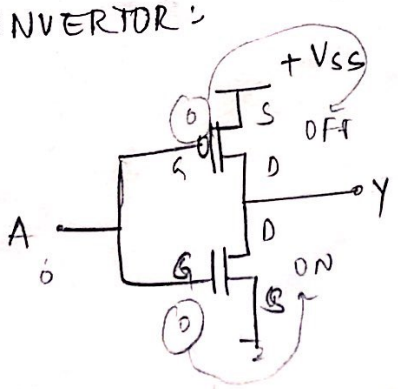
where C_{ox} = outside capacit
μ_n = electron mobilit
L = channel length

Expression for Drain current in non-saturation.

$$I_D = \frac{\mu_n C_{ox} W}{2L} \left\{ 2(V_{GS} - V_t) V_{DS} - V_{DS}^2 \right\}$$

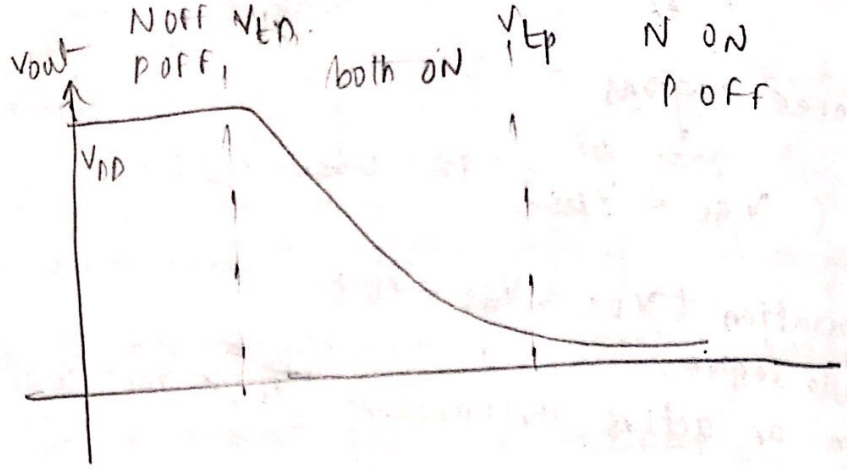
CMOS :-

CMOS INVERTOR :-



A	Y
0	1
1	0

transfer characteristics of CMOS inverter:



CMOS NAND:

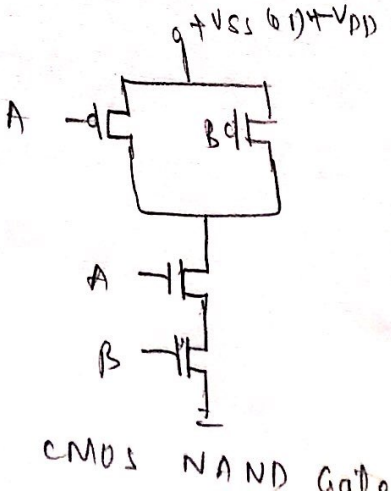
To implement nand using CMOS we need to follow the steps.

STEP 1:- Take complement of input $Y = \overline{A \cdot B}$

$\therefore \overline{Y} = A \cdot B$ No. of transistors = No. of I/Ps

1. Pull down – And – series
   or – parallel } NMOS

2. Pull up – AND – parallel } PMOS
   Or – Series



CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

1) $Y = (A \cdot B + C)D + E$

Sol:- $\overline{Y} = (AB + C)D + E$