**LAB 4: Finite State Machine as an Arbiter Circuit**

**Objectives:**

1. Design a sequential process using finite state machine.

2. Model control unit and an arbiter circuit for a CPU.

**a) Finite state machine**

A state diagram of a simple Mealy machine is shown in Figure 1. **Write the given program and**

**simulate the result.**



**Figure 1**: Simple Mealy machine

**b) Exercise: *Design of Arbiter Circuit***

Assume that there are three devices in the system, called device 1, device 2, and device 3. It is

easy to see how the FSM can be executed to handle more devices. The request signals are

named x1, x2 and x3 and the grant signals are called y1, y2 and y3. The devices are assigned a

priority level such that device 1 has the highest priority, device 2 has the next highest, and device 3 has the lowest priority. Thus if more than one request signal is asserted when the FSM assigns a grant, the grant is given to the requesting device that has the highest priority. Figure 2 depicted a state diagram of FSM for the *arbiter circuit*. **Write a VHDL code for the arbiter circuit based on the state diagram in Figure 2 and simulate the result.**



**Figure 2**: State diagram for the Arbiter