ANALOG VLSI DESIGN:

Analog VLSI design contributes the VLSI design and technology by the implementation of analog amplification circuits with respect to digital integration.

Analog Circuits such as Common Source amplifier, Common Gate amplifiers etc are implemented with respect to digital integration for amplification.

- On an observance analog contributes 20% and digital contributes 80%.

So, here we implement the analog circuits into CMOS transistor logic, for going digital integration, thus also studying there small signal model[1] becomes necessary.

Small Signal Models of a MOSFET: *(Considering nMOSFET)*

There are two types of small signal model of MOSFET i.e.:

1. Low Frequency Small Signal Model of MOSFET
2. High Frequency Small Signal Model of MOSFET

Low Frequency Small Signal Model of MOSFET:

In analog circuit, MOSFET devices are normally operated in saturation, here the drain current I_{ds} of nMOSFET can be written as,

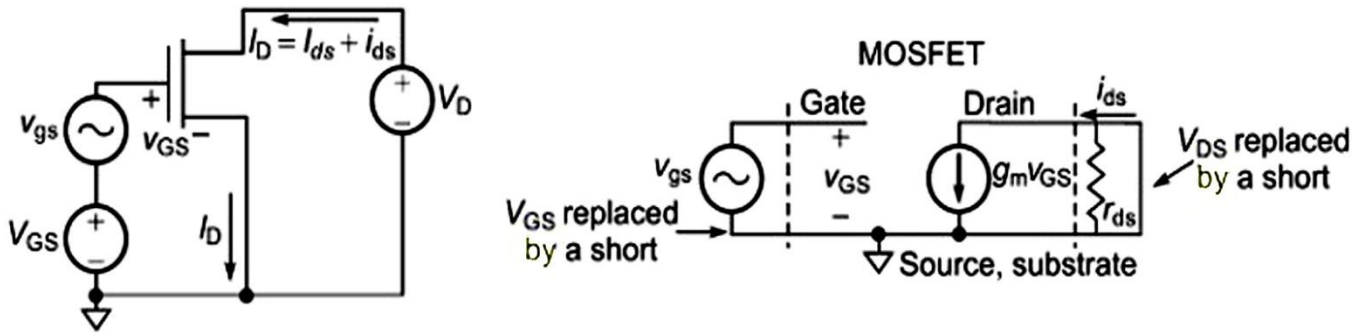
$$I_{ds} = \frac{\beta}{2}\left(v_{gs} - V_{THN}\right)^2\left[1 + \lambda_c\left(V_{ds} - V_{ds,sat}\right)\right]$$

Where:

$V_{ds,sat} \ll V_{ds}$

λ_c *is Channel length modulation parameter*

$\beta = \frac{\mu c_{ox} W}{L}$ (μ *is Electron Mobility,* c_{ox} *is Gate oxide capacitance,* W *is Width and* L *is the length*)



CIRCUIT OF MOSFET AND ITS LOW FREQUENCY SMALL SIGNAL MODEL

[1] ***Small signal models are used to analyze transistor circuits easily and rapidly. A small signal model is drawn by using simple approximations by retaining its essential features and discarding its less important features***

The circuit diagram of a nMOSFET and its small signal model is shown above, the dc sources are labelled say as V_{GS} and ac sources with their subscripts i.e. v_{gs} respectively.

Assuming $V_{GS} >> v_{gs}$. Since the MOSFET is in the saturation region, $V_{DS} > V_{GS} - V_{THN}$, the total (ac + dc) drain current is given as,

$$I_D = I_{ds} + i_{ds} = \frac{\beta}{2}\left(V_{GS} + v_{gs} - V_{THN}\right)^2(1 + \lambda_c V_{ds})$$

The forward transconductance, g_m, of the MOSFET is given as,

$$g_m = \left.\frac{\partial I_D}{\partial v_{GS}}\right|_{V_{GS}=Constant} = \beta\left(V_{GS} + v_{gs} - V_{THN}\right)(1 + \lambda_c V_{ds})$$

For the small signal low frequency ac equivalent circuit, it is seen that V_{ds} and V_{GS} are replaced by a short and for small signal, $v_{gs} << V_{GS}$. Since $\lambda_c < 1$ and $\lambda_c V_{ds} << 1$, hence the transconductance can be written as,

$$\boldsymbol{g_m = \beta(V_{GS} - V_{THN}) = \sqrt{2\beta I_{ds}}}$$

The output resistance is given as,

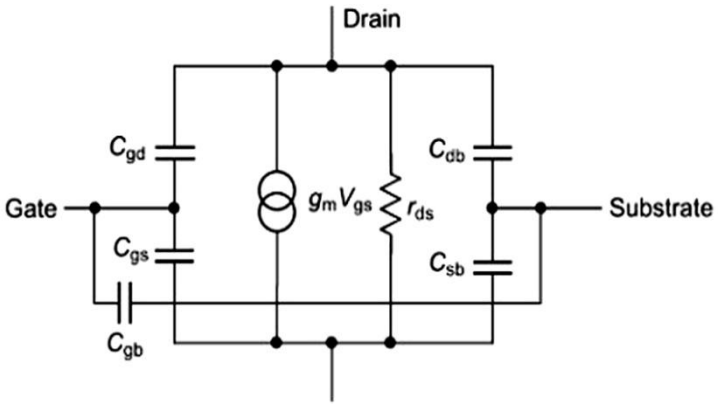
$$\boldsymbol{r_{out} = r_{ds} = \left.\frac{\partial V_{ds}}{\partial I_D}\right|_{V_{GS}=Constant} = \frac{1}{\beta(V_{GS} - V_{THN})^2\lambda_c} = \frac{1}{\lambda_c I_{ds}}}$$

The maximum voltage gain can be given as,

$$\boldsymbol{A_V = \frac{\partial V_{ds}}{\partial V_{gs}} = -\frac{1\Big/\frac{\partial V_D}{\partial V_{ds}}}{1\Big/\frac{\partial I_D}{\partial V_{gs}}} = -\frac{\sqrt{2\beta I_{ds}}}{\lambda_c I_{ds}} = -\frac{\sqrt{2\beta}}{\lambda_c\sqrt{I_{ds}}}}$$

High Frequency Small Signal Model of MOSFET:

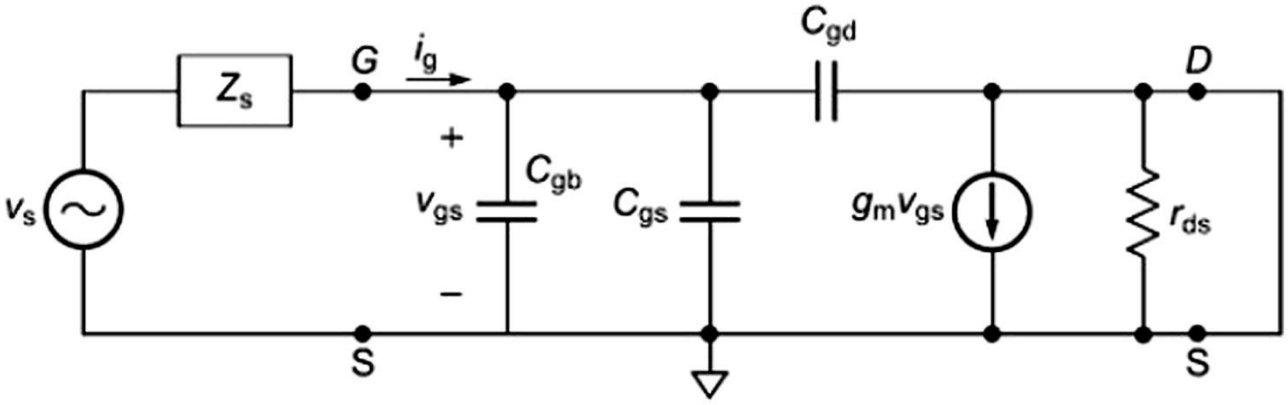
In the high frequency model of MOSFET, the MOSFET capacitances are considered as shown.



HIGH FREQUENCY SMALL SIGNAL MODEL

As seen the capacitances of drain diffusion region, source diffusion regions and gate over field region are denoted by C_{db}, C_{sb} and C_{gb}. The capacitances of gate- drain and gate- source are denoted by C_{gd} and C_{gs}.

The above high frequency small signal model can be further simplified as shown below,



SIMPLIFIED HIGH FREQUENCY SMALL SIGNAL MODEL

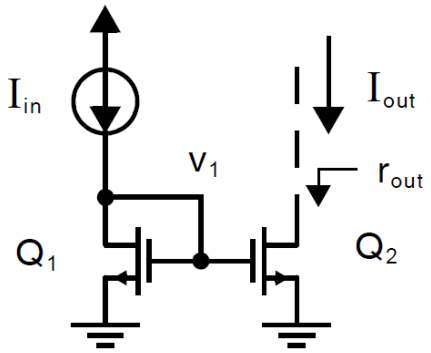
The current gain can be given as,

$$\frac{i_{ds}}{i_g} = \frac{\beta(V_{gs} - V_{THN})}{j2\pi f(C_{gb} + C_{gs} + C_{gd})}$$

What is a Current Mirror/ Ideal Current Mirror?

An ideal current mirror is a two-port circuit that accepts an input current I_{in} and produces and output current $I_{out} = I_{in}$. Since current sensing is best done with a low resistance, for example an ammeter, the ideal current source will have zero input resistance. An ideal current source has a high output resistance and, hence, so will an ideal current mirror. In this way, the ideal current mirror faithfully reproduces the input current regardless of the source and load impedances to which it is connected.

<u>Simple CMOS Current Mirror</u>:



A SIMPLE CMOS CURRENT MIRROR

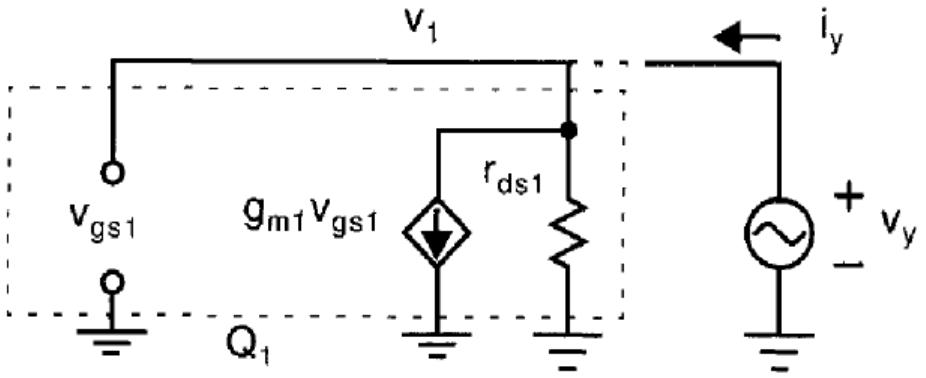
A simple CMOS current mirror is shown in figure, in which it is assumed that both the transistors are in the active region. If the finite output impedances of the transistors (Q_1 and Q_2) are ignored and are of same size, then Q_1 and Q_2 will have the same current since both have same gate- source voltage V_{gs}.

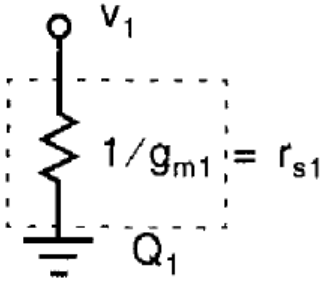
When considering finite output impedance, which ever transistor has a larger drain- source voltage V_{ds} will also have a larger current and the finite output impedance of the transistors will cause the small signal output impedance of the current mirror i.e. the small signal impedance looking into the drain of Q_2, to be less than infinite.

To find the output impedance of the current mirror, r_{out}, the small signal circuit is analyzed after placing a signal source $_X$, at the output node. As per definition,

$$r_{out} = \frac{V_X}{i_X}$$

Where i_X is the current flowing out of the source and into the drain of Q_2.





SMALL SIGNAL MODEL FOR Q_1 *EQUIVALENT SMALL SIGNAL MODEL FOR Q_1*

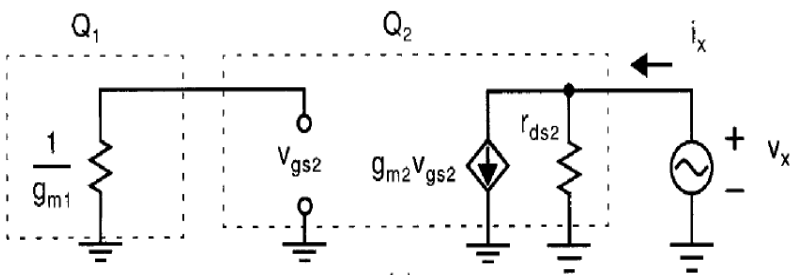
Consider the small signal model of Q_1 alone as shown which is a low frequency small signal model. It is to be noted that Q_1 is diode connected i.e. its drain and gate are connected and I_{in} does not exist in the small signal model, I_{in} is replaced with an open circuit because it is an independent current source. This model can further be reduced by Thevenins equivalent circuit. The Thevenins equivalent output voltage is 0 since the circuit is stable and contains no input signal. This circuit's Thevenins equivalent output impedance is found by applying a test signal voltage, V_y at V_1 and measuring the signal current, i_Y, as shown. Here the current i_y is given as,

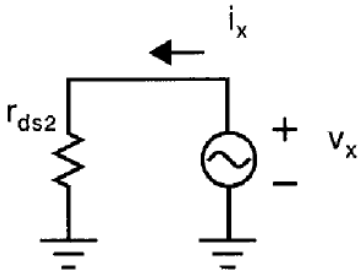
$$\boldsymbol{i_y = \frac{V_y}{r_{ds1}} + g_{m1}V_{gs1} = \frac{V_y}{r_{ds1}} + g_{m1}V_y}$$

Recalling the output impedance is given by,

$$r_{out} = \frac{V_y}{i_y} = \frac{1}{g_{m1}} || \, r_{ds1}$$

This is because $r_{ds1} >> 1/ g_{m1}$. We approximate the output impedance equal to $1/ g_{m1}$, which results in the equivalent model as shown for Q_1.



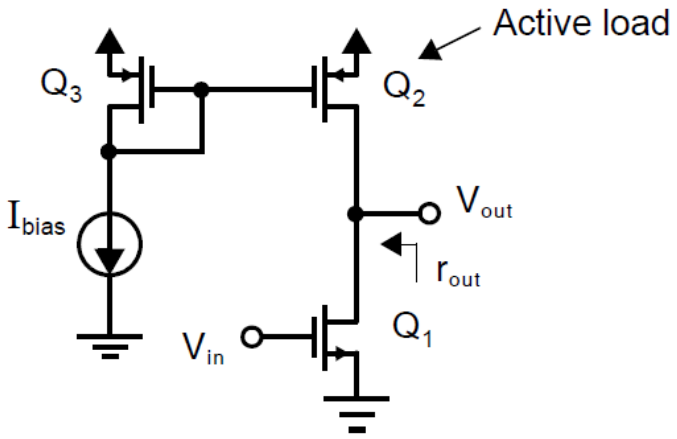


SMALL SIGNAL MODEL FOR CMOS CURRENT MIRROR *EQUIVALENT SMALL SIGNAL MODEL FOR CMOS CURRENT MIRROR*

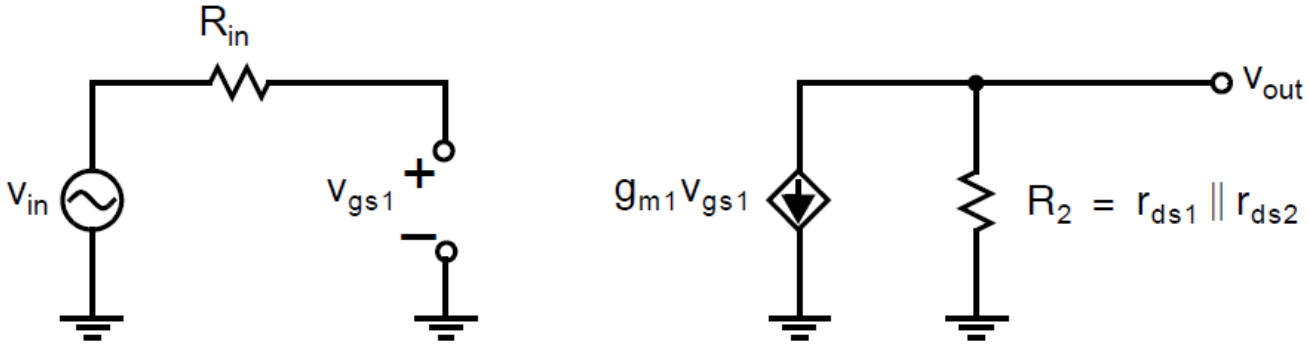
Further we lead to the small signal model of the CMOS current mirror as shown, where V_{gs2} has been connected to ground via a resistance of $1/ g_{m1}$. Since no current flows through $1/ g_{m1}$ resistor, $V_{gs2} = 0$, no matter what voltage V_x is applied to the current mirror output. This is no surprise since MOS transistors operate unilaterally at low frequencies. Thus, since $g_{m2} V_{gs2} = 0$, the circuit is simplified to the equivalent small signal model as shown. The small signal output impedance, r_{out} is equal to r_{ds2}.

Therefore, a simple CMOS current mirror has a small-signal input resistance of $1/ g_{m1}$ *and a small-signal output resistance* r_{ds2}.

Common Source Amplifier:



A COMMON SOURCE AMPLIFIER



SMALL SIGNAL EQUIVALENT MODEL FOR COMMON SOURCE AMPLIFIER

The common-source amplifier is a popular gain stage, especially when high input impedance is desired as shown. The use of an active load takes advantage of the nonlinear, large-signal transistor current–voltage relationship to provide large small-signal resistances without large dc voltage drops.

Here, an n- channel common-source amplifier has a p- channel current mirror used as an active load to supply the bias current for the drive transistor. By using an active load, a high- impedance output load can be realized without using excessively large resistors or a large power- supply voltage. As a result, for a given power supply voltage, a larger voltage gain can be achieved using an active load than would be possible if a resistor were used for the load.

For example, if a 100 kΩ load were required with a bias current, a resistive- load approach would require a power- supply voltage of 100 kΩ × 100 μA. An active load takes advantage of the nonlinear, large-signal transistor current voltage relationship to provide large small-signal resistances without large dc voltage drops.

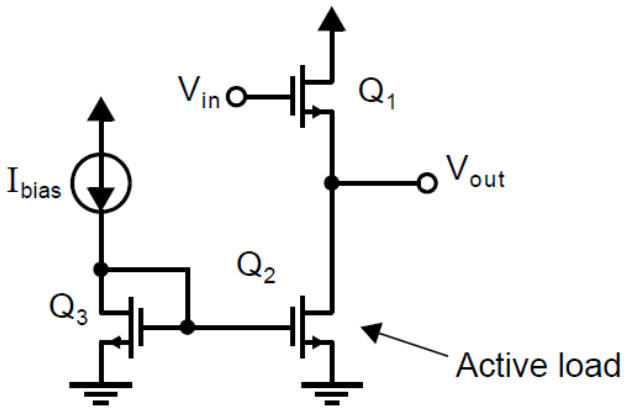
The small- signal equivalent circuit for the low-frequency analysis of the common-source amplifier as shown, where V_{in} and R_{in} are the Thévenin equivalent of the input source. It is assumed that the bias voltages are such that both transistors are in the active region. The output resistance, R_2- is made up of the parallel combination of the drain- to- source resistance of Q_1, i.e. r_{ds1}, and the drain- to- source resistance of Q_2, i.e. r_{ds2}. Notice that the voltage- controlled current source modeling the body effect has not been included since the source is at a small signal ground, and, therefore, this source always has 0 current.

Using the small signal analysis, we have $v_{gs1} = v_{in}$ and, therefore,

$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1}R_2 = -g_{m1}(r_{ds1} \parallel r_{ds2})$$

Depending on the device sizes, currents, and the technology used, a typical gain for this circuit is in the range of -5 to -100. To achieve similar gains with resistive loads, much larger power-supply voltages must be used which also greatly increases the power dissipation.

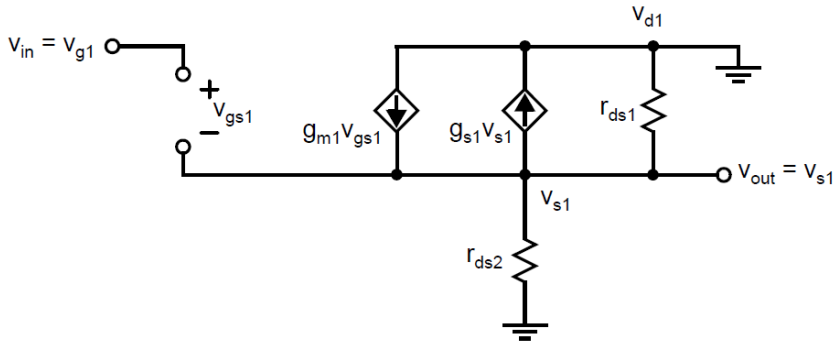
<u>Common Drain Amplifier or Source Follower</u>:



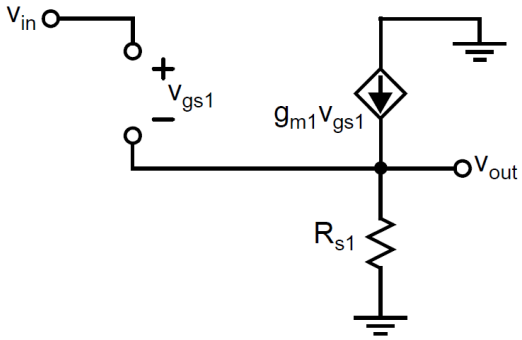
A COMMON DRAIN AMPLIFIER OR SOURCE FOLLOWER

A general use of current mirrors is to supply the bias current of source- follower amplifiers, as shown. Here Q_1 is the source follower and Q_2 is an active load that supplies the bias current of Q_1. These amplifiers are commonly used as *voltage buffers* and are therefore commonly called source followers.

They are also referred to as common-drain amplifiers, since the input and output nodes are at the gate and source nodes respectively, with the drain node being at small-signal ground. Although the dc level of the output voltage is not the same as the dc level of the input voltage, ideally the small-signal voltage gain is close to unity. In reality, it is somewhat less than unity. However, although this circuit does not generate voltage gain, it does have the ability to generate current gain.



LOW FREQUENCY SMALL SIGNAL MODEL



EQUIVALENT SMALL SIGNAL MODEL

It is to be noted that the voltage-controlled current source that models the body effect of MOS transistors has been included because the source is not at small- signal ground. The body effect is a major limitation on the small signal gain. From the small signal it is seen that r_{ds1} is parallel to r_{ds2}, also that the voltage-controlled current source modelling the body effect produces a current that is proportional to the voltage across it. This relationship makes the body effect equivalent to a resistor of size $1/ g_{s1}$, which is also in parallel with r_{ds1} and r_{ds2}. Thus the small signal model is reduced to equivalent small signal model as shown in which $R_{s1} = r_{ds1} \parallel r_{ds2} \parallel 1/ g_{s1}$.

Now writing the nodal equation at V_{out}, and noting that $V_{gs1} = V_{in} – V_{out}$, we have,

$$v_{out}/R_{s1} - g_{m1}(v_{in} - v_{out}) = 0$$

To minimize circuit equation errors, a consistent methodology should be maintained when writing nodal equations. The methodology employed here is as follows: The first term is always the node at which the currents are being summed. This node voltage is multiplied by the sum of all admittances connected to the node. The next negative terms are the adjacent node voltages, and each is multiplied by the connecting admittance. The last terms are any current sources with a multiplying negative sign used if the current is shown to flow into the node.

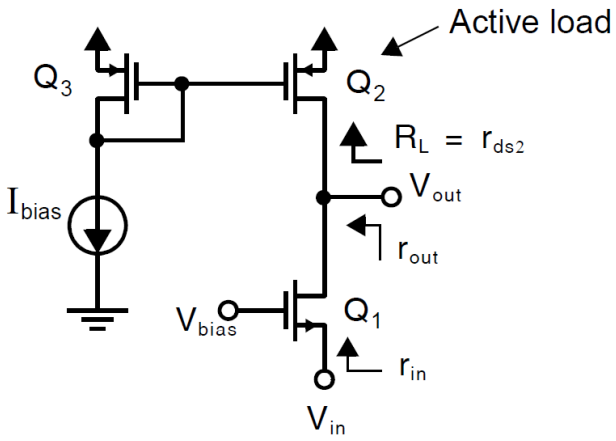
Solving for V_{out}/ V_{in}, we have,

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + G_{s1}} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} = g_{m1}\left(\frac{1}{g_{m1}} \parallel \frac{1}{g_{s1}} \parallel r_{ds1} \parallel r_{ds2}\right)$$

Normally, g_{s1} is on the order of one-tenth to one-fifth that of g_{m1}. Also, the transistor output admittances, g_{ds1} and g_{ds2}, might be one-tenth that of the body-effect parameter, g_{s1}. Therefore, it is seen that the body-effect parameter is the major source of error causing the gain to be less than unity. Notice also that at low frequencies the stage is completely unilateral. In other words, there is no signal flow from the output to the input.

Common Gate Amplifier:

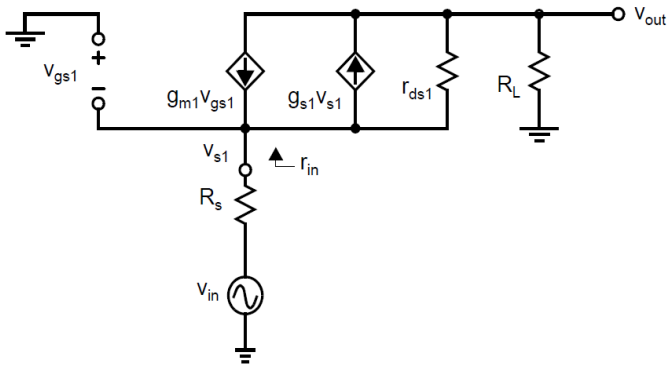
The common-gate amplifier as shown provides a voltage gain comparable to that of the common-source amplifier, but with a relatively low input resistance on the order of $1/g_m$.



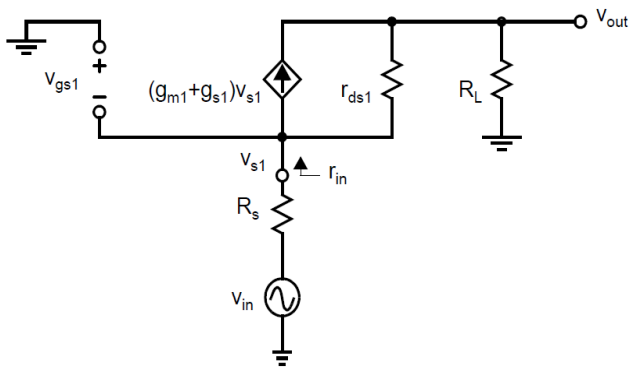
A COMMON GATE AMPLIFIER- WITH CURRENT MIRROR ACTIVE LOAD

A common application for a common- gate amplifier is as the first stage of an amplifier where the input signal is a current, in such cases a small input impedance is desired in order to ensure all of the current signal is drawn into the amplifier, and none is "lost" in the signal source impedance. Aside from its low input impedance, the common gate amplifier is similar to a common-source amplifier, in both cases the input is applied across V_{gs}, except with opposite polarities, and the output is taken at the drain. Hence, in both cases the small signal gain magnitude approximately equals the product of g_m and the total impedance at the drain.

If we use straightforward small-signal analysis, when the impedance seen at (in this case, the output impedance of the current mirror formed by Q_2) is much less than r_{ds1}, the input impedance, r_{out}, is found to be $1/ g_{m1}$ at low frequencies. However, in integrated applications, the impedance seen at V_{out} is often on the same order of magnitude or even much greater than r_{ds1}. In this case, the input impedance at low frequencies can be considerably larger than $1/ g_{m1}$. To see this result, consider the small-signal model as shown. In this model, the voltage-dependent current source that models the body effect has been included. It is noticed that $V_{gs1} = - V_{s1}$ and therefore the two current sources can be combined into a single current source, as shown in the simplified small signal model. This simplification is always possible for a transistor that has a grounded gate in a small-signal model, and considerably simplifies taking the body effect into account.



LOW FREQUENCY SMALL SIGNAL MODEL



EQUIVALENT OR SIMPLIFIED SMALL SIGNAL MODEL

The body effect for transistors with grounded gates can be ignored, and then, after the analysis is complete, simply replace the constants g_{mi} with $g_{mi} + g_{si}$. However, now we include the body-effect parameter throughout the analysis.

At node V_{out}, we have

$$v_{out}(G_L + g_{ds1}) - v_{s1}g_{ds1} - (g_{m1} + g_{s1})v_{s1} = 0 \quad \text{(Equation 1)}$$

Rearranging slightly, we have,

$$\frac{v_{out}}{v_{s1}} = \frac{g_{m1} + g_{s1} + g_{ds1}}{G_L + g_{ds1}} = (g_{m1} + g_{s1} + g_{ds1})(R_L \parallel r_{ds1}) \cong g_{m1}(R_L \parallel r_{ds1}) \quad \text{(Equation 2)}$$

Here the gain is approximately equal to $g_{m1}/(G_L + g_{ds1})$.

The current going into the source of Q_1 is given by,

$$i_s = v_{s1}(g_{m1} + g_{s1} + g_{ds1}) - v_{out}g_{ds1} \quad \text{(Equation 3)}$$

Combining equations 2 and 3 to find the input admittance $y_{in} = 1/r_{in}$ we have,

$$y_{in} = \frac{i_s}{v_{s1}} = \frac{g_{m1}+g_{s1}+g_{ds1}}{1+\frac{g_{ds1}}{G_L}} = \frac{g_{m1}}{1+\frac{g_{ds1}}{G_L}} \quad \text{(Equation 4)}$$

Alternatively, we have,

$$r_{in} = \frac{1}{y_{in}} = \frac{1}{g_{m1}}\left(1 + \frac{R_L}{r_{ds1}}\right)$$

With the p- channel active load, $R_L = r_{ds2}$. Since, in this case, is approximately the same magnitude as r_{ds1}, the input impedance, r_{in}, is about $2/ g_{m1}$for low frequencies- twice as large as the expected value of $1/ g_{m1}$. This increased input impedance must be taken into account in applications such as transmission- line terminations. In some examples, the current-mirror output impedance realized by is much larger than (i.e. $R_L >> r_{ds1}$,), and so the input impedance for this common-gate amplifier is much larger than $1/ g_{m1}$. This increased input impedance often occurs in integrated circuits and is not commonly known.

The attenuation from the input source to the transistor source can be considerable for a common-gate amplifier when R_s is large. This attenuation is given by,

$$\frac{V_{s1}}{V_{in}} = \frac{G_s}{G_s + y_{in}}$$

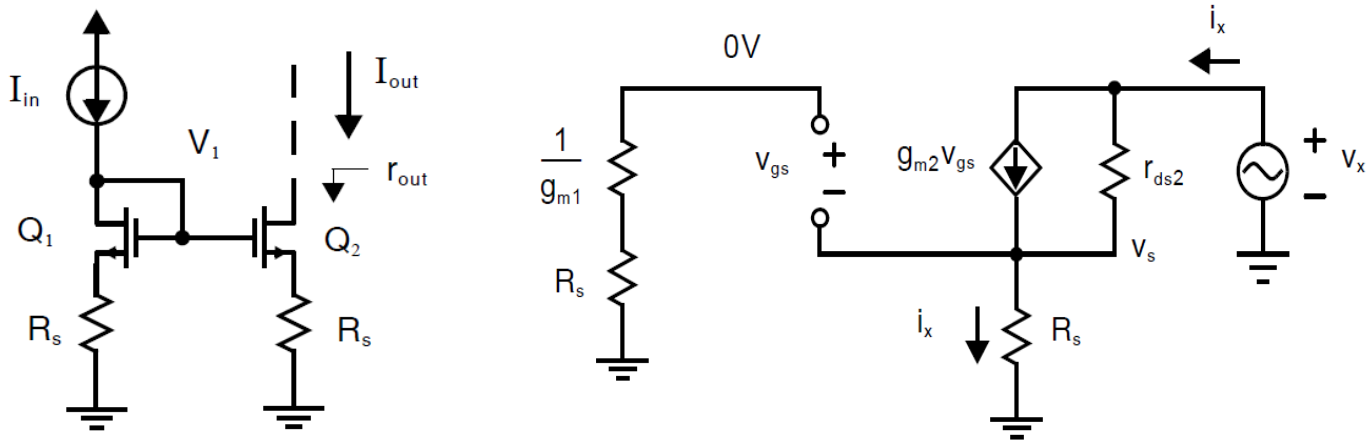
Using equation 4 to replace y_{in}, we have- using admittance- divider rule,

$$\frac{V_{s1}}{V_{in}} = \frac{G_s}{G_s + \frac{g_{m1}}{1+\frac{g_{ds1}}{G_L}}} \quad \text{(Equation 5)}$$

Using equation 2 and 5, to find the overall dc gain- which is given as,

$$A_V = \frac{V_{out}}{V_{in}} = \left[\frac{G_s}{\left(G_s + \frac{g_{m1}}{1 + \frac{g_{ds1}}{G_L}}\right)}\right] \frac{g_{m1}}{G_L + g_{ds1}}$$

Source Degenerated Current Mirror:



SOURCE DEGENERATED CURRENT MIRROR AND ITS SMALL SIGNAL MODEL

A source degenerated current mirror is used to increase the output impedance. A source degenerated current mirror is shown along with its small signal model.

Here since no current flow through the gate, the gate voltage is 0 V. The current i_x sourced by the applied voltage source is equal to the current through the degeneration resistor R_s. Therefore, we have,

$$v_s = i_x R_s \quad \text{(Equation 1)}$$

And

$$v_{gs} = -v_s \quad \text{(Equation 2)}$$

Setting i_x equal to the total current through g_{m2} V_{gs} and r_{ds2} gives,

$$i_x = g_{m2} v_{gs} + \frac{v_x - v_s}{r_{ds2}} \quad \text{(Equation 3)}$$

Substituting equation 1 and 2 in 3 gives,

$$i_x = -i_x g_{m2} R_s + \frac{v_x - i_x R_s}{r_{ds2}} \quad \text{(Equation 4)}$$

Rearranging, we find the output impedance to be given as,

$$r_{out} = \frac{v_x}{i_x} = r_{ds2}[1 + R_s(g_{m2} + g_{ds2})] \cong r_{ds2}(1 + R_s g_{m2}) \quad \text{(Equation 5)}$$

Where g_{ds2} is equal to $1/ r_{ds2}$, which is much less than g_{m2}.

Since the gate is at a small signal ground, the body effect can be considered by replacing g_{m2} in the above equation with $g_{m2} + g_{s2}$.

Therefore equation 5 becomes,

$$r_{out} = \frac{v_x}{i_x} = r_{ds2}[1 + R_s(g_{m2} + g_{s2} + g_{ds2})] \cong r_{ds2}[1 + R_s(g_{m2} + g_{s2})]$$

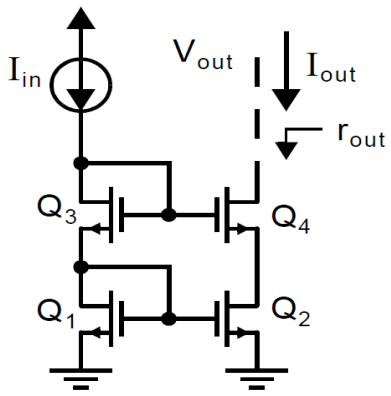
HIGH OUTPUT IMPEDANCE CURRENT MIRRORS:

The current mirrors which have output impedances that are larger than that of a simple current mirror by a factor of $g_m r_{ds}$- the maximum gain of a single transistor are **high output impedance current mirrors**.

The two types of high output impedance current mirrors are:

1. Cascode Current Mirror
2. Wilson Current Mirror

Cascode Current Mirror:



CASCODE CURRENT MIRROR

A cascode current mirror is shown in figure, where the output impedance looking into the drain of Q_2 is r_{ds2}, which is analysed very similar to the analysis of a simple current mirror. Therefore the output impedance can be immediately derived by considering Q_4 as a current source with a source degeneration resistor of value equal to r_{ds2}.

It is to be noted that the addition of a cascode device to a CMOS current mirror increases its output resistance by approximately the gain of the cascode device, $g_m r_{ds}$.
Using,

$$r_{out} = \frac{v_x}{i_x} = r_{ds2}[1 + R_s(g_{m2} + g_{ds2})] \cong r_{ds2}(1 + R_s g_{m2})$$

And noting that Q_4 is now the cascode transistor rather than Q_2, we have,

$$r_{out} = r_{ds4}[1 + R_s(g_{m4} + g_{s4} + g_{ds4})]$$

Where now Rs = r_{ds2}. Therefore the output impedance is given as,

$$\begin{aligned} r_{out} &= r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4} + g_{ds4})] \\ &\cong r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4})] \\ &\cong r_{ds4}(r_{ds2} g_{m4}) \end{aligned}$$

Thus, the output impedance has been increased by a factor of $g_m r_{ds2}$, which is an upper limit on the gain of a single transistor MOS gain- stage, and might be a value between 10 and 100, depending on the transistor sizes and currents and the technology being used. This significant increase in output impedance can be instrumental in realizing single stage amplifiers with large low frequency gains.

The disadvantage in a cascode current mirror is that it reduces the maximum output signal swings possible before transistors enter the triode region. This can be illustrated by having a n- channel transistor to be in the active region- also called the saturation or pinch- off region, its drain- source voltage must be greater than V_{eff}, where V_{eff} is,

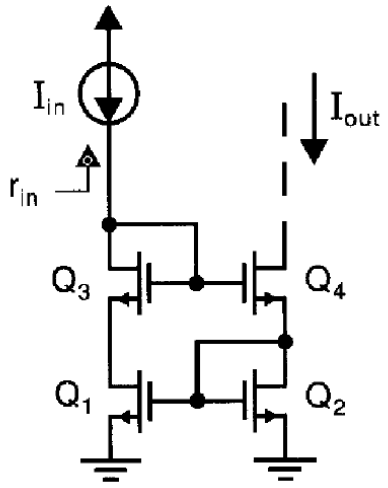
$$V_{eff} \equiv V_{GS} - V_{tn}$$

Which is further given by,

$$V_{eff} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

Wilson Current Mirror:

The Wilson current mirror is an example of using shunt- series feedback to increase the output impedance. The Wilson current mirror is shown in figure.



WILSON CURRENT MIRROR

Here Q_2 senses the output current and then the mirrors it to I_{D1}, which in turn is subtracted from the input current I_{in}, it is to be noted that I_{D1} must be precisely equal I_{in}- otherwise the voltage at the gate of Q_3, Q_4 would either increase or decrease, and the negative feedback loop forces this equality. This feedback arrangement increases the output impedance by an amount equal to 1 plus the loop gain.

Assuming all devices are matched, the output impedance without the feedback due to Q_1, Q_3 would be 2 r_{ds4}, taking into account that Q_4 has source degeneration equal to 1/ g_{m2} (i.e. the small signal impedance of diode connected Q_2), which is responsible for the 2 factor.

The loop gain is approximately given as,

$$A_L = \frac{g_{m1}(r_{ds1} || r_{in})}{2}$$

Where r_{in} is the input impedance of the biasing current source I_{in}.

The factor of 1/ 2 is due to the voltage attenuation from the gate of Q_4 to its source, caused by the source degeneration of the diode connected Q_2.

Assuming r_{in} is approximately equal to r_{ds1}, then the loop gain is given by,

$$A_L = \frac{g_{m1} r_{ds1}}{4}$$

And the output impedance is therefore given as,

$$r_{out} = r_{ds4} \frac{g_{m1}(r_{ds1} || r_{in})}{2} = r_{ds4} \frac{g_{m1} r_{ds1}}{2}$$

It is seen from the equation of output impedance that the output impedance of the Wilson current mirror is roughly one- half the output impedance for that of a cascode current mirror. For this reason the cascode current mirror is often preferred over the Wilson current mirror.

The output voltage swing, the minimum allowed voltage across the current mirror before Q_4 enters the triode region is $2 V_{eff1} + V_{in}$, which is similar to that of the cascode current mirror.

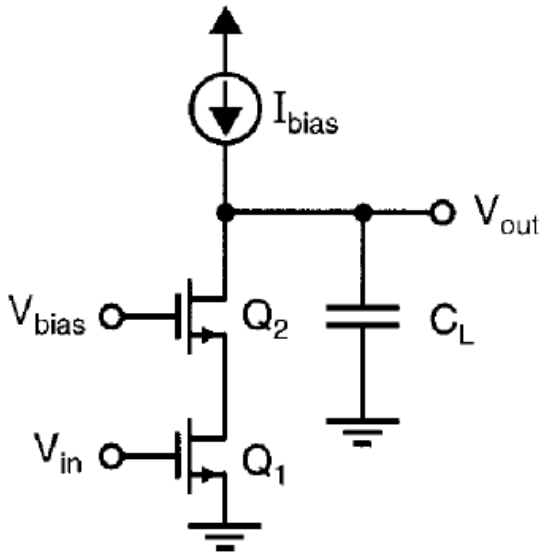
Therefore, it is noted that in the Q_3 is not required in the Wilson current mirror, it has been included to give Q_1 and Q_2 the same drain- source bias voltages and thus minimizes the inaccuracies caused by the large signal output impedances of the transistors. Without this transistor the output current would be slightly smaller than the input current because V_{DS1} would be larger than V_{DS2}, keeping the small signal output impedance remaining the same.

Cascode Amplifier or Cascode Gain Stage:

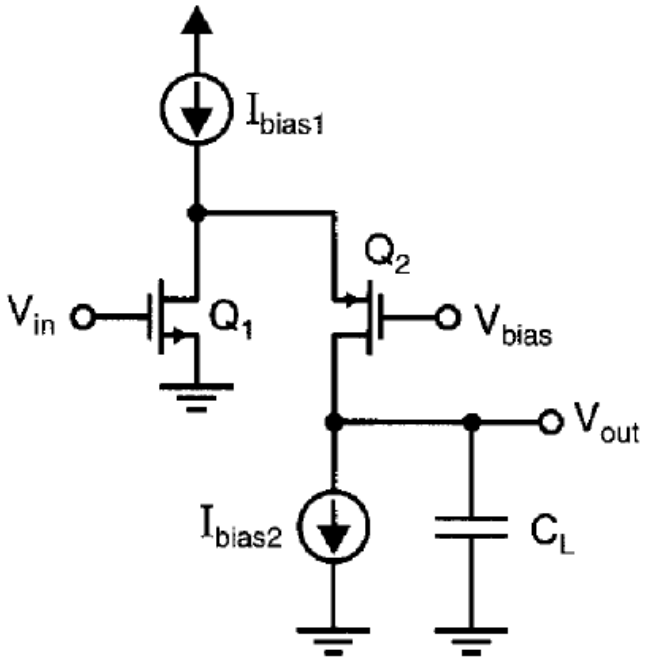
The cascode amplifier is commonly used configuration in digital IC design which consists of a common source connected transistor feeding into a common gate connected transistor.

Two illustrations/ types of cascode amplifiers are:

1. Telescopic cascode amplifier
2. Folded- cascode amplifier



TELESCOPIC CASCODE AMPLIFIER



FOLDED CASCODE AMPLIFIER

As seen telescopic cascode amplifier has both common n- channel transistors Q_1- common source and Q_2- common gate, this is referred as a *telescopic cascode amplifier* and as seen a folded cascode amplifier has a n- channel common source transistor Q_1 and a p- channel common gate , this is referred as a *folded cascode amplifier*.

The folded cascode amplifier allows the dc level of the output signal to be the same as the dc level of the input signal, but this folded cascode amplifier is slower than the telescopic cascode amplifier because of the impedance levels of the folded cascode is roughly three times larger due to the smaller transconductance of the p- channel transistors as compared to n- channel transistors, although parasitic capacitances at the source of the cascode transistor are similar in both the amplifier cases.

There are two major reasons for the demand of these amplifier stages i.e.:

1. They can have larger gain for a single stage due to large impedances at the output- to enable this high gain the current sources connected to the output nodes are realized using high quality cascode current mirrors. This gain is obtained without degradation in speed and sometimes also with an increase in speed.
2. They limit the voltage across the input drive transistor- this minimizes any shorted short channel effects which becomes more important with modern technologies having very low short channel length transistors.

The analysis of the cascode gain stage/ amplifier is based on the telescopic stage,

WKT, using current mirrors, the impedance looking into the drain of cascode transistor Q_2 is approximately given by,

$$r_{d2} = g_{m2}\, r_{ds1}\, r_{ds2}$$

The total impedance at the output node is r_{ds2} in parallel with R_L, where R_L is the output impedance of the bias current source, I_{bias}. Assuming I_{bias} is a high quality source with output impedance of the order of,

$$R_L = g_{m-p}\, r^2_{ds-p} \qquad \text{(Equation 1)}$$

Then the total impedance at the output node is,

$$R_{out} = \frac{g_m\, r^2_{ds}}{2} \qquad \text{(Equation 2)}$$

Now, to find the approximate low- frequency gain, we use a part of the analysis of the common gate amplifier. i.e.

$$y_{in} = \frac{i_s}{v_{s1}} = \frac{g_{m1} + g_{s1} + g_{ds1}}{1 + \frac{g_{ds1}}{G_L}} = \frac{g_{m1}}{1 + \frac{g_{ds1}}{G_L}}$$

Therefore, the low frequency impedance looking into the source of the common gate or cascode, transistor Q_2 is given as,

$$y_{in2} = \frac{g_{m2} + g_{s2} + g_{ds2}}{1 + \frac{g_{ds2}}{G_L}} = \frac{g_{m2}}{1 + \frac{g_{ds2}}{G_L}} \qquad \text{(Equation 3)}$$

Substituting equation 1 in equation 3, we get,

$$y_{in\,2} = \frac{g_m}{1 + \frac{g_{ds}}{g^2{}_{ds}/g_m}} = g_{ds} \quad \text{(Equation 3)}$$

Therefore, the gain from the input to the source of Q_2 is given by,

$$\frac{v_{s2}}{v_{in}} = \frac{g_{m1}}{g_{ds1} + y_{in2}} = -\frac{g_m}{2g_{ds}}$$

Therefore, the overall gain is given by,

$$A_V = \frac{v_{s2}}{v_{in}}\frac{v_{out}}{v_{s2}} = -\frac{g_m}{2g_{ds}}\frac{g_{m2}}{G_L + g_{ds2}} = -\frac{g_m}{2g_{ds}}\frac{g_{m2}}{g_{ds2}} = -\frac{1}{2}\left(\frac{g_m}{g_{ds}}\right)^2$$

Problems:

1. Considering the current mirror shown, where I_{in} = 100 µA and each transistor has W/L = 100 µm/ 1.6 µm. Given that $\mu_n C_{ox}$ = 92 µA/ V^2, V_{tn} = 0.8V and r_{ds} = [8000L (µm)] / [I_D (mA)], find r_{out} for the current mirror and the value of g_{m1}. Also, estimate the change in I_{out} for 0.5V change in the output voltage.

Sol.

Given:

I_{in} = 100 µA

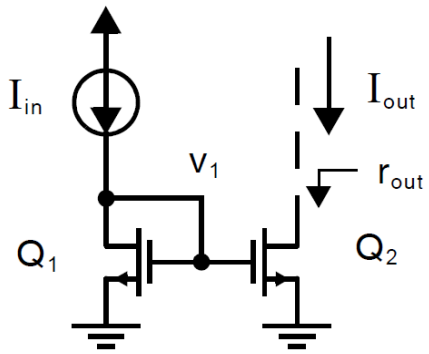
W/L = 100 µm/ 1.6 µm

$\mu_n C_{ox}$ = 92 µA/ V^2

V_{tn} = 0.8V

r_{ds} = [8000L (µm)] / [I_D (mA)]

ΔV = 0.5V



To find:

r_{out} = ?

g_{m1} = ?

ΔI_{out} = ?

Here, W/L ratios of Q_1 and Q_2 are same, the nominal value of I_{out} equals that of I_{in} = 100 µA.

Therefore, r_{out} is given as,

$$r_{out} = r_{ds\,2} = \frac{8000\ L\ (\mu m)}{I_D\ (mA)} = \frac{8000\ \times 1.6}{0.1} = 128\ k\Omega$$

The value of g_{m1} is given by,

$$g_{m1} = \sqrt{2\mu_n C_{ox}\ (W/L)\ I_{D1}} = \sqrt{2 \times 92 \left(\frac{100}{1.6}\right) \times 100} = 1.07\ mA/\ V$$

The change in the output current can be estimated as,

$$\Delta I_{out} = \frac{\Delta V}{r_{out}} = \frac{0.5}{128} = 3.9\ \mu A$$

2. Assuming all transistors have W/L = 100 µm/ 1.6 µm as shown with $\mu_n C_{ox}$ = 90 µA/ V^2, $\mu_p C_{ox}$ = 30 µA/ V^2, I_{bias} =100 µA, $r_{ds-\ n}$ = [8000L (µm)] / [I_D (mA)] and $r_{ds-\ p}$ = [12000L (µm)] / [I_D (mA)]. Find the gain of the stage?

Sol.

Given:

W/L = 100 µm/ 1.6 µm

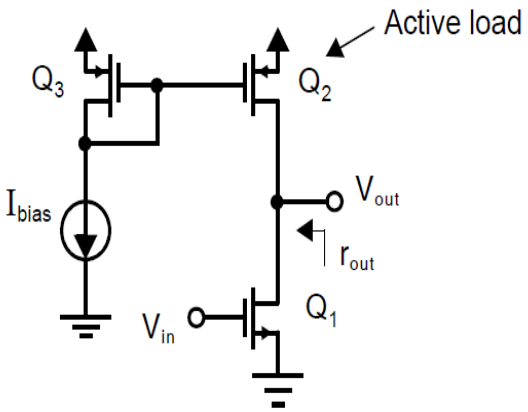
$\mu_n C_{ox}$ = 90 µA/ V^2

$\mu_p C_{ox}$ = 30 µA/ V^2

I_{bias} =100 µA

$r_{ds-\ n}$ = [8000L (µm)] / [I_D (mA)]

$r_{ds-\ p}$ = [12000L (µm)] / [I_D (mA)]



To find:

A_V = ?

WKT, the gain A_V is given as,

$$A_V = -g_m\,(r_{ds\,1} || r_{ds\,2})$$

Now finding,

$$g_{m1} = \sqrt{2\mu_n C_{ox}\,(W/L)\,I_{bias}} = \sqrt{2 \times 90 \left(\frac{100}{1.6}\right) \times 100} = 1.06\ \text{mA/ V}$$

$$r_{ds1} = \frac{8000\ L\ (\mu m)}{I_D\ (mA)} = \frac{8000 \times 1.6}{0.1} = 128\ k\Omega \text{ and } r_{ds2} = \frac{12000\ L\ (\mu m)}{I_D\ (mA)} = \frac{12000 \times 1.6}{0.1} = 192\ k\Omega$$

Now substituting the above found values in,

$$A_V = -g_m (r_{ds1} || r_{ds2})$$

We get,

$$A_V = -1.06(128 \,||\, 192) = -81.4$$

Therefore, the gain of the stage/ amplifier is – 81.4 respectively.

3. Consider a source follower as shown, where all transistors have W/L = 100 µm/ 1.6 µm with $\mu_n C_{ox}$ = 90 µA/ V^2, $\mu_p C_{ox}$ = 30 µA/ V^2, I_{bias} =100 µA, r_{ds-n} = [8000L (µm)] / [I_D (mA)] and $\gamma_n = 0.5\ V^{1/2}$. Find the gain of the stage?

Sol.

Given:

W/L = 100 µm/ 1.6 µm

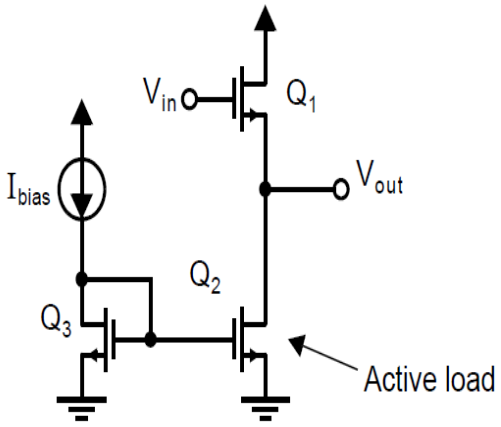
$\mu_n C_{ox}$ = 90 µA/ V^2

$\mu_p C_{ox}$ = 30 µA/ V^2

I_{bias} =100 µA

r_{ds-n} = [8000L (µm)] / [I_D (mA)]

$\gamma_n = 0.5\ V^{1/2}$



To find:

A_V = ?

WKT, the gain A_V of a source follower is given as,

$$A_V = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} = \frac{g_{m1}}{g_{m1} + g_{s1} + 1/r_{ds1} + 1/r_{ds2}}$$

Now finding,

$$g_{m1} = \sqrt{2\mu_n C_{ox}\,(W/L)\,I_{bias}} = \sqrt{2 \times 90\left(\frac{100}{1.6}\right) \times 100} = 1.06\ \text{mA/ V}$$

$$r_{ds1} = r_{ds2} = \frac{8000\ L\ (\mu m)}{I_D\ (mA)} = \frac{8000\ \times 1.6}{0.1} = 128\ k\Omega$$

$$g_{s1} = \frac{\gamma\, g_m}{2\sqrt{V_{SB} + |2\emptyset_F|}} = \frac{0.5\ g_m}{2\sqrt{2 + 0.7}} = 0.15\, g_m = 0.15 \times 1.06 = 0.16\ \text{mA/ V}$$

$$(\text{Here } V_{SB} = 2 \text{ and } \emptyset_F = 0.35 \rightarrow \text{Standard Values})$$

Therefore, the gain is given by,

$$A_V = \frac{1.06}{1.06 + 0.16 + {}^{1}/_{128} + {}^{1}/_{128}} = 0.86$$

Therefore, the gain of the source follower is 0.86 respectively.

4. Consider a source degenerated current mirror as shown, where I_{in} = 100 µA, each transistor W/L = 100 µm/ 1.6 µm, R_s = 5 kΩ, $\mu_n C_{ox}$ = 92 µA/ V^2, V_{tn} = 0.8V and r_{ds} = [8000L (µm)] / [I_D (mA)]. Find r_{out} for the current mirror. Assume the body effect can be approximated by $g_s = 0.2\ g_m$.

Sol.

Given:

W/L = 100 µm/ 1.6 µm

R_s = 5 kΩ

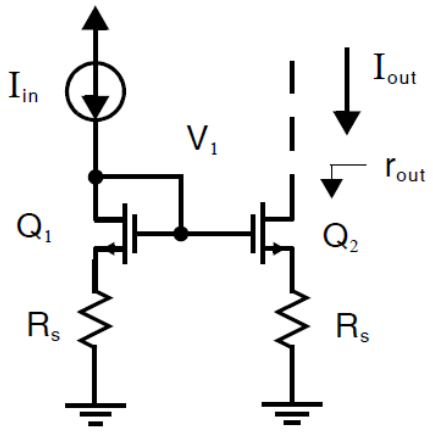
$\mu_n C_{ox}$ = 92 µA/ V^2

V_{tn} = 0.8V

r_{ds} = [8000L (µm)] / [I_D (mA)]

$g_s = 0.2\ g_m$

I_{in} = 100 µA



To find:

r_{out} = ?

WKT,

$$r_{out} = r_{ds2}[1 + R_s(g_{m2} + g_{s2})]$$

$$I_{out} = I_{in}$$

Now finding,

$$g_{m2} = \sqrt{2\mu_n C_{ox}\,(W/L)\,I_{out}} = \sqrt{2 \times 92\left(\frac{100}{1.6}\right) \times 100} = 1.07\ \text{mA/ V}$$

$$r_{ds2} = \frac{8000\ L\ (\mu m)}{I_D\ (mA)} = \frac{8000\ \times 1.6}{0.1} = 128\ k\Omega$$

Therefore, the r_{out} is given by,

$$r_{out} = 128[1 + 5(1.07 + 0.2 \times g_m)]$$

$$r_{out} = 128[1 + 5(1.07 + 0.2 \times 1.07)] = 950\ k\Omega$$

Therefore, the output resistance r_{out} of the source denegation current mirror is 950 kΩ respectively.

5. Consider a cascode current mirror as shown, where I_{in} = 100 µA, each transistor W/L = 100 µm/ 1.6 µm, $\mu_n C_{ox}$ = 92 µA/ V^2, V_{tn} = 0.8V and r_{ds}= [8000L (µm)] / [I_D (mA)]. Find r_{out} for the current mirror. Assume the body effect can be approximated by g_s = 0.2 g_m. Also find the minimum output voltage at V_{out} such that the output transistors remain in the active region.

Sol.

Given:

W/L = 100 µm/ 1.6 µm

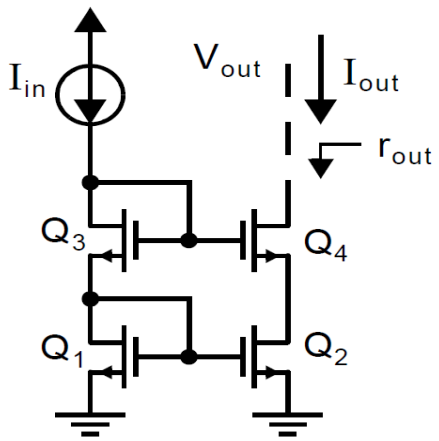
$\mu_n C_{ox}$ = 92 µA/ V^2

V_{tn} = 0.8V

r_{ds} = [8000L (µm)] / [I_D (mA)]

g_s = 0.2 g_m

I_{in} = 100 µA



To find:

r_{out} = ?

V_{out} = ?

WKT,

$$r_{out} = r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4})]$$

$$I_{out} = I_{in}$$

Now finding,

$$g_{m4} = \sqrt{2\mu_n C_{ox} (W/L) I_{out}} = \sqrt{2 \times 92 \left(\frac{100}{1.6}\right) \times 100} = 1.07 \text{ mA/ V}$$

$$r_{ds2} = r_{ds4} = \frac{8000 \text{ L } (\mu m)}{I_D \text{ (mA)}} = \frac{8000 \times 1.6}{0.1} = 128 \text{ k}\Omega$$

Therefore, the r_{out} is given by,

$$r_{out} = 128[1 + 128(1.07 + 0.2 \times 1.07)] = 21 \text{ M}\Omega$$

The maximum output voltage is determined by,

$$V_{out} = 2 \times V_{eff} + V_{tn}$$

Now finding,

$$V_{eff} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} \left(\frac{W}{L}\right)}} = \sqrt{\frac{2 \times 100}{92 \times \left(\frac{100}{1.6}\right)}} = 0.19V$$

Therefore,

$$V_{out} = 2 \times 0.19 + 0.8 = 1.18V$$

Therefore, the output resistance r_{out} of the cascode current mirror is 21 MΩ and the maximum output voltage is 1.18V respectively.

Assignment:

1. What is transistor sizing?
2. Assuming g_m is on the order of 0.5 mA/ V and r_{ds} is on the order of 100 kΩ, then what is the gain of the cascode amplifier?