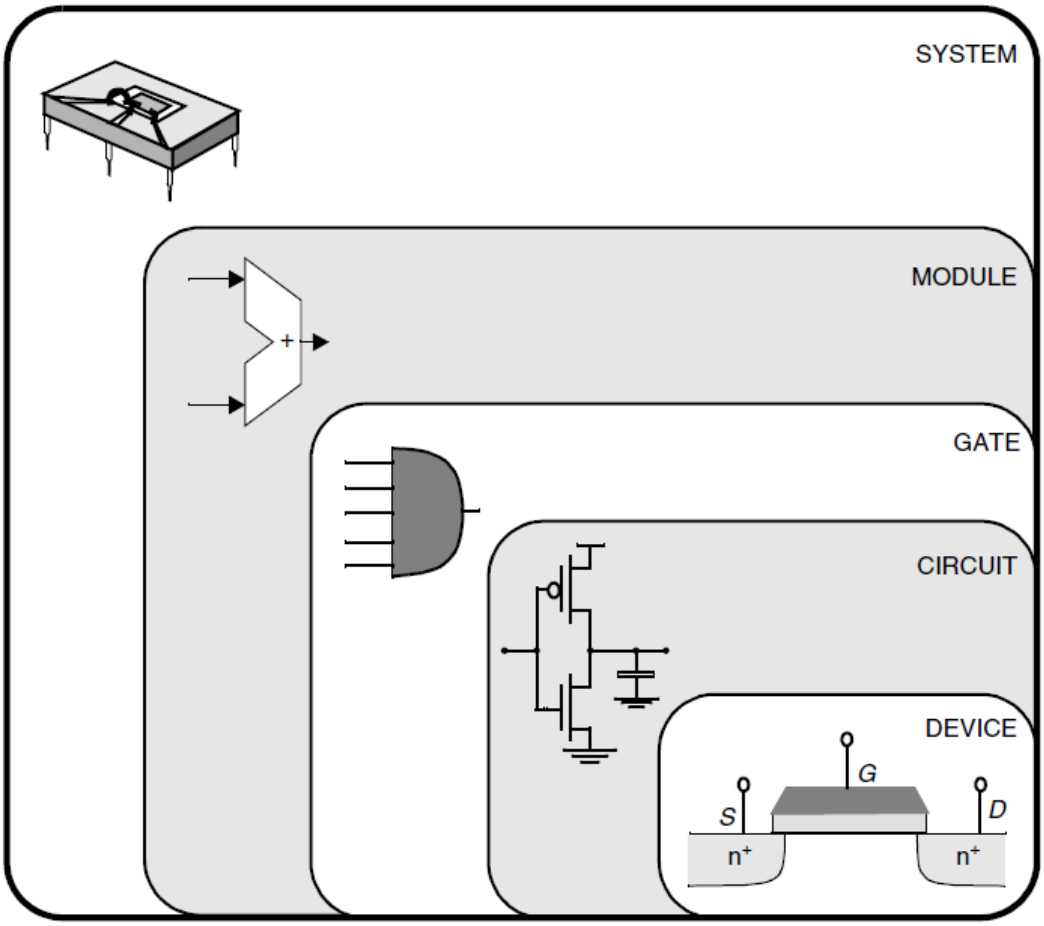
Very Large Scale Integrated Technology and Design (VLSI or VLSI Technology and VLSI Design):

VLSI is a process of creating an integrated circuit by using thousands of transistors on a single chip and it's designing of the circuit using computer aid via HDL is called as VLSI design.

- With the advent of VLSI, designers could design single chips with more than 100, 000 transistors and since the circuits were very large, it was practically difficult to verify them using breadboard, so computer aided logic simulators were used to very these circuits before they were fabricated on chip.
- The designers built small building blocks of the gate- level digital circuits and then derive higher level blocks from them, this process was continued until they built the top- level block, these was then verified with the help of logic simulators.
- It became very easy to iron out bugs in the chip architecture.
- The use of HDLs like Verilog HDL and VHDL and their simulators made the VLSI design very simple and modern development.

Design Abstraction Levels in Digital Circuits:

Typically used abstraction levels in digital circuit design are, in order of increasing abstraction, the device, circuit, gate, functional module (e.g. adder) and system levels (e.g. processor), as illustrated.



DESIGN ASBTRACTION LEVELS IN DIGITAL CIRCUITS

MOS Technology- Metal- oxide- semiconductor Technology:

MOS technology is a promising technology for IC design and implementation as integration circuit design and implementation requires minimum power dissipation, smaller chip area, lower time delay, low production cost, highest stability, testability and higher reliability.

The MOS technology is based on pMOS, nMOS and CMOS (combination of pmos and nmos) and BiCMOS devices/ transistors with each having its own properties which make them important. As pMOS is easy to manufacture, nMOS can operate faster and CMOS offers very high regularity and lower power dissipation than other MOS devices.

- Mostly nMOS, CMOS and BiCMOS are used and preferred.

Preference of nMOS:

1. nMOS design methodology and design rules are easily learned and provide an excellent introduction to structured design for VLSI.
2. nMOS technology provide an excellent background for other technologies. Particularity, familiarity with nmos allows relatively easy transition to CMOS design.
3. Both CMOS and nMOS technologies are likely to be current for some time, as there are areas of application where one or other is more suitable. Both are well suited for VLSI system requirements.

Comparison between CMOS and Bipolar:

CMOS Technology/ CMOS Devices	Bipolar or BiCMOS Technology/ Bipolar Devices
It has low- state power dissipation.	It has high power dissipation.
It has high input impedance, packing density and noise margin.	It has low input impedance, packing density and noise margin.
Threshold voltage of CMOS devices is highly scalable on comparison to bipolar devices.	Threshold voltage of bipolar devices is low scalable on comparison to bipolar devices.
High delay sensitivity to load.	Low delay sensitivity to load.
These devices have unidirectional capability.	These devices have bidirectional capability.
Low transconductance and output drive current.	High transconductance and output drive current.
Low gain	High gain

Moore's Law:

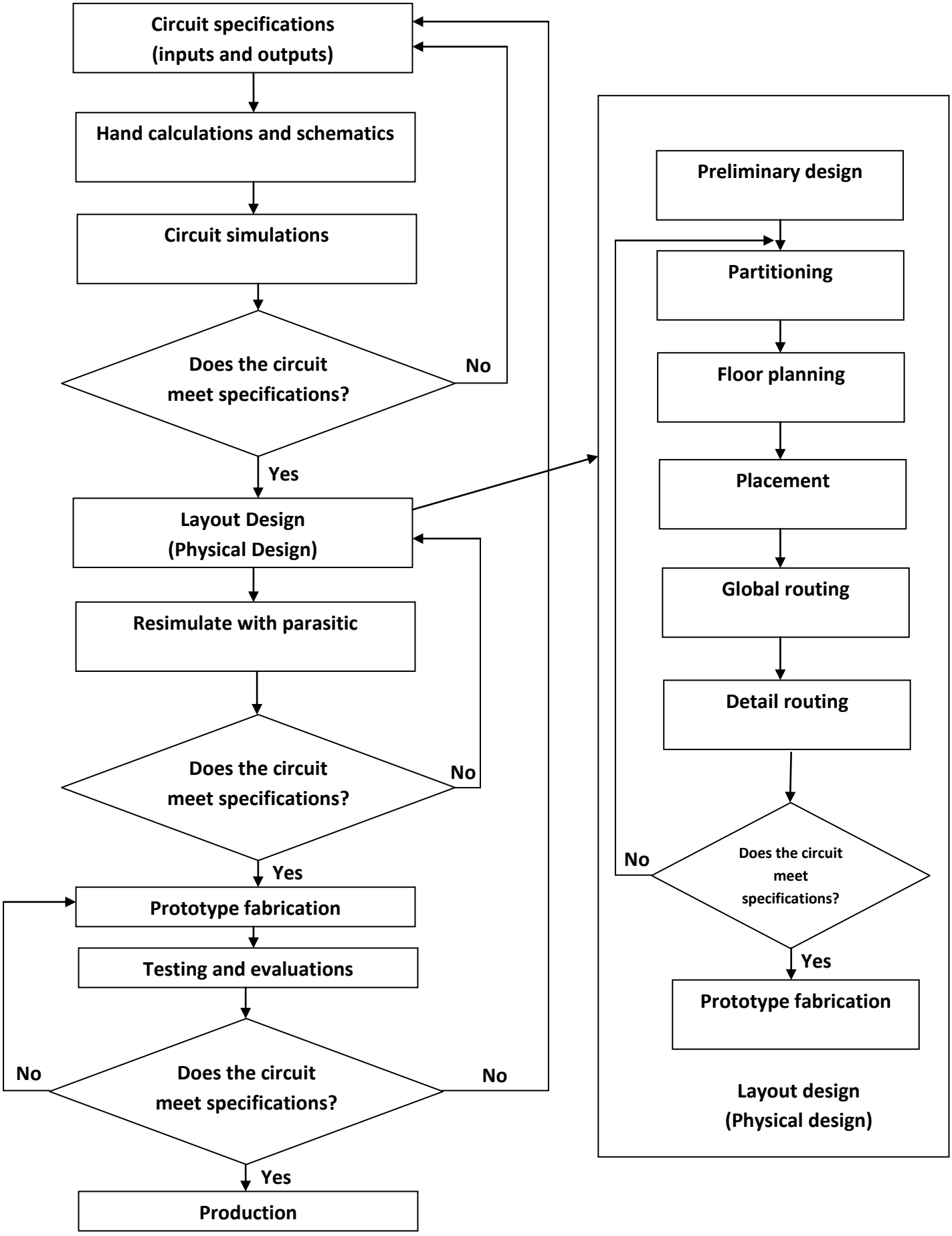
(The observation made in 1965 by Gordon Moore, co-founder of Intel)

Moore's law states that the number of transistors per square inch on a dense integrated circuit doubles approximately every two years.

Basic IC design flow Chart/ CMOS IC Design Process:

The CMOS circuit design consists of selection of circuit specifications including inputs, outputs, hand calculation, circuit simulations, and layout design of the circuits including parasitic evaluation, fabrication and testing.

Flow Chart for MOS/ CMOS IC Design Process



The circuit specifications are set as per the requirements of the applications/ projects. This can be a result of trade- off between cost and performances and changes in customer needs. The circuit design process in the flow chart is followed in custom IC designed chip which is also called as **Application Specific Integrated Circuits (ASIC)**. The custom chip design method is mainly used for development of mass produced chips such as microprocessors, central processing unit (CPU), memory, etc.

- As the layer design consists of area minimization, wire- length minimizations, and routing, so the layout design includes partitioning, floor planning and placement for area minimization, wire length and routing for delay minimization of signals.

Basic MOS Transistor:

nMOS Transistor:

nMOS transistors are fabricated using p- substrate and the source and drain are formed by diffusing n- type impurities into the regions, and the n- type regions are extended mainly in lightly doped p- substrate. Two p- n junctions are formed by the source, gate and drain.

The establishment of current between source and drain and its control are made in two ways:

1. Enhancement mode or Enhancement mode nMOS transistor
2. Depletion mode or Depletion mode nMOS transistor

Enhancement mode:

In enhancement mode, the current is established between source and drain after the formation of channel. When the gate- to- source voltage $V_{gs} = V_{ds} = 0$, no channel is established and the device is in non conducting state. When the gate is connected to the positive voltage with respect to source ($V_{gs} > 0$), the negative charges are induced to substrate and these induced charges make the charge inversion region in the substrate between source and drain, as a result a conducting channel is formed in between source and drain. To make an inversion layer for a channel formation (between source and drain), a minimum voltage is required between the gate and source and the voltage is called a **threshold voltage (V_{th})**.

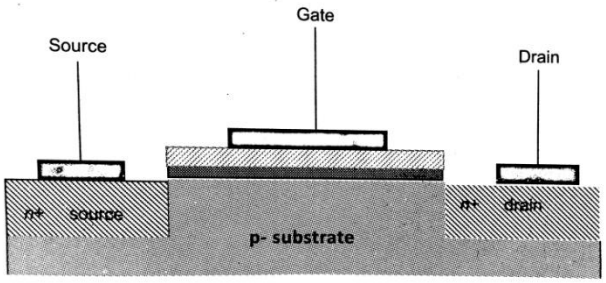
When V_{ds} is applied between the source and drain in the nMOS having channel, the effective gate voltage $V_g = V_{gs} - V_{th}$ and no current flows if $V_{gs} < V_{th}$. When $V_{ds} = V_{gs} = V_{th}$ then the device is **nonsaturated**.

When V_{ds} increases to be greater than $V_{gs} - V_{th}$, there is an insufficient electric field available to give creation of channel. The channel is therefore, punched off. In this condition the diffusion current completes the path between source and drain and behaves as a constant- current source having a constant resistance. This condition is known as **saturation condition**.

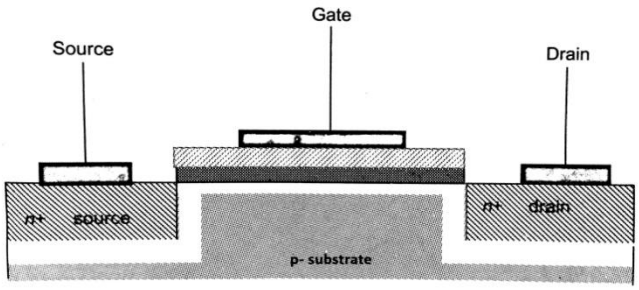
Depletion Mode:

In depletion mode of an nMOS transistor, the channel is established because of the implant even when $V_{gs} = 0$ and for the channel to cease to exist, a negative voltage V_{thd} must be applied between the gate and source.

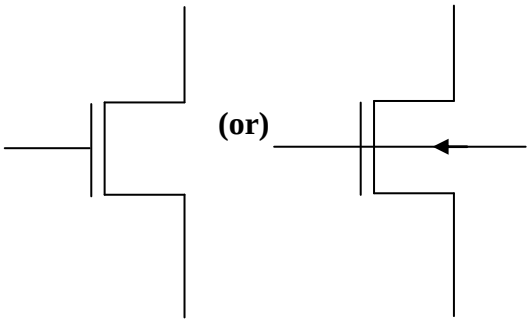
- Typically $V_{thd} < -0.8\ V_{DD}$, depending on the implant and substrate bias.



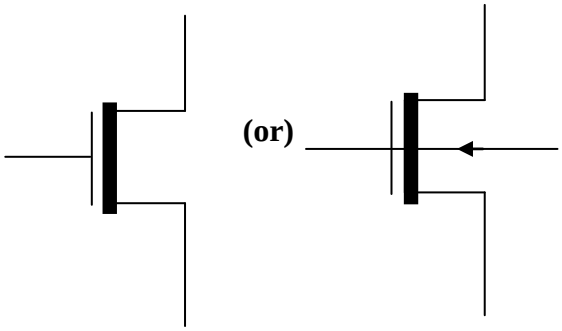
nMOS Enhancement Mode



nMOS Depletion Mode



Circuit Symbol of nMOS (Enhancement Mode)



Circuit Symbol of nMOS (Depletion Mode)

nMOS Fabrication:

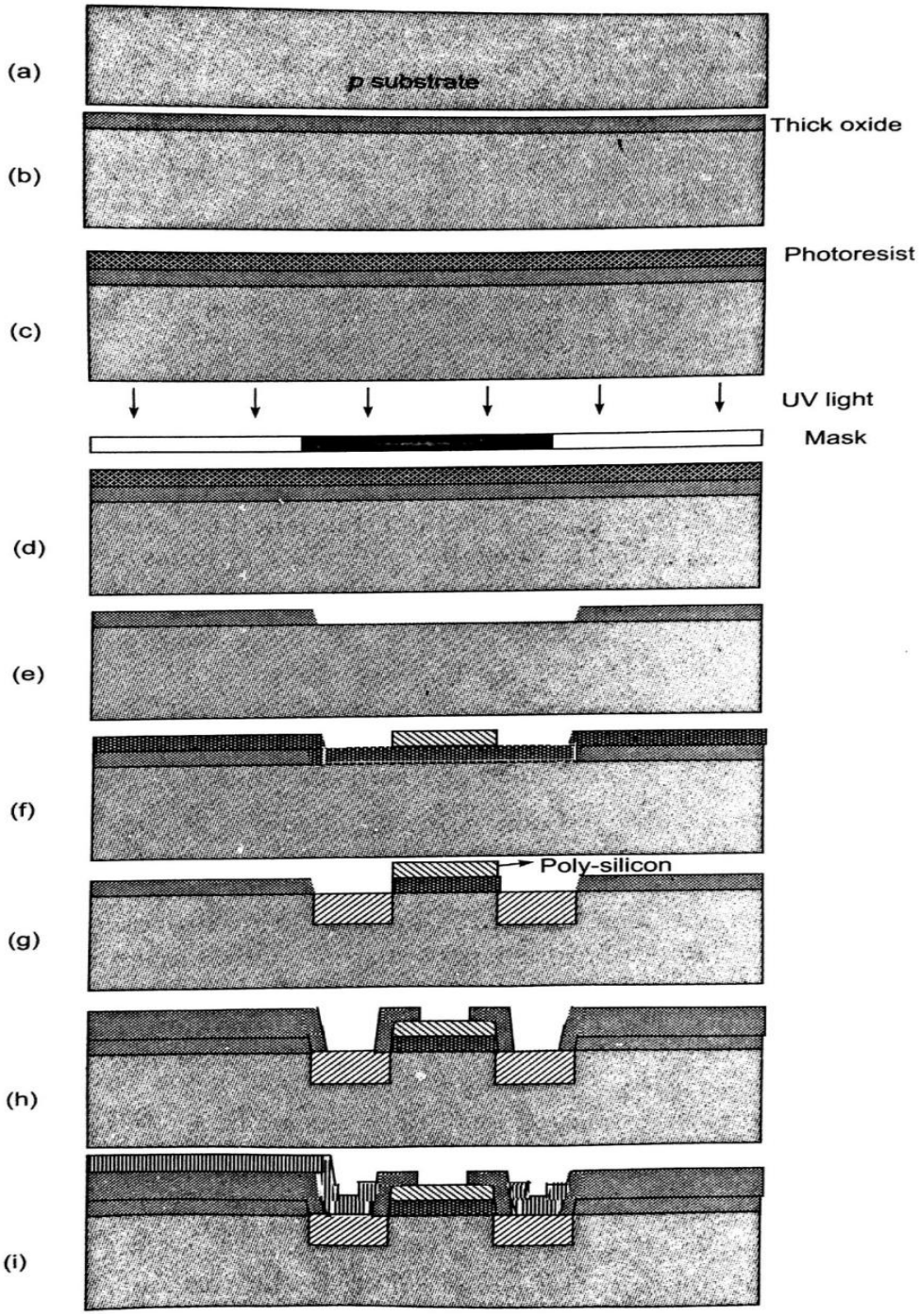
a. Processing is carried out on a thin silicon wafer/ substrate cut from a single crystal doped with p- type impurities of concentration 10^{15}/ cm^3 to 10^{16}/ cm^3.
b. A layer of silicon dioxide SiO_2 (typically 1μm thick) is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.
c. The surface is now is covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.
d. The photoresist layer is then exposed to ultraviolet (UV) light through a mask which defines those regions into which diffusion is to take place together with transistor channels.
e. These areas are subsequently readily etched away together with the underlying SiO_2 so that the wafer surface is exposed in those areas defined by the mask.
f. The remaining photoresist is removed and a thin layer of SiO_2 is grown over the entire chip surface and then polysilicon is deposited on the top of this to form the gate structure. The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapour deposition (CVD). In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary.
g. Further photoresist coating and masking allows the polysilicon to be patterned and then the thin oxide is removed to expose areas into which n- type impurities are to be diffused to form the source and drain. Diffusion is achieved by heating the wafer to a high temperature and passing a gas

containing the desired n- type impurity (say phosphorus) over the surface. It is now noted that the polysilicon and underlying SiO_2 acts as a mask during diffusion, the process is self aligning.

h. The whole chip then has metal (aluminium) deposited over its surface to a thickness typically in excess of 1μm. This metal layer is then masked and etched to form the required interconnection pattern.

i. It is now clearly seen that the process revolves around the formation or deposition and pattering of three layers, separated by s SiO_2 insulation. The layers are diffusion within the substrate, polysilicon on oxide on the substrate, and metal insulated again by oxide.

For formation depletion mode devices it is only necessary to introduce a masked ion implantation step between steps *e* and *f* or steps *f* and *g* respectively.



pMOS Transistor:

pMOS transistors are fabricated using n- substrate and the source and drain are formed by diffusing p- type impurities into the regions, and the p- type regions are extended mainly in lightly doped n- substrate. Two p- n junctions are formed by the source, gate and drain.

The establishment of current between source and drain and its control are made in two ways:

1. Enhancement mode or Enhancement mode pMOS transistor
2. Depletion mode or Depletion mode pMOS transistor

Enhancement mode:

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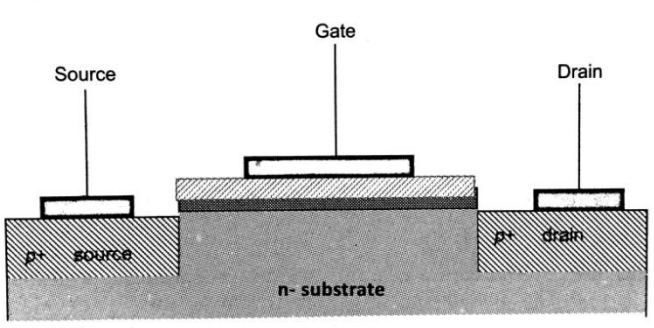
When V_{ds} is applied between the source and drain in the pMOS having channel, the effective gate voltage $V_g = V_{gs} - V_{th}$ and no current flows if $V_{gs} < V_{th}$. When $V_{ds} = V_{gs} = V_{th}$ then the device is **nonsaturated**.

When V_{ds} increases to be greater than $V_{gs} - V_{th}$, there is an insufficient electric field available to give creation of channel. The channel is therefore, punched off. In this condition the diffusion current completes the path between source and drain and behaves as a constant- current source having a constant resistance. This condition is known as **saturation condition**.

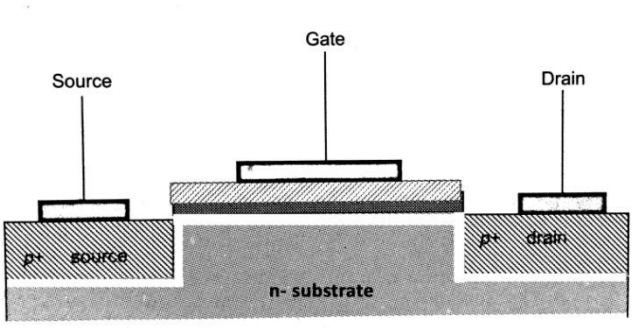
Depletion Mode:

In depletion mode of an nMOS transistor, the channel is established because of the implant even when $V_{gs} = 0$ and for the channel to cease to exist, a negative voltage V_{thd} must be applied between the gate and source.

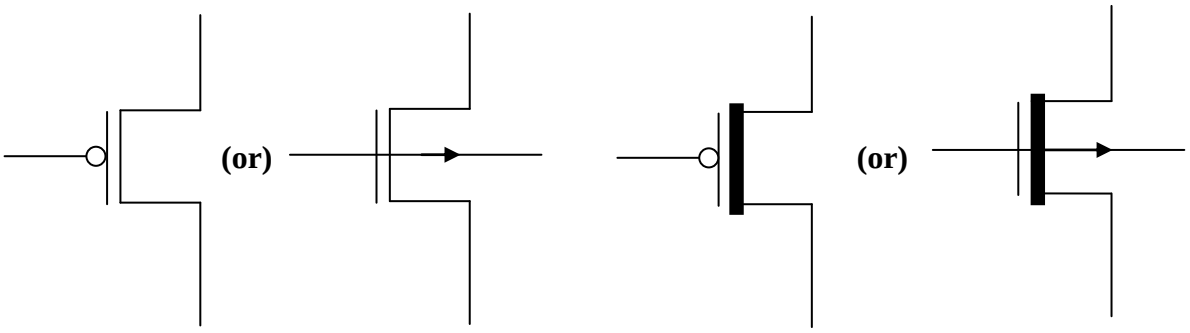
- Typically $V_{thd} < -0.8\ V_{DD}$, depending on the implant and substrate bias.



pMOS Enhancement Mode



pMOS Depletion Mode



Circuit Symbol of pMOS (Enhancement Mode) **Circuit Symbol of pMOS (Depletion Mode)**

pMOS Fabrication:

(Same as nMOS with n- substrate and p- diffusion)

a. Processing is carried out on a thin silicon wafer/ substrate cut from a single crystal doped with n- type impurities of concentration 10^{15}/ cm^3 to 10^{16}/ cm^3.
b. A layer of silicon dioxide SiO_2 (typically 1μm thick) is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.
c. The surface is now is covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.
d. The photoresist layer is then exposed to ultraviolet (UV) light through a mask which defines those regions into which diffusion is to take place together with transistor channels.
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f. The remaining photoresist is removed and a thin layer of SiO_2 is grown over the entire chip surface and then polysilicon is deposited on the top of this to form the gate structure. The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapour deposition (CVD). In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary.
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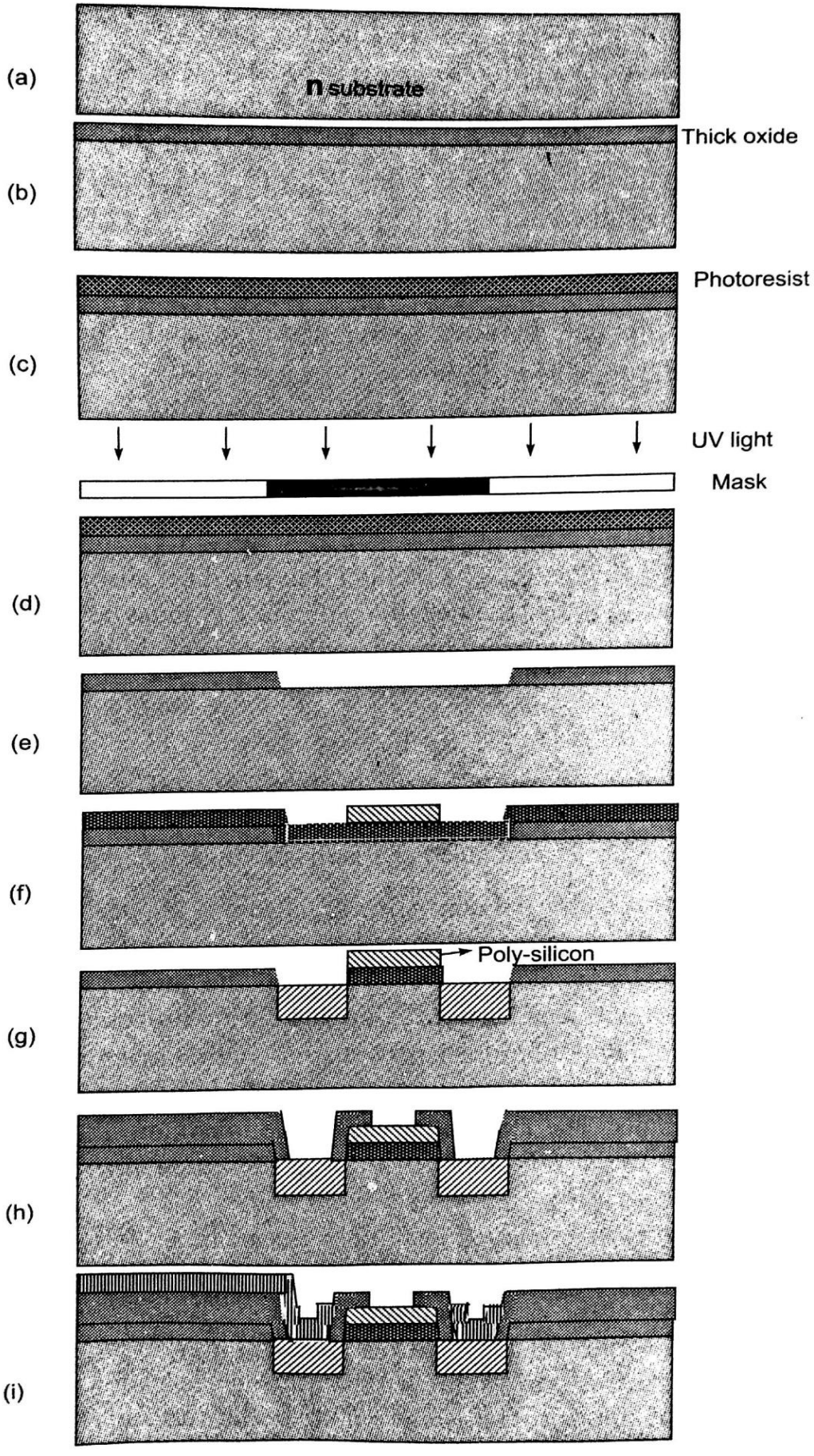

(a)
n substrate
(b)
Thick oxide
(c)
Photoresist
UV light
Mask
(d)
(e)
(f)
Poly-silicon
(g)
(h)
(i)

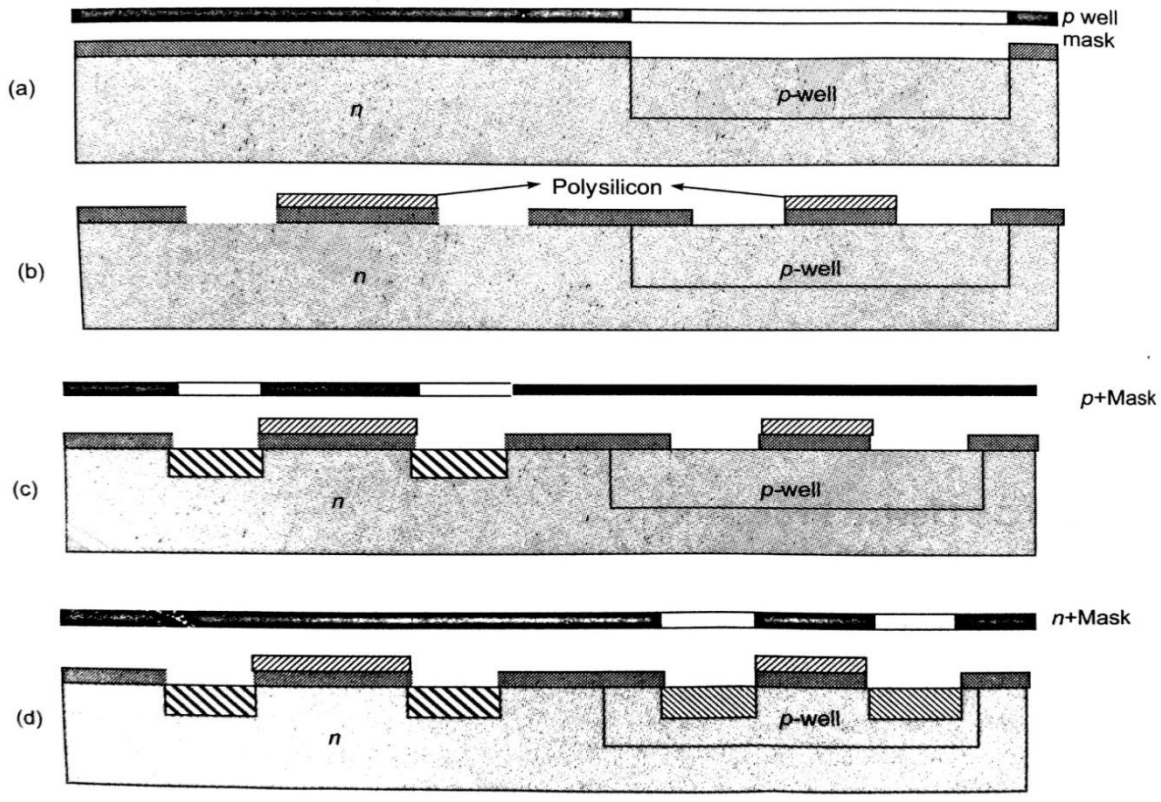
CMOS Transistor:

CMOS transistor/ device is a combination of pMOS and nMOS. There are two types of device processing in CMOS:

1. p- well CMOS
2. n- well CMOS

p- well CMOS device Fabrication:

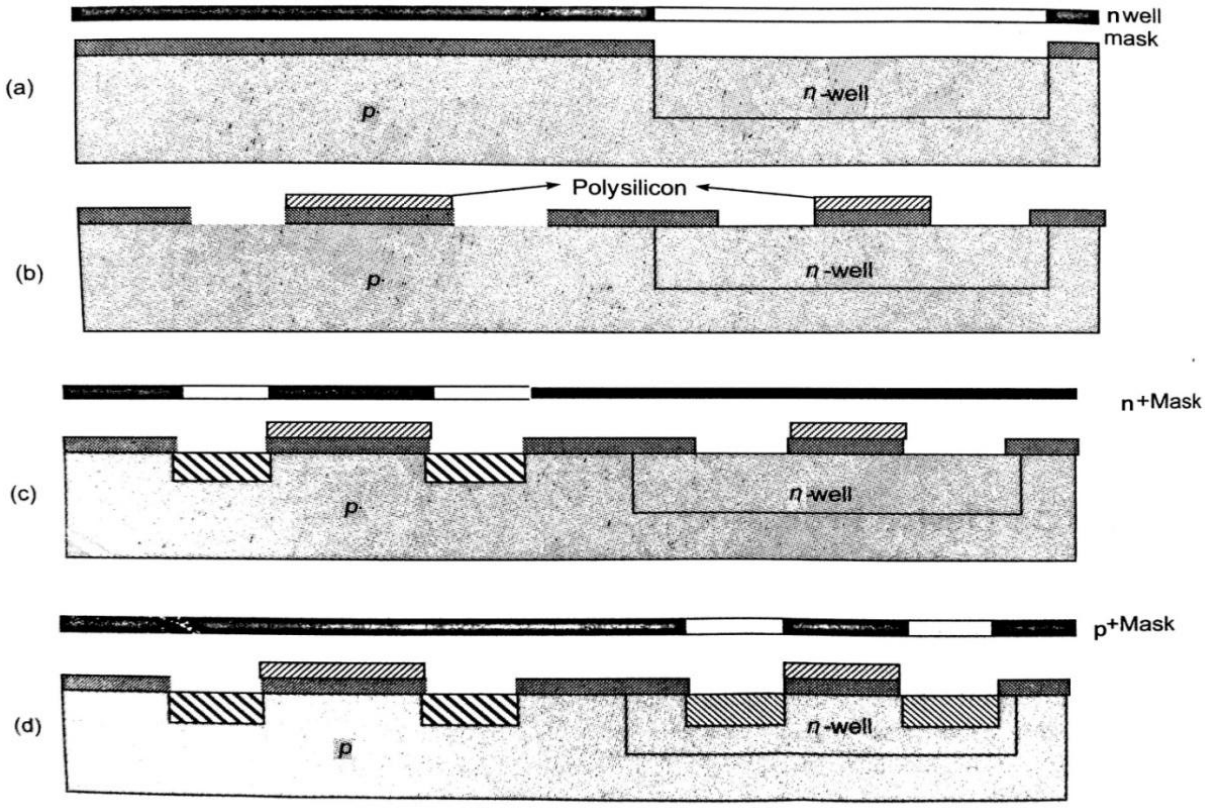
a. The p- well region is made by using mask 1 and diffusion of deep p- well impurity into the n- type substrate.
b. nMOS and pMOS active regions are formed by using mask 2.
c. Gate oxidation (thinox) region is defined.
d. Formation and patterning of polysilicon layer are made by using mask 3.
e. Mask 4 having p- type diffusion layer is used to define all areas of p- type diffusion and the p- type diffusion is made on these regions.
f. Mask 5 having n diffusion layer is used to define all areas of n diffusion and n diffusion is made on these layers.
g. Contact cut areas are defined by using mask 6 and contacts are made.
h. The metal layers are formed by using mask 7.
i. Overall glass with cuts for bonding pads are made by using mask 8.



CMOS FABRICATION PROCESS (p- well) (a) formation of p- well (b) polysilicon layer for Gate formation (c) p- type diffusion (d) n- type diffusion

n- well CMOS device Fabrication:

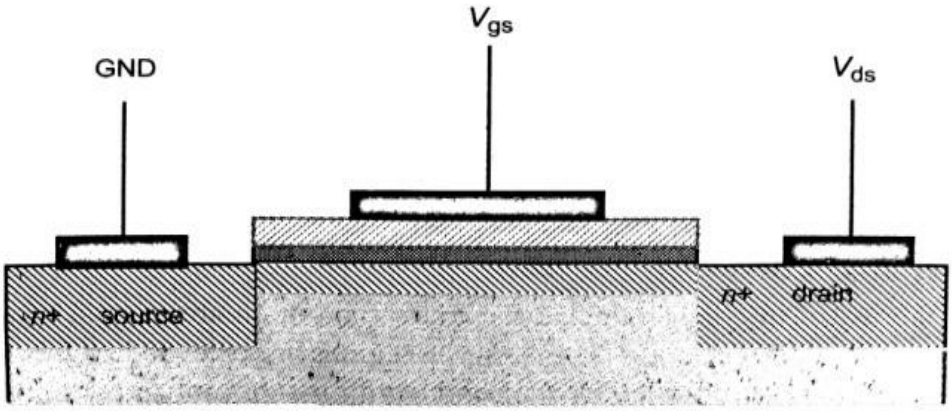
a. The n- well region is made by using mask 1 and diffusion of deep n- well impurity into the p- type substrate.
b. nMOS and pMOS active regions are formed by using mask 2.
c. Gate oxidation (thinox) region is defined.
d. Formation and patterning of polysilicon layer are made by using mask 3.
e. Mask 4 having n- type diffusion layer is used to define all areas of n- type diffusion and the n- type diffusion is made on these regions.
f. Mask 5 having p diffusion layer is used to define all areas of p diffusion and p diffusion is made on these layers.
g. Contact cut areas are defined by using mask 6 and contacts are made.
h. The metal layers are formed by using mask 7.
i. Overall glass with cuts for bonding pads are made by using mask 8.



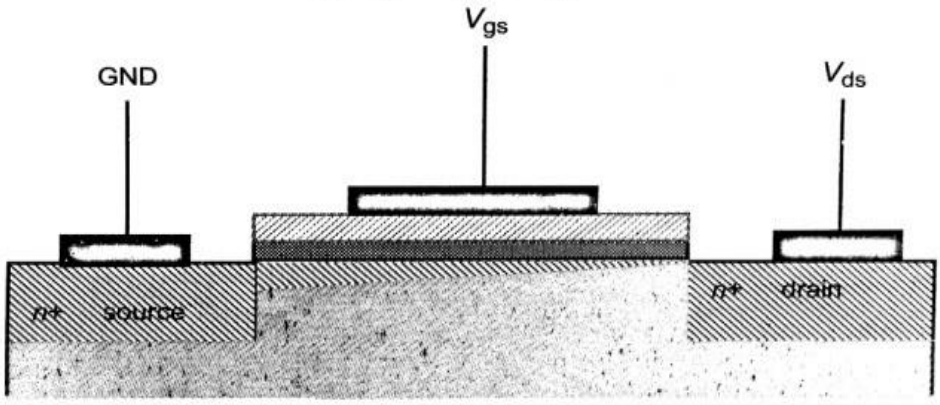
CMOS FABRICATION PROCESS (n- well) (a) formation of n- well (b) polysilicon layer for Gate formation (c) n- type diffusion (d) p- type diffusion

Drawbacks/ Deficiencies of MOS:

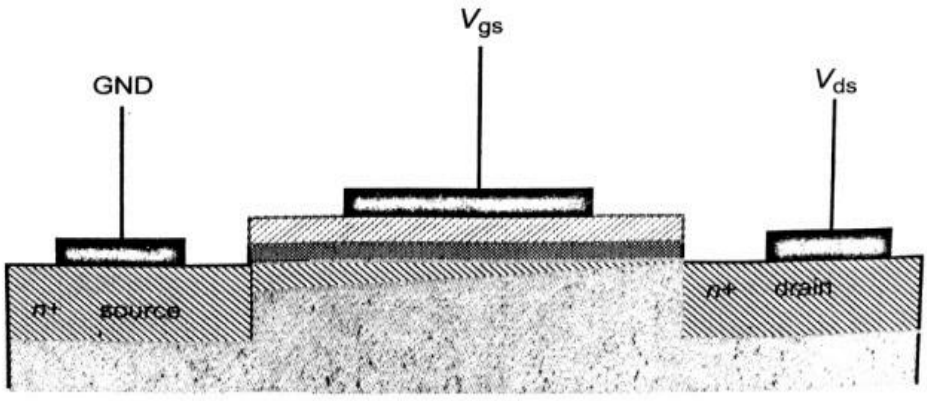
1. MOS devices have limited load- driving capabilities which is because of limited current- sourcing and current- sinking abilities associated with p and n transistors.
2. Bipolar transistors also provide higher gain, better noise and high- frequency characteristics than MOS circuits.



(a) $V_{gs} > V_{th}$ and $V_{ds} = 0$ V



(b) $V_{gs} > V_{th}$ and $V_{ds} = V_{gs} - V_{th}$



(c) $V_{gs} > V_{th}$ and $V_{ds} > (V_{gs} - V_{th})$

Enhancement MOS for different V_{ds} and V_{gs} (considering nMOS)

BiCMOS Transistor:

The combination of CMOS with bipolar transisitor is a BiCMOS device. BiCMOS is an effective way of speeding up of VLSI circuits.

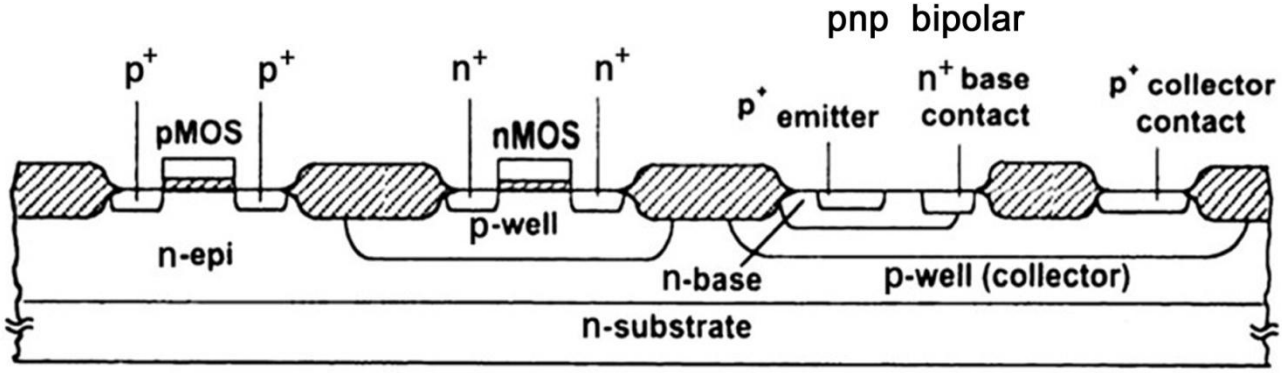
- Usage of BiCMOS technology improves the speed of ALU, ROM and barrel switch etc.
- The fabrication of BiCMOS is similar to CMOS along with additional steps for the fabrication of Bipolar transistor.

There are two types of BiCMOS devices:

1. n- well BiCMOS
2. p- well BiCMOS

p- well BiCMOS Fabrication:

1. The p- well region is made by using mask 1 and diffusion of deep p- well impurity into the n- type substrate.
2. nMOS and pMOS active regions are formed by using mask 2.
3. Gate oxidation (thinox) region is defined.
4. Formation and patterning of polysilicon layer are made by using mask 3.
5. Mask 4 having p- type diffusion layer is used to define all areas of p- type diffusion and the p- type diffusion is made on these regions.
6. Mask 5 having n diffusion layer is used to define all areas of n diffusion and n diffusion is made on these layers.
7. Contact cut areas are defined by using mask 6 and contacts are made.
8. The metal layers are formed by using mask 7.
9. Overall glass with cuts for bonding pads are made by using mask 8.

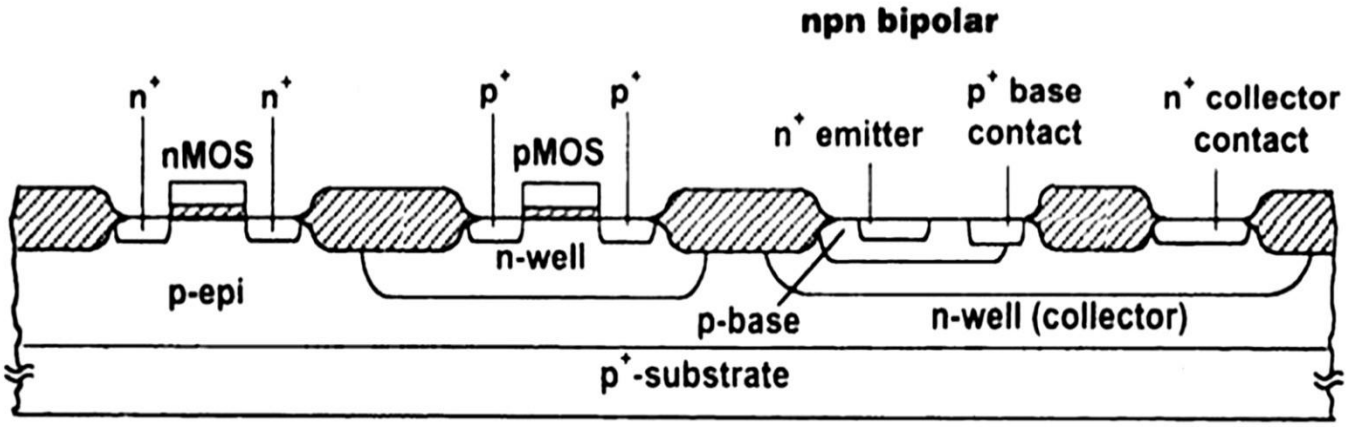


p- well BiCMOS with pnp Bipolar transistor

n- well BiCMOS Fabrication:

1. The n- well region is made by using mask 1 and diffusion of deep n- well impurity into the p- type substrate.
2. nMOS and pMOS active regions are formed by using mask 2.
3. Gate oxidation (thinox) region is defined.
4. Formation and patterning of polysilicon layer are made by using mask 3.
5. Mask 4 having n- type diffusion layer is used to define all areas of n- type diffusion and the n- type diffusion is made on these regions.
6. Mask 5 having p diffusion layer is used to define all areas of p diffusion and p diffusion is made on these layers.
7. Contact cut areas are defined by using mask 6 and contacts are made.

8. The metal layers are formed by using mask 7.
9. Overall glass with cuts for bonding pads are made by using mask 8.



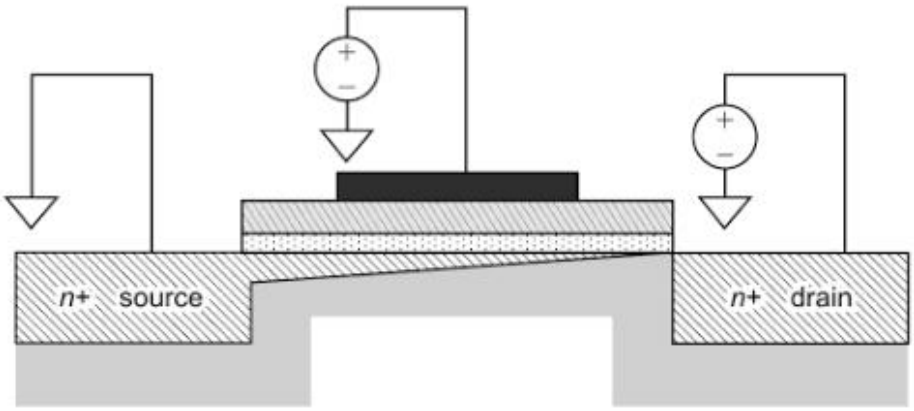
n- well BiCMOS with npn Bipolar transistor

Basic Electrical Properties of MOS:

The MOS has certain basic electrical properties such as:

1. **Drain to source current I_{ds} versus drain to source voltage V_{ds} relationship:**
   The concept of MOS evolves from the use of a voltage on the gate to induce a charge in the channel between source and drain, which may then be caused to move from source to drain under the influence of an electric field created by voltage V_{ds} applied between drain and source. Since the charge induced is dependent on the gate to source voltage V_{gs}, then I_{ds} is dependent on both V_{gs} and V_{ds}.

$$I_{ds} = -I_{ds} = \frac{Charge\ induced\ in\ channel\ (Q_c)}{Electron\ transit\ time\ (\tau)} \quad (Equation\ 1)$$



nMOS Transistor

First transit time:

$$\tau_{sd} = \frac{Length\ of\ Channel\ (L)}{Velocity\ (v)}$$

WKT,

$$Velocity\ v = \mu E_{ds}$$

Where:
$\mu\ is\ the\ electron\ or\ hole\ mobility\ (surface)$
$E_{ds}\ is\ the\ dielectric\ field (drain\ to\ source)$

Now,

$$E_{ds} = \frac{V_{ds}}{L}$$

Therefore,

$$v = \frac{\mu V_{ds}}{L}$$

Thus

$$\tau_{sd} = \frac{L^2}{\mu V_{ds}} \quad (Equation\ 2)$$

The typical values of μ at room temperature are:
$\mu_n = 650 cm^2/Vsec\ \ and \mu_p = 240\ cm^2/Vsec$

Now, studying the I_{ds} in saturation and non- saturation region:

- **Saturated Region ($\boldsymbol{V_{ds} \geq V_{gs} - V_{th}}$):**

The saturation commences when $V_{ds} = V_{gs} - V_{th}$. Since at this point the IR drop in the channel equals the effective gate to channel voltage at the drain and we may assume that the current remains fairly constant as V_{ds} increases further.

Thus,

$$I_{ds} = K\frac{W}{L}\frac{\left(V_{gs} - V_{th}\right)^2}{2}$$

Or

$$\boldsymbol{I_{ds} = \frac{C_g \mu}{2L^2}\left(V_{gs} - V_{th}\right)^2}$$

This expressions holds for both enhancement and depletion mode.

- **Non Saturated Region ($V_{ds} < V_{gs} - V_{th}$):**

Here the charge induced in channel due to gate voltage is due to the voltage difference between the gate and the channel V_{gs}.

The effective voltage is given as,

$$V_g = V_{gs} - V_{th}$$

where V_{th} is the threshold voltage needed to invert the charge under the gate and establish the channel

The induced charge is,

$$Q_c = E_g \epsilon_{ins}\ \epsilon_0 WL$$

Where:

E_g *is the average electric field, gate to channel*

ϵ_{ins} *is the relative permittivity of insulation between gate and channel*

ϵ_0 *is the permittivity of free space* $= 8.85 \times 10^{-14}\ F/cm$

Now,

$$E_g = \frac{\left((V_{gs} - V_{th}) - \frac{V_{ds}}{2}\right)}{D}$$

Where:

D is the oxide thickness

Thus,

$$Q_c = \frac{\left((V_{gs} - V_{th}) - \frac{V_{ds}}{2}\right)}{D} \epsilon_{ins}\ \epsilon_0 WL \quad (Equation\ 3)$$

Combining equations 3 and 2 with equation 1, we get

$$I_{ds} = \frac{\mu\ \epsilon_{ins}\ \epsilon_0 W \left((V_{gs} - V_{th}) - V_{ds}\right)\ V_{ds}}{2\ L\ D}$$

Or

$$\boldsymbol{I_{ds} = K\frac{W}{L}\left((V_{gs} - V_{th})V_{ds} - \frac{{V_{ds}}^2}{2}\right)}$$

Where:

$$K = \frac{\mu\, \epsilon_{ins}\, \epsilon_0}{D}$$

Here, the gate/ channel capacitance is,

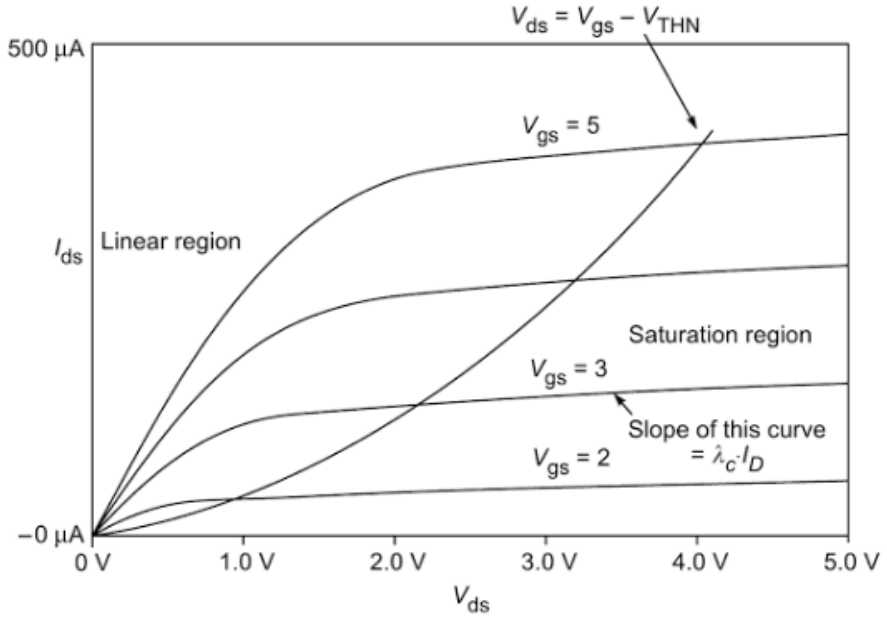
$$C_g = \frac{\epsilon_{ins}\, \epsilon_0 WL}{D} (Parallel\ Plate)$$

Therefore,

$$K = \frac{C_g\, \mu}{WL}$$

Therefore,

$$\boldsymbol{I_{ds} = \frac{C_g\, \mu}{L^2}\left((V_{gs} - V_{th}) V_{ds} - \frac{{V_{ds}}^2}{2} \right)}$$



I_{ds} Vs V_{ds} Characteristics of MOS (Considering nMOS)

2. Transistor Transconductance g_m:

Transconductance expresses the relationship between output current I_{ds} and the input voltage V_{gs} i.e.

$$g_m = \left. \frac{\delta\, I_{ds}}{\delta\, V_{gs}} \right|_{V_{ds} = constant}$$

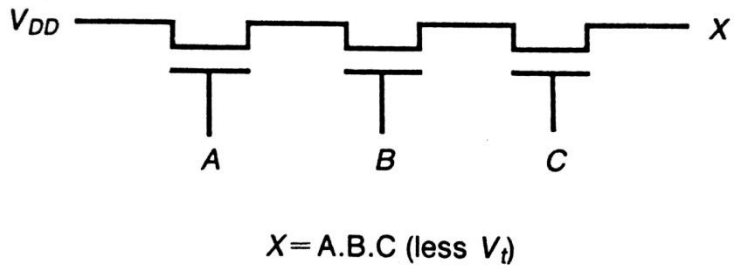
The transconductance in terms of circuit and parameters is given as,

$$g_m = \frac{\mu\, \varepsilon_{ins}\, \varepsilon_0}{D} \frac{W}{L} (V_{gs} - V_{th})$$

3. The pass transistor/ pass transistor:

Here the isolated nature of gate allows MOS transistors to be used as switches in series with lines carrying logic levels in a similar way to the use of relay contacts. This application of MOS transistors is called pass transistor.

- Using this application switching logic arrays can be formed such as AND array.

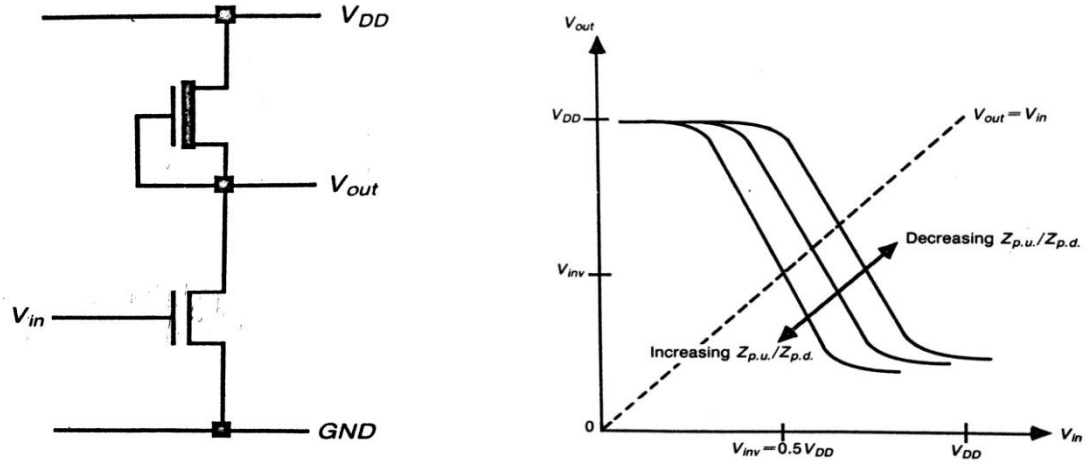


Pass transistor AND Gate

4. The nMOS and CMOS inverter:

A basic requirement for producing a complete range of logic circuits is the inverter, the inverter is needed for restoring logic levels, for NAND and NOR gates, and for sequential and memory circuits of various forms.

- The basic inverter circuit requires a transistor with source connected to ground and a load resistor of some sort connected from the drain to the positive supply rail V_{DD}. The output is taken from the drain and the input applied between gate and ground.
- Use of depletion mode MOS is preferred as resistors are not conveniently produced on the silicon substrate.



nMOS inverter and its transfer characteristics

The gain of the nMOS is determined by the slope of transfer characteristics, which is,

$$Gain = \frac{\delta V_{out}}{\delta V_{in}}$$

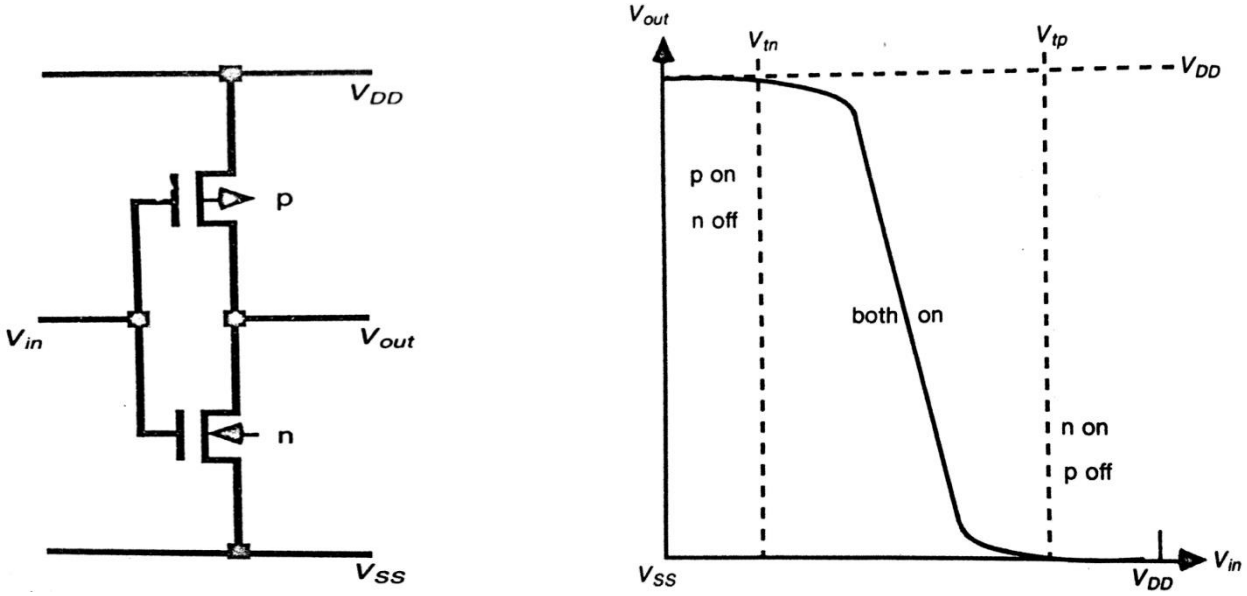
The current / voltage relationships for the MOS/ CMOS inverter transistor is given as,

$$I_{ds} = K\frac{W}{L}\left((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right)$$

and in the resistive region as,

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_{th})^2}{2}$$

The V_{ds} for nMOS is high since the output is high and V_{ds} for pMOS is less since the output is high.



CMOS inverter circuit and its transfer characteristics

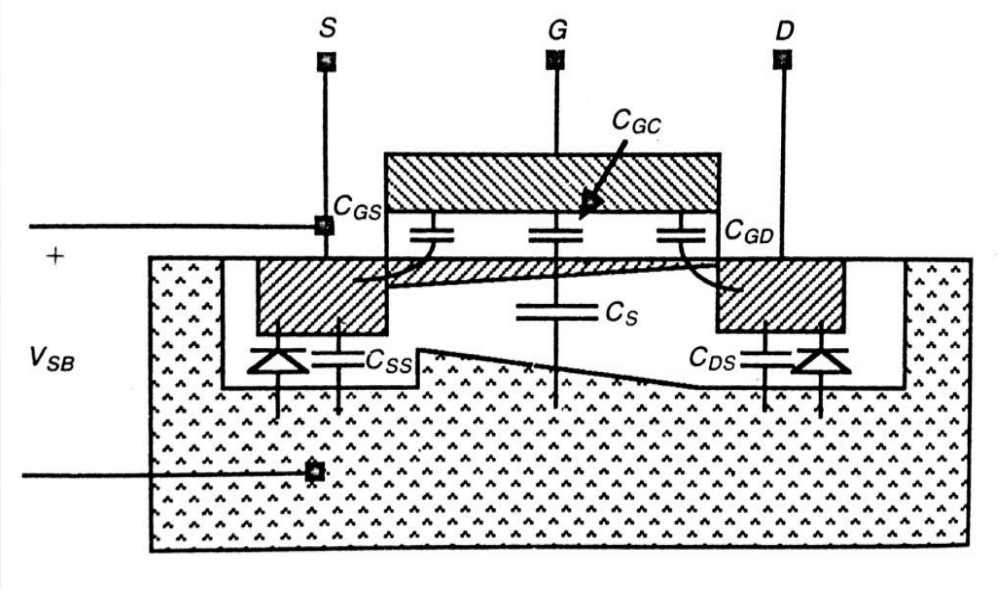
5. MOS transistor circuit model:

The MOS transistor can be modelled with varying degrees of complexity.

Considering the actual physical construction of the device leads to some understanding of the various components of the model.

- The capacitances associated are:
  - C_{GC} = gate to channel capacitance
  - C_{GS} = gate to source capacitance
  - C_{GD} = gate to drain capacitance
  - C_{SS} = source to substrate capacitance
  - C_{DS} = drain to source capacitance
  - C_S = channel to substrate capacitances

Here C_{GS} and C_{GD} are small for self- aligning nMOS process.

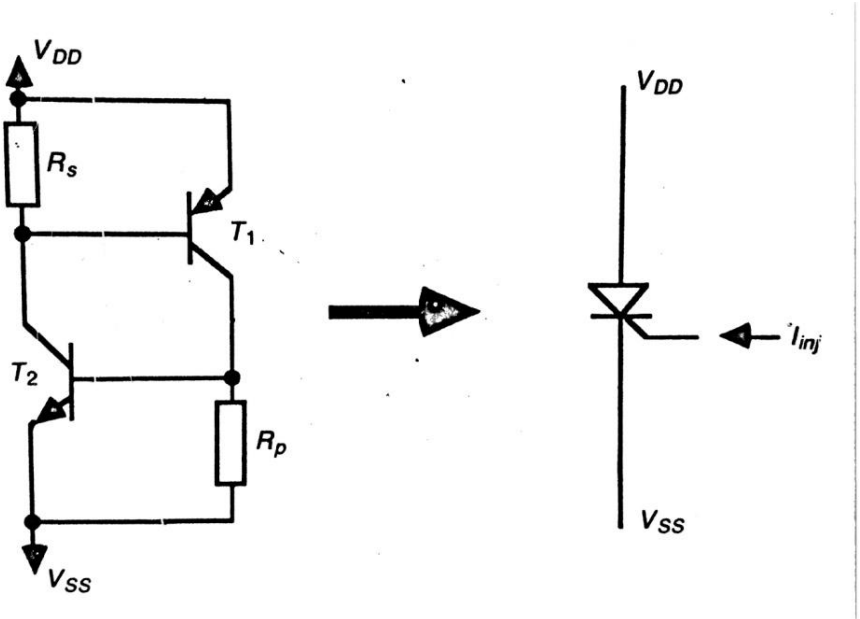


nMOS transistor model

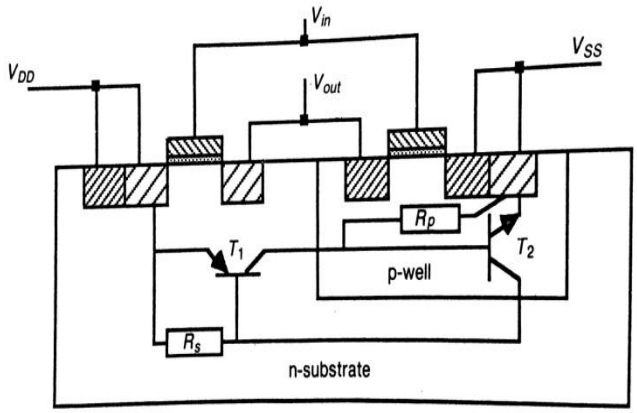
6. Latch- Up in CMOS circuits:

Latch- up is a condition in which the parasitic components give rise to the establishment of low-resistance conducting paths between V_{DD} and V_{SS} with consequent disastrous results. Therefore careful control during fabrication is necessary to avoid this problem.

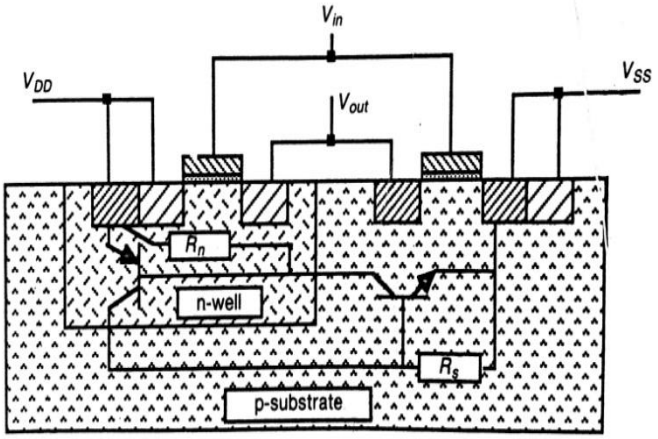
- Latches may be induced by glitches on the supply rails or by incident radiation. The mechanism involves the key parasitic components associated with a p- well structure in with an inverter circuit. There are, in effect, two transistors and two resistances associated with p- well and with the regions of the substrate which forms a path between V_{DD} and V_{SS}.



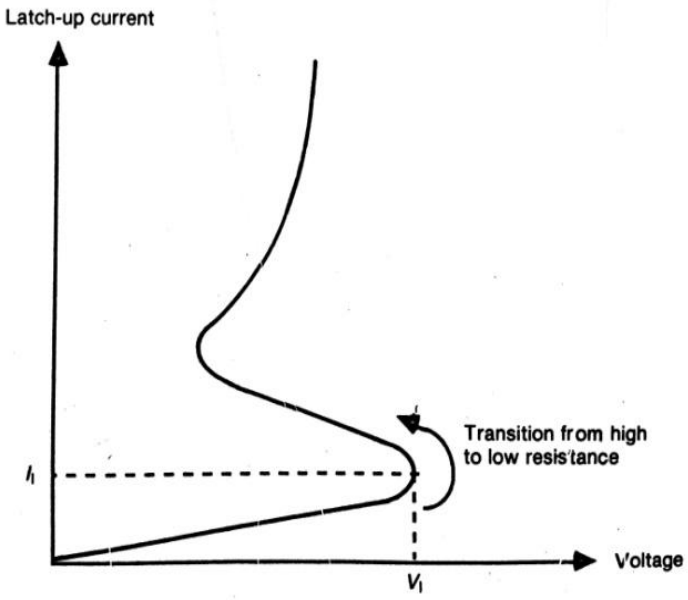
Latch- up circuit model



Latch up effect in p- well



Latch up effect in n- well



Latch- up current Vs voltage

7. Threshold Voltage and Body Effect:

The minimum voltage required between the gate and source V_{GS} necessary to cause an inversion layer so as to create the conducting channel between the source and drain is called a **threshold voltage (V_{th})**.

The threshold voltage V_{th} may be expressed as:

$$V_{th} = \phi_{ms} + \frac{Q_B - Q_{SS}}{C_0} + 2\phi_{fN}$$

Where:

$$V_{th} = threshold\ voltage$$

$$\phi_{ms} = work\ function\ difference\ between\ gate\ and\ Silicon$$
$$Q_B = charge\ per\ unit\ area\ in\ the\ depletion\ layer\ beneath\ the\ oxide$$
$$Q_{SS} = charge\ density\ at\ Si{:}SiO_2 interface$$
$$C_0 = capacitance\ per\ unit\ gate\ area$$
$$\phi_{fN} = Fermi\ level\ potential\ between\ inverted\ surface\ and\ bulk\ Si$$

When V_{SB} causes the channel to be depleted of charge carriers and thus the threshold voltage V_{th} is raised, this change is V_{th} is expressed as,

$$V_{th} = V_{th0} + \gamma\sqrt{|-2\phi f| + V_{SB}} - \sqrt{|-2\phi f|}\ (at\ V_{gs} = 0)$$

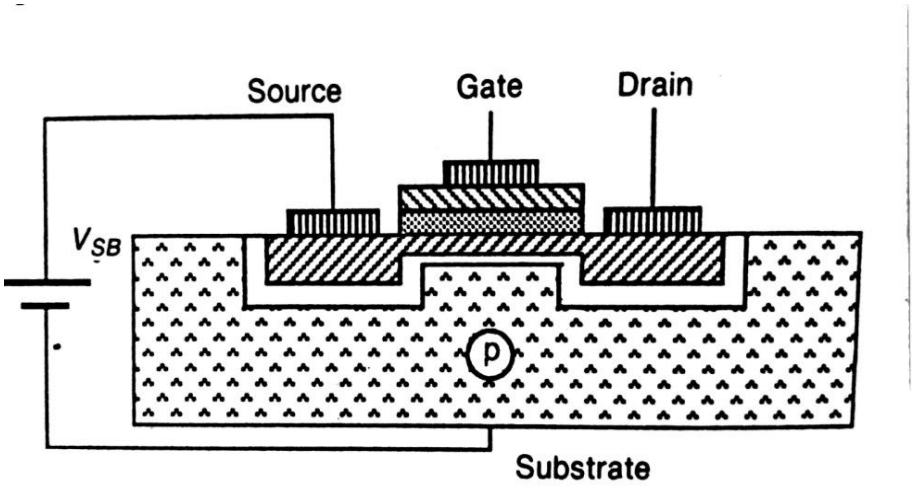
where:

$$\gamma = Body\ Effect\ Coefficient = \frac{1}{Cox}\sqrt{2\ \epsilon_{si}\ N\ A\ q}$$

$$V_{th0}\ is\ the\ threshold\ voltage\ at\ which\ V_{SB} = 0$$

- Threshold voltage is negative for pMOS and positive for nMOS.

When the substrate bias $V_{substrate}$ or V_{SB} gets added to the channel substrate junction potential, this leads to an increase of the gate- channel voltage drop. This is called **body effect** which affects the threshold voltage. This maintains the charge neutrality.



nMOS device sown with body effect

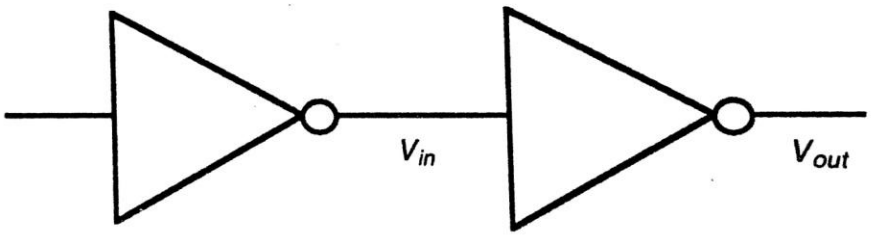
The body effect coefficient γ is given as,

$$\boldsymbol{\gamma = Body\ Effect\ Coefficient = \frac{1}{Cox}\sqrt{2\ \epsilon_{si}\ N\ A\ q}}$$

8. Pull- up to pull- down ratio (Z_{pu} / Z_{pd}) for an nMOS inverter driven by another nMOS inverter:

Considering an inverter is driven from the output of another similar inverter. Consider the depletion mode transistor for which $V_{gs} = 0$ under all conditions, with

$$V_{in} = V_{out} = V_{inverter}$$



nMOS inverter driven directly from another inverter

WKT,

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_{th})^2}{2} \quad (Equation\ 1)$$

In depletion mode $V_{gs} = 0$, therefore the above equation 1 becomes,

$$I_{ds} = K\frac{W_{pu}}{L_{pu}}\frac{(-V_{thd})^2}{2} \quad (Equation\ 2)$$

In enhancement mode $V_{gs} = V_{inverter}$, therefore the above equation 1 becomes,

$$I_{ds} = K\frac{W_{pd}}{L_{pd}}\frac{(V_{inverter} - V_{th})^2}{2} \quad (Equation\ 3)$$

Equating equations 3 and 2 we get

$$K\frac{W_{pd}}{L_{pd}}\frac{(V_{inverter} - V_{th})^2}{2} = K\frac{W_{pu}}{L_{pu}}\frac{(-V_{thd})^2}{2}$$

$$\frac{W_{pd}}{L_{pd}}(V_{inverter} - V_{th})^2 = \frac{W_{pu}}{L_{pu}}(-V_{thd})^2 \quad \text{(Equation 4)}$$

Here W_{pu}, W_{pd} L_{pu} and L_{pd} are the widths and lengths of the pull − up and pull − down transistors respectively.

WKT,

$$\frac{L_{pd}}{W_{pd}} = Z_{pd}\ and\ \frac{L_{pu}}{W_{pu}} = Z_{pu} \quad (Equation\ 5)$$

Substituting equation 5 in equation 4 respectively, we get

$$\frac{1}{Z_{pd}}(V_{inverter} - V_{th})^2 = \frac{1}{Z_{pu}}(-V_{thd})^2$$

$$V_{inverter} = V_{th} - \frac{V_{td}}{\sqrt{\frac{Z_{pu}}{Z_{pd}}}} \quad (Equation\ A)$$

The typical values for V_{th}, V_{thd} and $V_{inverter}$ are V_{th} = 0.2 V_{DD}, V_{thd} = - 0.6 V_{DD} and $V_{inverter}$ = 0.5 V_{DD} (for equal margins)

Substituting the above values in equation A, we get

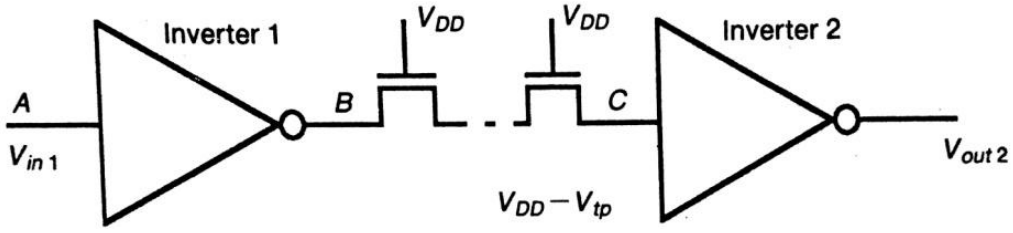
$$0.5 = 0.2 + \frac{0.6}{\sqrt{\frac{Z_{pu}}{Z_{pd}}}}$$

$$\sqrt{\frac{Z_{pu}}{Z_{pd}}} = 2$$

$\frac{Z_{pu}}{Z_{pd}} = \mathbf{4}$**,** for an inverter directly driven from an inverter.

- The pull- up to pull- down ratio for an nMOS inverter driven through one or more pass transistors is given as,

$$\frac{\frac{Z_{pu\,2}}{Z_{pd\,2}}}{\frac{Z_{pu\,1}}{Z_{pd\,1}}} = \mathbf{8},$$ summarization for an nMOS transistor



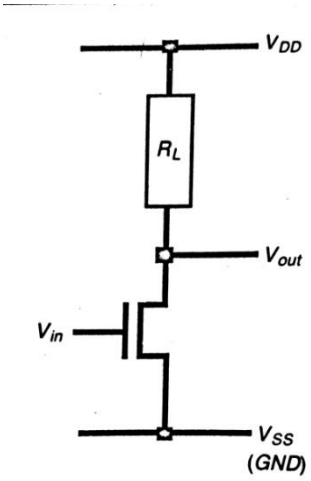
Pull- up to pull- down ratios for inverting logic coupled by pass transistors

9. Design of MOS inverters with different loads/ Alternative forms of Pull- Up:

There are four possible different loads to which the inverter is subjected:

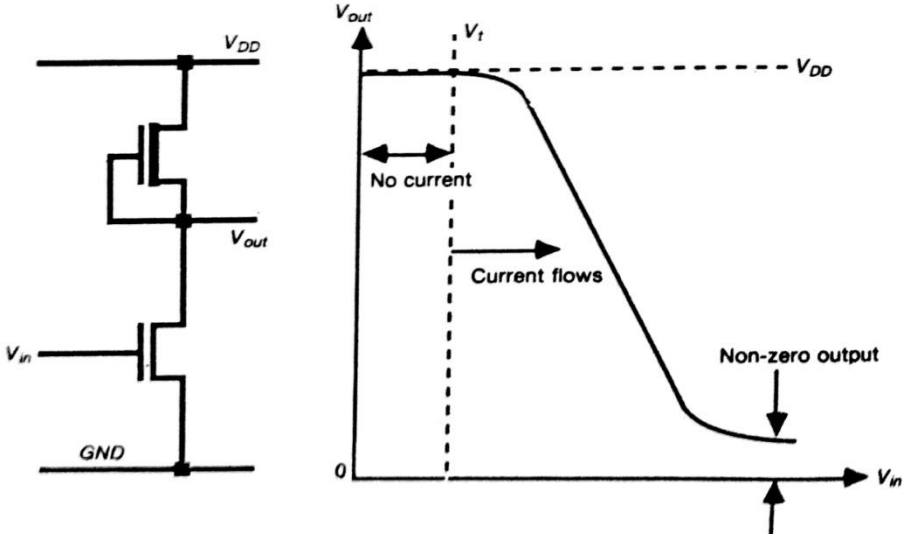
1. Load Resistance R_L:

   This arrangement is not practical due to the large space requirements of resistors produced in a silicon substrate.



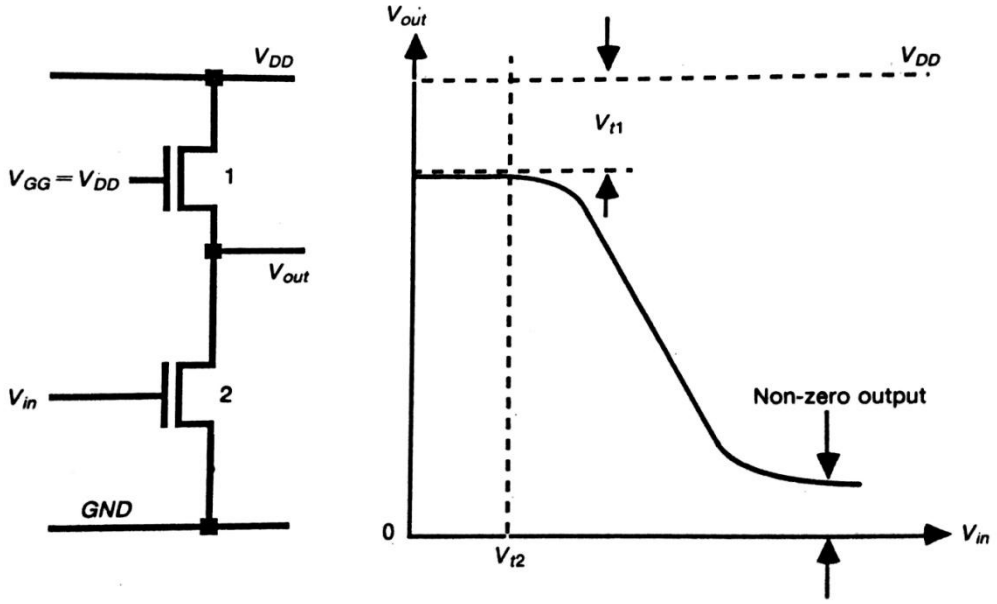
Resistor Pull- Up

2. nMOS Depletion Mode Transistor Pull up:
   a. Dissipation is high since current flows when V_{in} = logical 1.
   b. Switching of output from 1 to 0 commences when V_{in} exceeds V_{th} of the pull down.
   c. When switching the output from 1 to 0. The pull up device is non saturated initially and this presents lower resistance through which to charge capacitive loads.



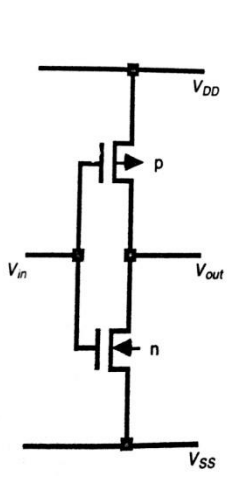
nMOS Depletion Mode Transistor Pull- Up And Transfer Characteristic

3. nMOS Enhancement mode pull up:
    a. Dissipation is high since current flows when V_{in} = logical 1 if V_{GG} is returned to V_{DD}.
    b. V_{out} can never reach V_{DD} (logical 1) if $V_{GG} = V_{DD}$ as is normally the case.
    c. V_{GG} may be derived from a switching source for example, one phase of the clock, so that dissipation can be greatly reduced.
    d. If V_{GG} is higher than V_{DD} then an extra supply rail is required.

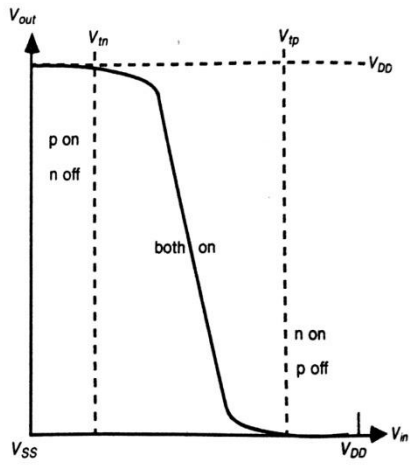


nMOS Enhancement Mode Transistor Pull- Up And Transfer Characteristic

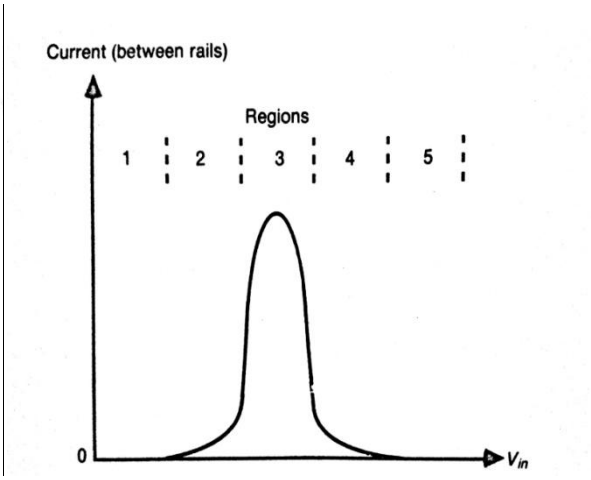
4. Complementary transistor pull- up (CMOS):
    a. No current flow either for logical 0 or for logical 1 inputs.
    b. Full logical 1 and 0 levels are presented at the output.
    c. For devices of similar dimensions the p- channel is slower than the n- channel device.



Circuit (CMOS)



Transfer Characteristics

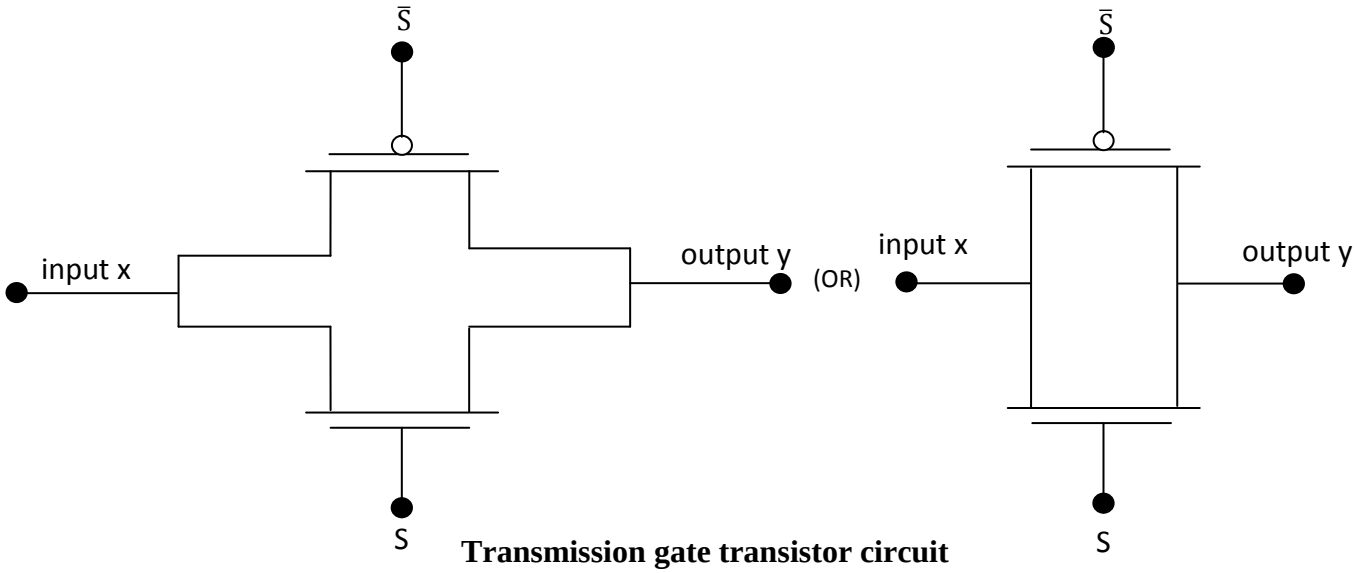


Current Vs V_{in}

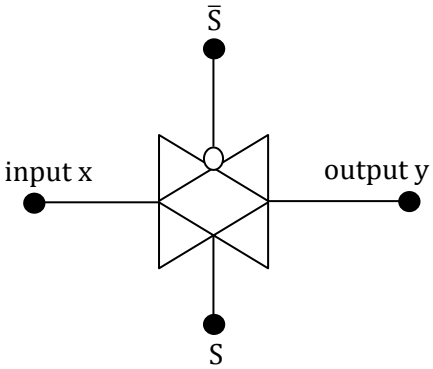
Transmission Gate/ CMOS Transmission Gate (TG) Logic:

The transmission gate (TG) is used in digital CMOS circuit design to pass or not pass a signal. The gate is made up of the parallel connection of p and n channel MOS devices/ pMOS and nMOS. The resistance between the input and the output can be estimated as $R_n \parallel R_p$. Transmission gates has the simplicity of switching and the ability to transmit the entire range of voltages.

- The TG logic technique builds on the complementary properties of nMOS and pMOS transistors i.e. nMOS devices pass a strong 0, but weak 1 while pMOS transistors pass a strong 1, but weak 0. Leading ideally the use of nMOS as pull down and pMOS as pull up.
- It is widely used solution to deal with voltage drop problem.

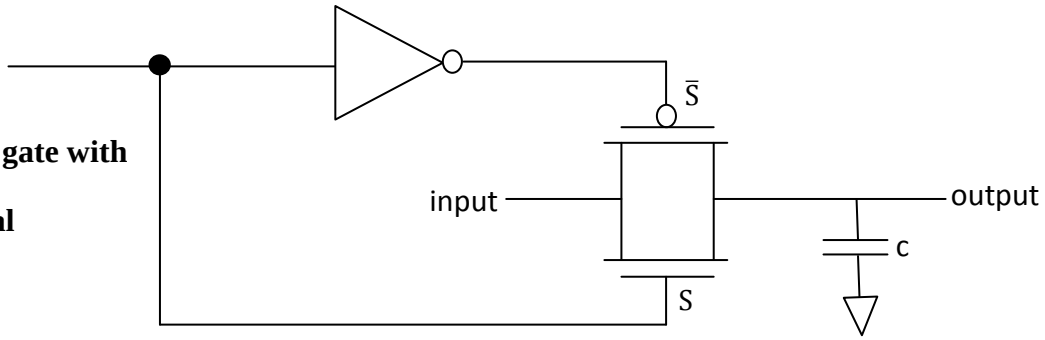


Transmission gate transistor circuit



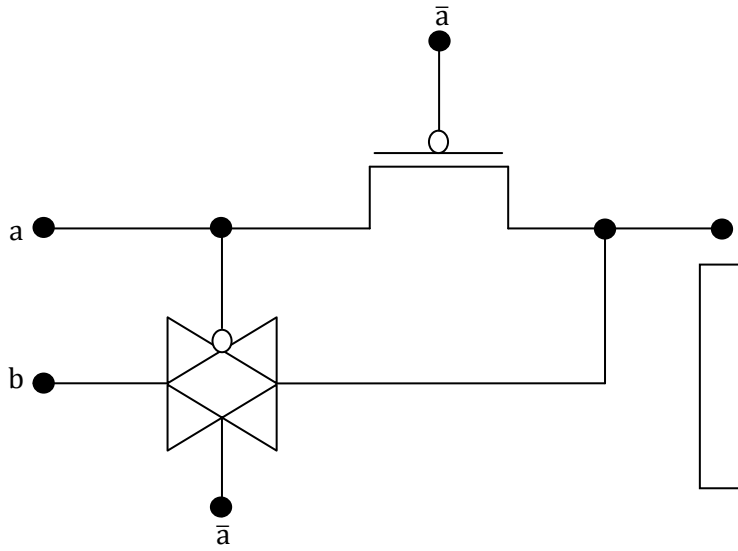
Transmission gate symbol

CMOS transmission gate with control signal



Transmission Logic Circuits:

1. Transmission Logic circuit for OR Gate/ Transmission based OR Gate:

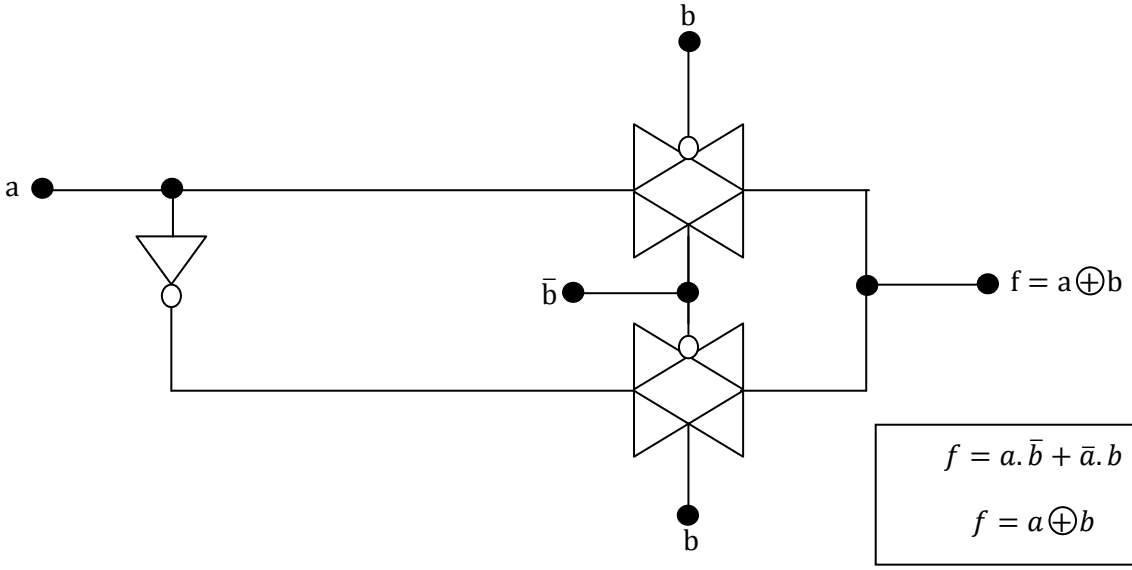


$f = a.\overline{(\bar{a})} + \bar{a}.b$

$f = a + \bar{a}.b$

$f = a + b$

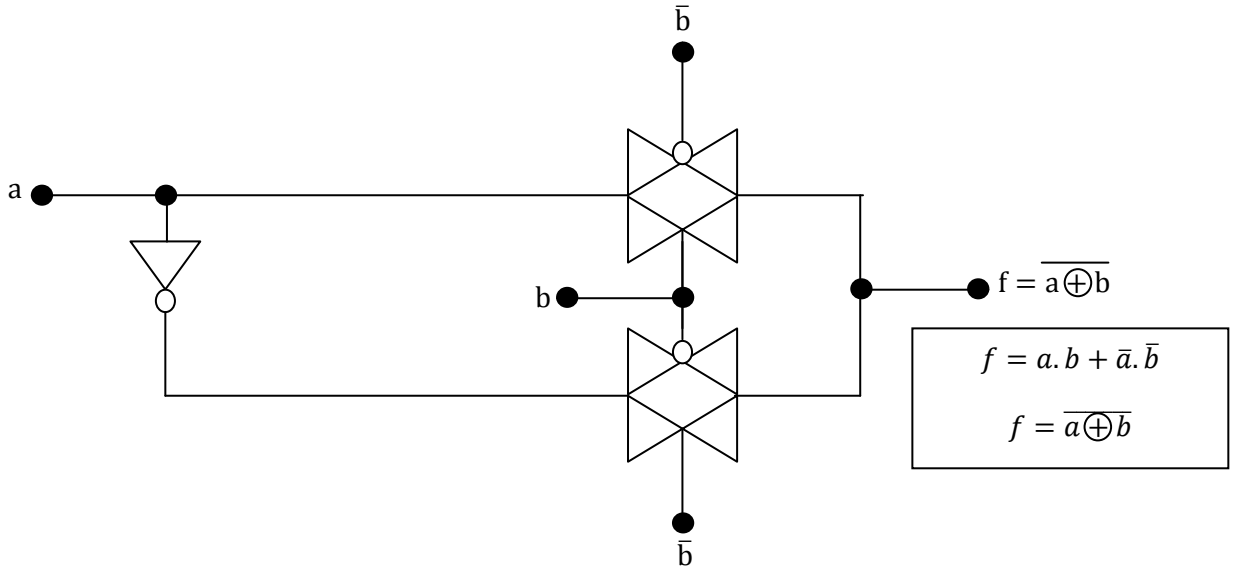
2. Transmission Logic circuit for XOR Gate/ Transmission based XOR Gate:



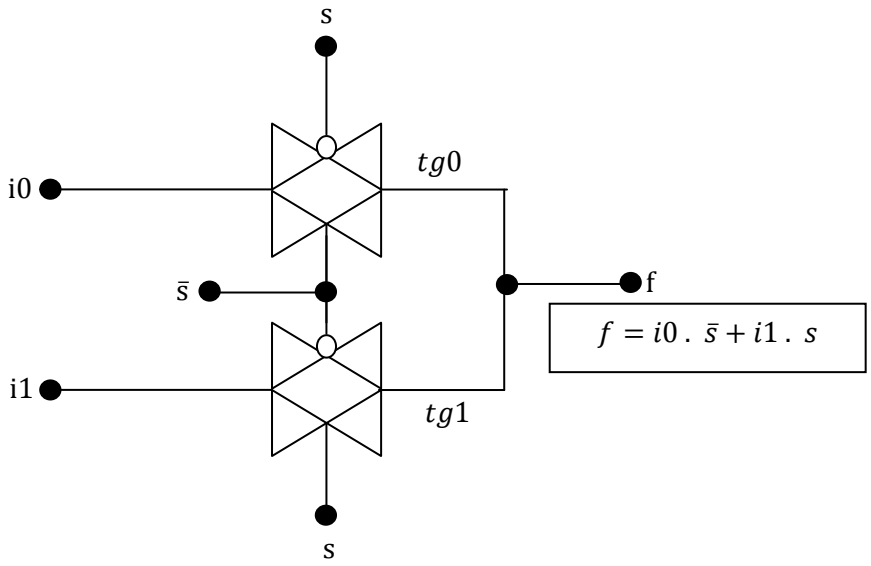
$f = a.\bar{b} + \bar{a}.b$

$f = a \oplus b$

3. Transmission Logic circuit for XNOR Gate/ Transmission based XNOR Gate:



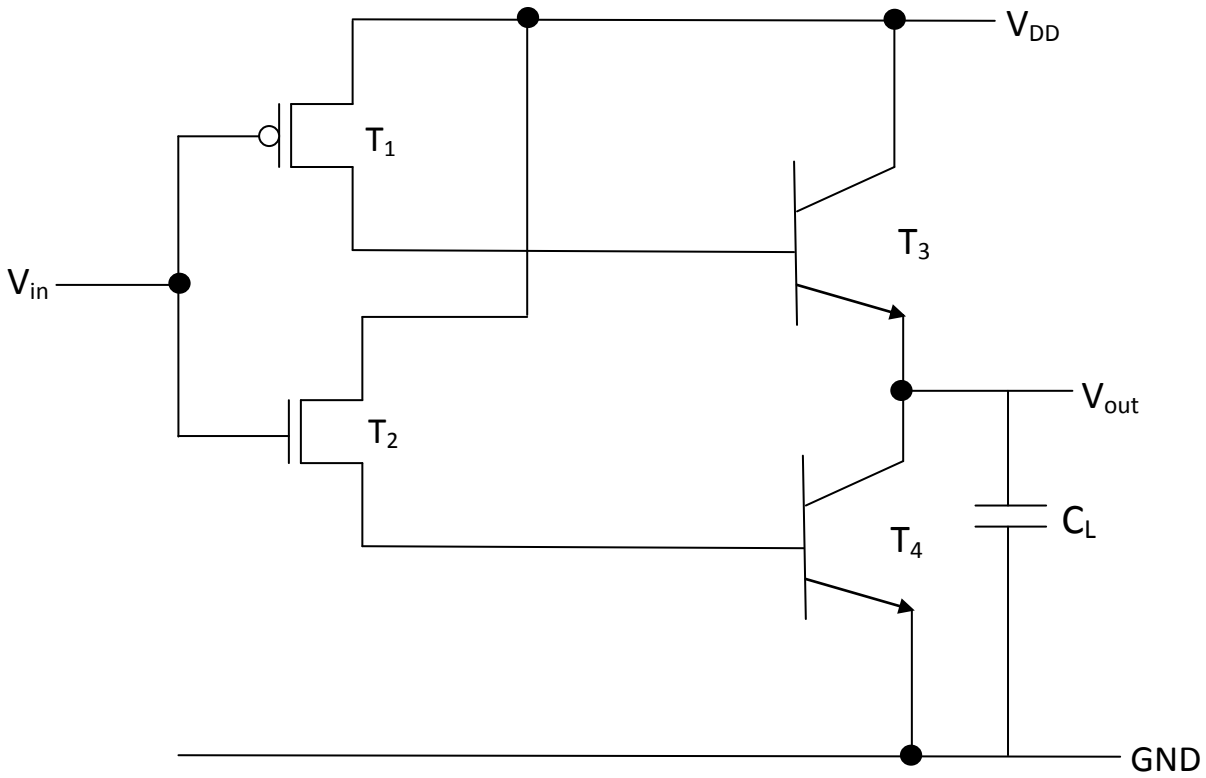
4. Transmission Logic circuit for 2- to- 1multiplexor/ Transmission based 2- to- 1multiplexor:



s	tg0	tg1	f
0	closed	open	i0
1	open	closed	i1

BiCMOS Inverter:

The BiCMOS inverter consist of two bipolar transistors T_3 and T_4 with one pMOS T_1 and one nMOS T_2 transistors, which are in enhancement mode respectively.



BiCMOS Inverter

As seen above the BiCMOS inverter operates with the use of two bipolar transistors, a pMOS and a nMOS transistor. The reason for preferring a BiCMOS inverter is its enhanced speed and in the BiCMOS inverter the area and power dissipation increases.

Operation:

Case 1:

With $V_{in} = 0$, T_1 is ON and T_3 is conducting but T_2 is OFF and T_4 is non conducting and since T_1 is ON and T_3 is conducting, acts as a current source to charge load capacitance to get V_{out} to be V_{DD}.

$V_{in} = 0$, $V_{out} = V_{DD}$			
T_1	**T_2**	**T_3**	**T_4**
ON	OFF	ON	OFF

Case 2:

With $V_{in} = V_{DD} = 5V = 1$, T_2 is ON and T_4 is conducting but T_1 is OFF and T_3 is non conducting and since T_2 is ON and T_4 is conducting, the load capacitance discharges through T_4 to make V_{out} to become 0V.

V_{in} = 1, V_{out} = C_L = 0			
T_1	**T_2**	**T_3**	**T_4**
OFF	ON	OFF	ON

So, in case 1 input is low and output is high, whereas in case 2 input is high and output is low.

The BiCMOS has the following advantages:

1. Low output resistance and high input resistance.
2. High current capability and high load current sinking.
3. It has an enhanced speed.

The main disadvantage of BiCMOS is that it lowers the noise margin of the logic. As the maximum output voltage is approximately V_{DD} – 0.7V, while the minimum logic output voltage is approximately 0.7V. Therefore, the low- output voltage of 0.7V is very close to the threshold voltage, susceptible to noise and in a BiCMOS inverter area and power dissipation increases.

Switching Characteristics of BiCMOS Inverter:

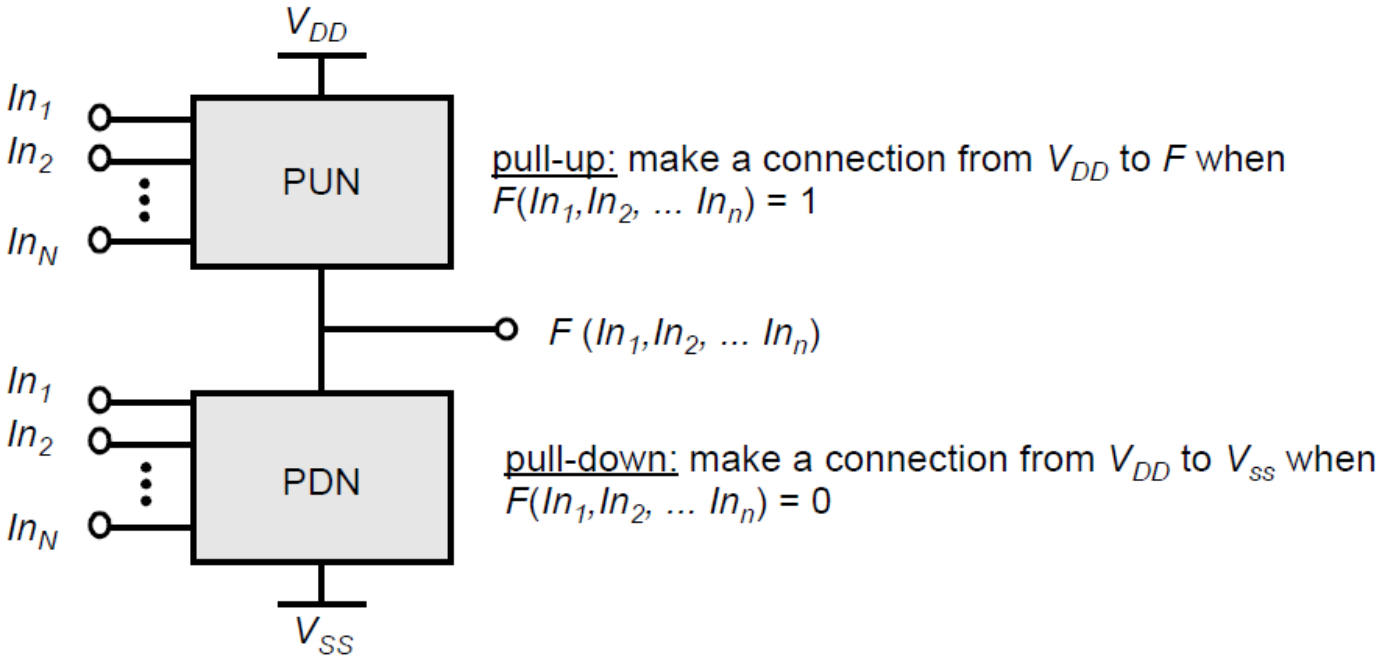
The delay associated with the BiCMOS inverter discharging a capacitance C_L, consists of two parts:

- The delay in T_4 turning on and the delay once C_L is discharging is through T_4. The delay associated with discharging C_L is given by $t_L = R_{npn} - C_L$.
- The low- to- high delay time can be estimated in much the same way as the high- to- low delay. The delay in charging C_L is given by $t_H = R_{npn}\ C_L = t_L$.

Basic Logic Gates with CMOS: (INVERTER, NAND, NOR, AOI and OAI Gates)

Here we design static circuits in which at every point in time, each gate output is connected to either V_{DD} or V_{ss} or GND via low resistance path. This is a static complementary CMOS design which is combination of two networks i.e.

1. The Pull- up network (PUN)- contains only pMOS transistors
2. The Pull- down network (PDN)- contains only nMOS transistors



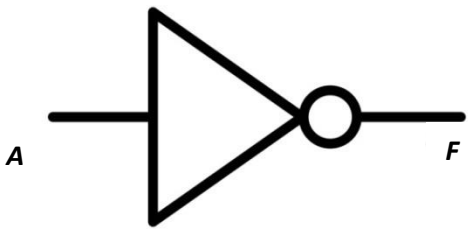
Designing:

For NAND Logic	For NOR Logic
PUN- pMOS transistors - Parallel Connection	PUN- pMOS transistors - Series Connection
PDN- nMOS transistors - Series Connection	PDN- nMOS transistors - Parallel Connection

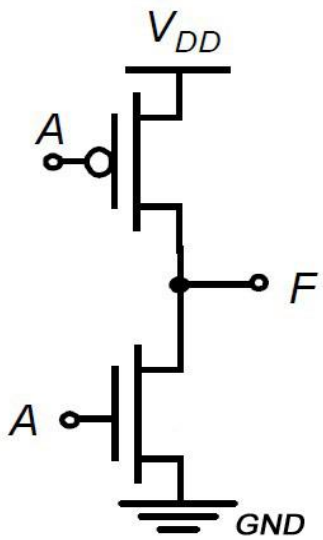
Note:
NAND logic implies to AND logic and
NOR logic implies to OR logic

1. NOT/ INVERTER LOGIC USING CMOS:

The CMOS inverter is obtained by connecting a pMOS in series with a nMOS. The CMOS inverter transistor circuit verifies the truth table of the inverter logic.



Gate Level Circuit Diagram



CMOS Transistor level circuit

Input A	Output F
0	1
1	0

Truth Table

Verliog HDL Description in Switch Level Modelling	Test Bench/ Simulation/ Stimulation

module my_not (f,a,);
input a;
output f;
supply1 vdd; // vdd (power supply)
supply0 gnd; // gnd (ground)
pmos (f,vdd,a); // instantiation of pmos switch
nmos (f,gnd,a); // instantiation of nmos switch
endmodule
	module my_not_test;
	reg a;
	wire f;
	my_not uut (f,a);
	initial
	begin
	$monitor ($time,"a=%b,f=%b",a,f);
	#100 a=0;
	#100 a=1;
	end
	endmodule

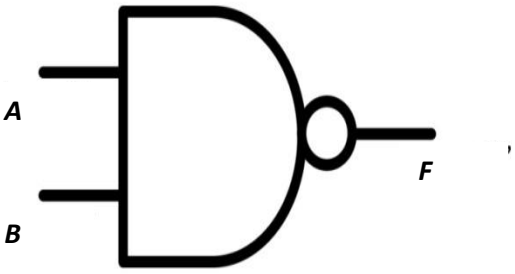
2. NAND GATE USING CMOS LOGIC (2 input):

A NAND based CMOS transistor circuit is obtained by connecting and using the inputs in both pMOS and nMOS transistors in the design as,

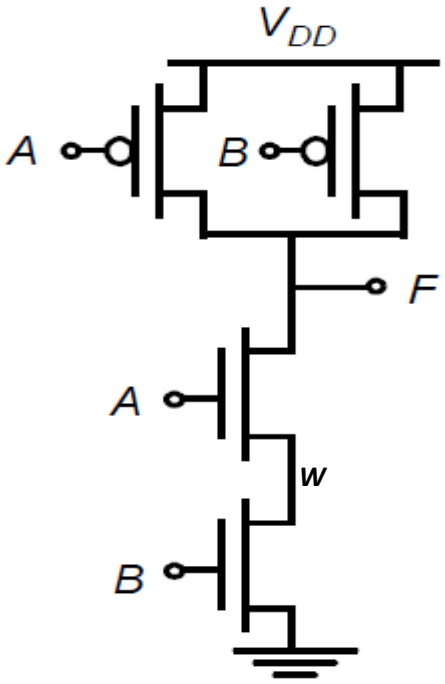
- PUN- pMOS transistors- Parallel Connection
- PDN- nMOS transistors - Series Connection

$$NAND\ FUNCTION\ (F = \overline{A.B})$$

The CMOS NAND transistor circuit verifies the truth table of the NAND logic.



Gate Level Circuit Diagram



CMOS Transistor level circuit

Input A	Input B	Output F
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

Verliog HDL Description in Switch Level Modeling	Test Bench/ Simulation/ Stimulation

module my_nand(f,a,b);
input a,b;
output f;
wire w; // internal wire w
supply1 vdd; // vdd (power supply)
supply0 gnd; // gnd (ground)
pmos (f,vdd,a); // instantiation of pmos switch
pmos (f,vdd,b); // instantiation of pmos switch
nmos (f,w,a); // instantiation of nmos switch
nmos (w,gnd,b); // instantiation of nmos switch
endmodule
	module my_nand_test;
	reg a,b;
	wire f;
	my_nand uut (f,a,b);
	initial
	begin
	$monitor
	($time,"a=%b,b=%b,f=%b",a,b,f);
	#100 a=0;b=0;
	#100 a=0;b=1;
	#100 a=1;b=0;
	#100 a=1;b=1;
	end
	endmodule

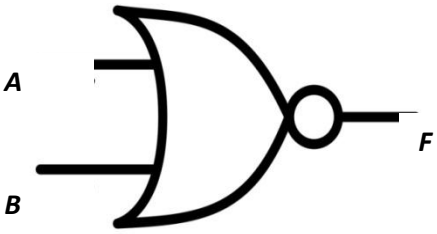
3. NOR GATE USING CMOS LOGIC (2 input):

A NOR based CMOS transistor circuit is obtained by connecting and using the inputs in both pMOS and nMOS transistors in the design as,

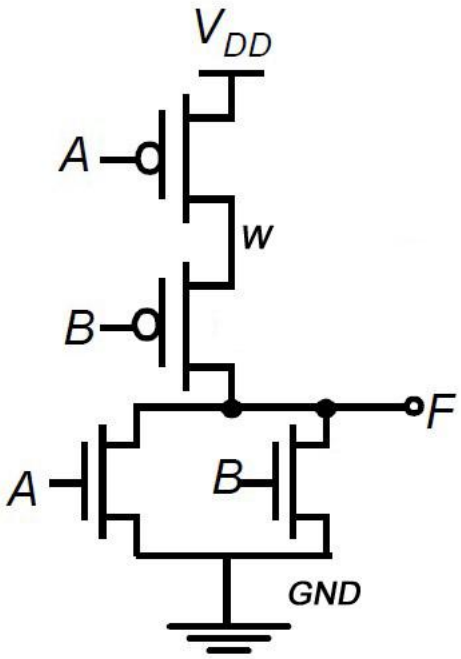
- PUN- pMOS transistors- series Connection
- PDN- nMOS transistors - Parallel Connection

$$NOR\ FUNCTION\ (F = \overline{A + B})$$

The CMOS NOR transistor circuit verifies the truth table of the NOR logic.



Gate Level Circuit Diagram



CMOS Transistor level circuit

Input A	Input B	Output F
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table

Verliog HDL Description in Switch Level Modelling	Test Bench/ Simulation/ Stimulation

module my_nor (f,a,b);
input a,b;
output f;
wire w; // internal wire w
supply1 vdd; // vdd (power supply)
	module my_nor_test;
	reg a,b;
	wire f;
	my_nor uut (f,a,b);
	initial

supply0 gnd; // gnd (ground)
pmos (w,vdd,b); // instantiation of pmos switch
pmos (f,w,a); // instantiation of pmos switch
nmos (f,gnd,a); // instantiation of nmos switch
nmos(f,gnd,b); // instantiation of nmos switch
endmodule
	begin
	$monitor
	($time,"a=%b,b=%b,f=%b",a,b,f);
	#100 a=0;b=0;
	#100 a=0;b=1;
	#100 a=1;b=0;
	#100 a=1;b=1;
	end
	endmodule

4. AOI LOGIC GATE (AND - OR - INVERTER LOGIC GATE):

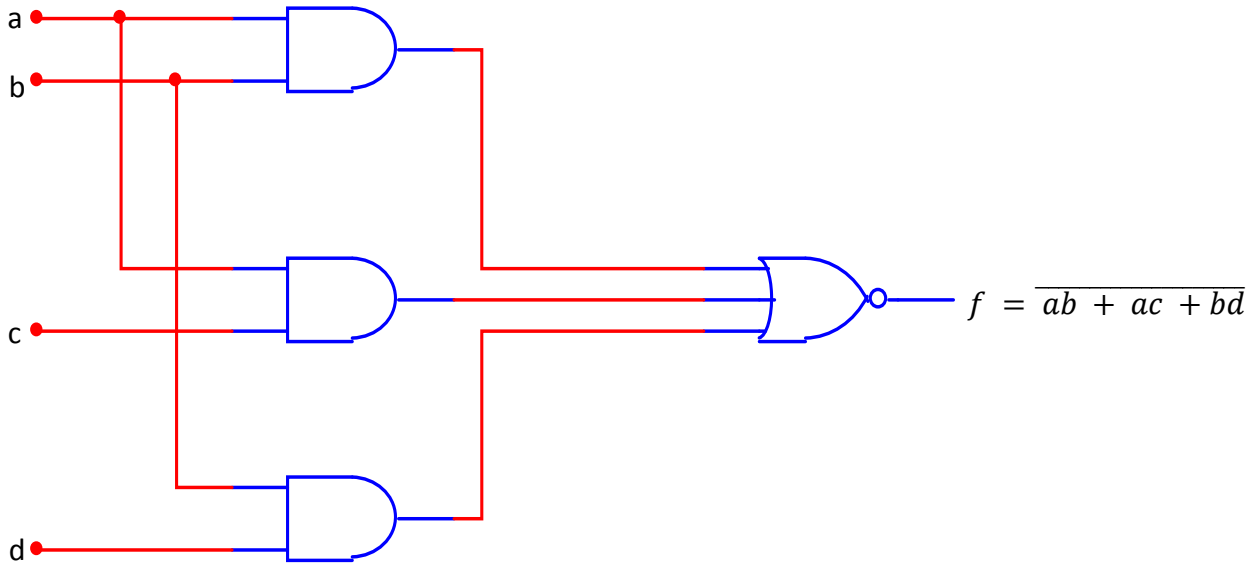
The AOI logic function implements the operation in the order AND, OR and INVERTER/ NOT. It is an inverted SOP (Sum of Products) function i.e.

$$f = \overline{ab + ac + bd}$$

for the inputs a, b, c and d respectively.

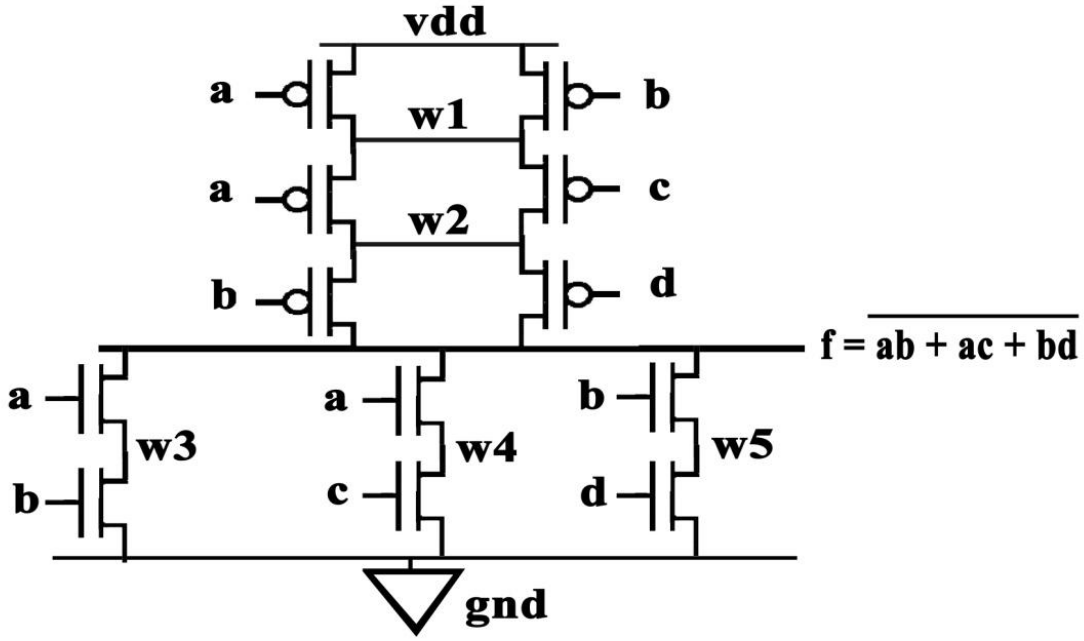
The CMOS transistor implementation is obtained following the design rules of both NAND and NOR logic i.e.

For NAND Logic	For NOR Logic
PUN- pMOS transistors - Parallel Connection	PUN- pMOS transistors - Series Connection
PDN- nMOS transistors - Series Connection	PDN- nMOS transistors - Parallel Connection



GATE LEVEL CIRCUIT DIAGRAM FOR AOI GATE

The AOI CMOS transistor circuit verifies the AOI logical performance i.e. its truth table.



CMOS TRANSISTOR LEVEL CIRCUIT DIAGRAM FOR AOI GATE

Inputs				Output
a	b	c	d	f
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE

5. OAI LOGIC GATE (OR - AND - INVERTER LOGIC GATE):

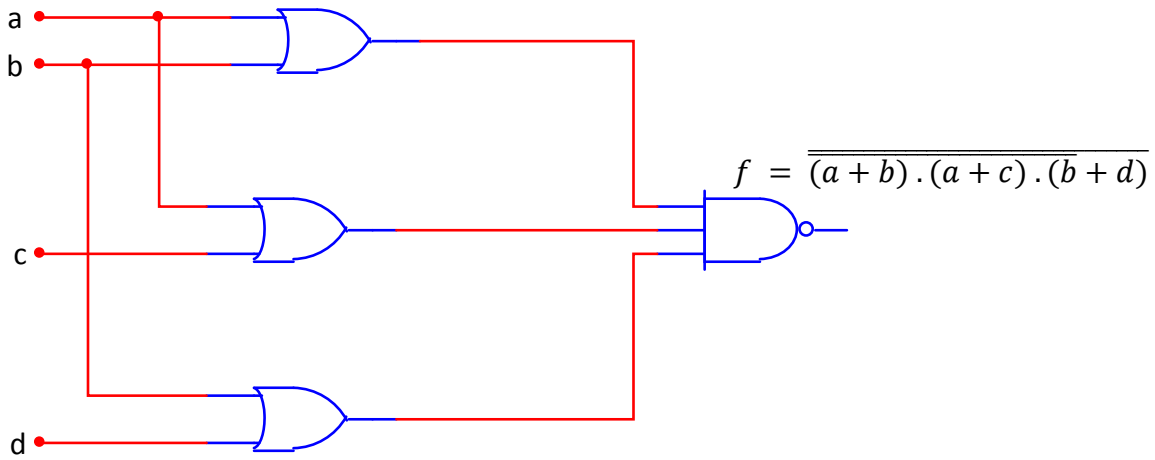
The OAI logic function implements the operation in the order OR, AND, and INVERTER/ NOT. It is an inverted POS (Product of Sums) function i.e.

$$f = \overline{(a+b).(a+c).(b+d)}$$

for the inputs a, b, c and d respectively.

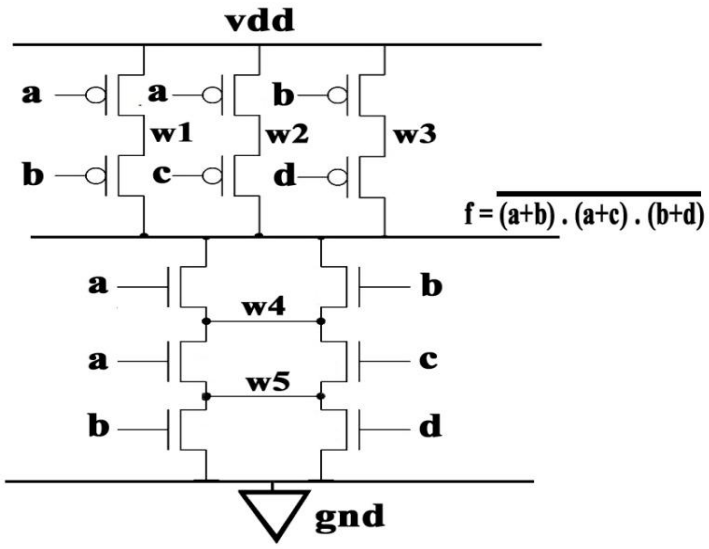
The CMOS transistor implementation is obtained following the design rules of both NAND and NOR logic i.e.

For NAND Logic	For NOR Logic
PUN- pMOS transistors - Parallel Connection	PUN- pMOS transistors - Series Connection
PDN- nMOS transistors - Series Connection	PDN- nMOS transistors - Parallel Connection



GATE LEVEL CIRCUIT DIAGRAM OF OAI

The OAI CMOS transistor circuit verifies the OAI logical performance i.e. its truth table.



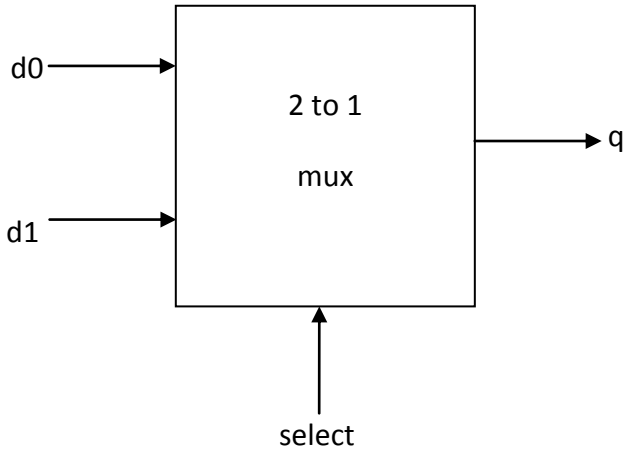
CMOS TRANSISTOR LEVEL CIRCUIT FOR OAI GATE

Inputs				Output
a	**b**	**c**	**d**	**f**
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

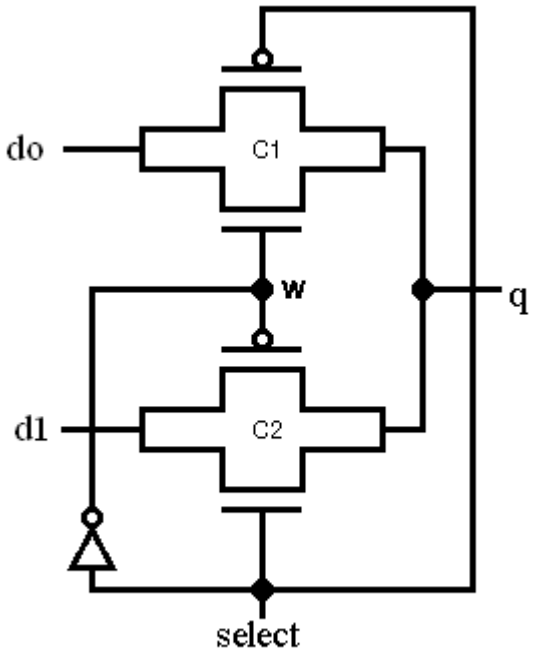
TRUTH TABLE

(Write switch level programs for AOI and OAI by yourself)

6. CMOS 2 to 1 MULTIPLEXER:



Gate Level Circuit Diagram



CMOS Transistor Circuit Diagram