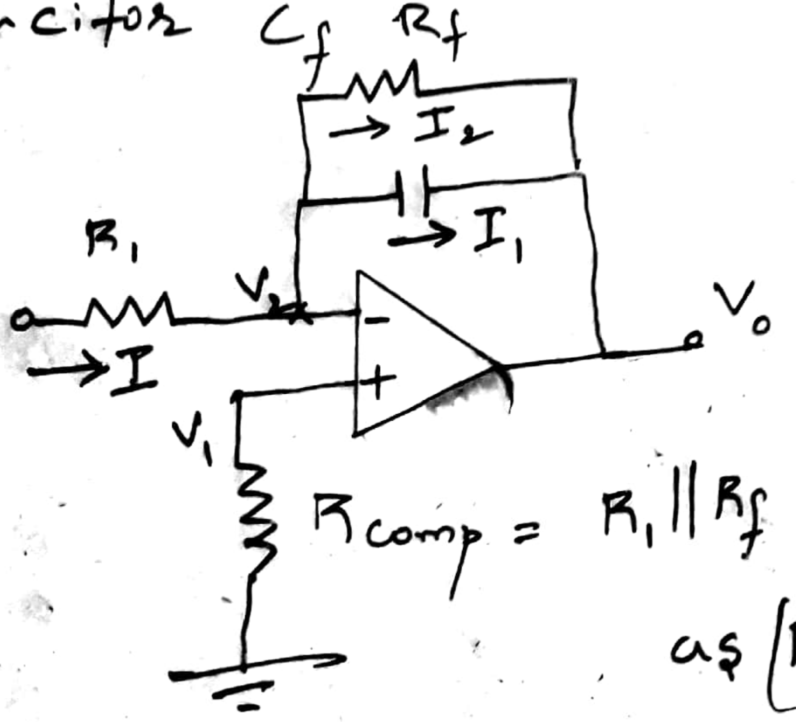
Practical Integrator: The limitations of an ideal integrator can be minimized in the Practical " ckt. which use a resistance R_f in parallel with capacitor C_f



$R_{comp} = R_1 || R_f = R_1$

as $(R_f >> R_1)$

*) The Resistance R_{comp} is also used to overcome the error due to bias current.

Analysis of practical Integrator

→ since i/p I inside op-amp is zero, the node 'B' is ground potential from the concept of virtual ground I (2)

$V_1 = V_2 = 0$

$$I = \frac{V_1 - V_2}{R_1}$$

$$= V_1/R_1 \quad (\because V_2 = 0)$$

$$||^{ly}\ I_1 = \frac{C_f\, d(V_2 - V_0)}{dt}$$

$$= \frac{-C_f\, dV_0}{dt}$$

$$I_2 = \frac{V_2 - V_0}{R_f}$$

$$I_2 = \frac{-V_0}{R_f}$$

Applying KCL at node 'A'

$$I = I_1 + I_2$$

$$\frac{V_{in}}{R_1} = \frac{-C_f\, dV_0}{dt} - \frac{V_0}{R_f}$$

Taking lapalace transform to the above equ

$$\frac{V_i(s)}{R_1} = -sC_f V_0(s) - \frac{V_0(s)}{R_f}$$

substitute I_1, I, I_2 valus in above Equ

$$\frac{V_i(s)}{R_1} = -V_o(s)\left(sC_f - 1/R_f\right)$$

$$\frac{V_i(s)}{R_1} = \frac{-V_o(s)\left(1+sC_fR_f\right)}{R_f}$$

$$= \frac{1}{\frac{R_1}{R_f}\left(1+sC_fR_f\right)} V_i(s)$$

$$-\frac{V_i(s)R_f}{\left(1+sC_fR_f\right)R_1} = V_o(s)$$

$$= \frac{1}{\frac{R_1}{R_f} + \frac{sR_1C_f\cancel{R_f}}{\cancel{R_f}}} V_i(s)$$

$$V_o(s) = \frac{R_f}{R_1\left(1+sC_fR_f\right)} V_i(s)$$

When R_f is large than

R_1/R_f can be neglected

$$V_o(s) = \frac{1}{\left(\frac{R_1}{R_f} + sR_1C_f\right)} \cdot V_i(s)$$

I ④

$$V_0(s) = \frac{1}{S R_1 C_f} V_i(s)$$

on Applying inverse laplace to above Equ

$$\boxed{V_0(t) = -\frac{1}{R_1 \cdot C_f} \int V_i(t)\, dt}$$