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Mitigation of Balanced and Unbalanced Voltage sag and Improving the Power Quality Using DVR

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Abstract: Voltage disturbances are the most common power quality problem due to increased use of complicated electronic equipment in industrial distribution system. There are many different solutions to compensate voltage sag but the use of a Dynamic Voltage Restorer (DVR) is considered to be the most effective method. This paper gives the investigation on DVR which compensates the balanced and unbalanced voltage sag at the load side. In this paper a new control scheme based on Synchronous reference frame theory is proposed to mitigate Voltage sag. The control scheme is verified using MATLAB/SIMULINK under different fault conditions.

Keywords: *DVR, power quality, Voltage Sag voltage swell.*

I. INTRODUCTION

Now a day, modern industrial equipments are based on electronic devices such as electrical drives and programmable logic controller. The electronic devices are very sensitive for the disturbances and are less tolerant to power quality problems such as voltage sags. Voltage sags are the most severe disturbances to the industrial equipments.

Voltage support at a load is achieved by reactive power injection at the load point of common coupling. The common method for this is to install mechanically operated shunt capacitors in the primary terminal of the distribution transformer. The mechanical switching may be via signals from a supervisory control and data acquisition (SCADA) system, with some timing schedule. The disadvantage is that, high speed transients cannot be compensated. Some sag is not corrected within the limited time with mechanical switching devices. Transformer taps may be used, but tap changing under load is not economical.

Another power electronic solution to the voltage regulation is by using custom power devices such as Unified power quality conditioner (UPQC), and Dynamic voltage restorer (DVR). DVR is one of the most custom power devices which inject voltage in series with the line to regulate the voltage at the load end..

II. OPERATION OF DVR

The general schematic diagram of DVR consists of an injection transformer, a harmonic filter, a voltage source converter (VSC), an energy storage unit and a control system. The single line diagram of DVR is shown in Fig. 1.

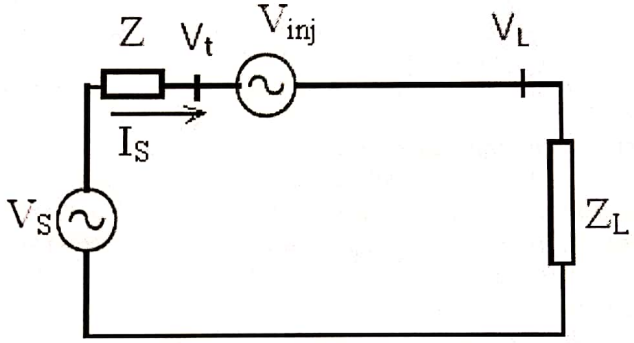

Fig 1: Single line diagram of DVR

The DVR injects a voltage (V_{inj}) in series with the terminal voltage (V_t) so that load voltage (V_L) is maintained a constant magnitude. The equivalent circuit of DVR is shown in Fig. 2. The system impedance Z_{TH} depends on the fault level of load bus. When the voltage (V_{TH}) drops, the DVR injects a series voltage (V_{inj}) through the injection transformer so that the required load voltage magnitude V_L can be maintained.

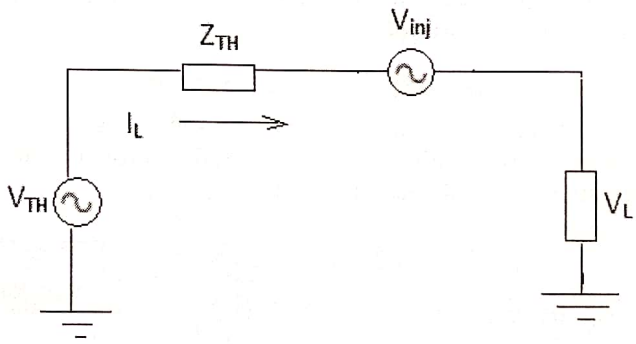

Fig 2: Equivalent circuit of DVR

The series injected voltage of the DVR can be written as

$$V_{DVR} = V_L + Z_{TH} I_L - V_{TH} \quad (1)$$

Where Z_{TH} : The load impedance condition

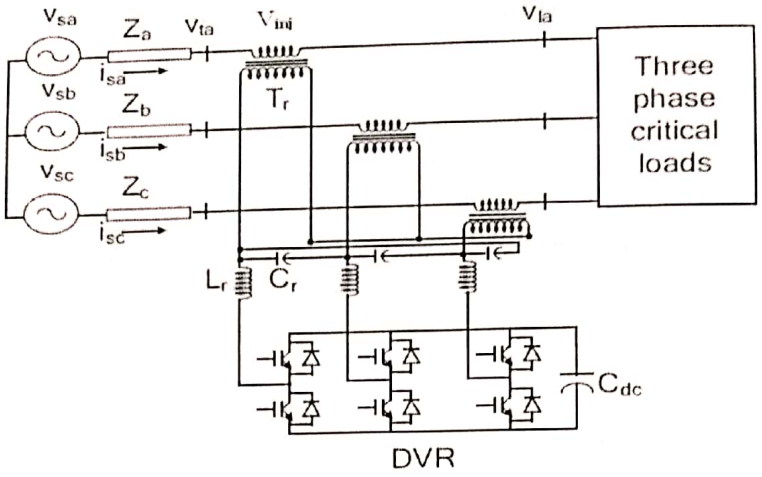

Fig 3: Three phase DVR scheme.

The source impedances (Z_a, Z_b, Z_c) are between source and the terminal. The DVR utilize three single phase transformers (T_r) To inject voltages in series with the terminal voltage. A voltage source converter (VSC) along with a DC capacitor (C_{dc}) is used to realize a DVR. The inductor in series (L_r) and the parallel capacitor (C_r) with the VSC are used to minimize the ripple in the injected voltage. The injected voltage has two components. The voltage injected in quadrature with the current is to maintain the load voltage at constant magnitude and in the in-phase voltage is to maintain the dc bus voltage of VSC and also to meet the power loss in the DVR. The control scheme is to achieve these two components of the injection voltage and this is possible by controlling the supply currents. The currents are sensed and these two components of currents, one is the component to maintain the DC bus voltage of DVR and the second one is to maintain the load terminal voltages, are added with the sensed load current to estimate the reference supply currents.

III. CONTROL SCHEME OF DVR

The proposed control scheme is based on estimation of reference supply currents. The proposed control scheme for the control of DVR is shown in Fig. 4.

The series compensator known as DVR is used to inject a voltage in series with the terminal voltage. The sag in terminal voltages are compensated by controlling the DVR and the proposed algorithm inherently provides a self-supporting dc bus for the DVR. The desired source currents (in d-q components) are obtained as

$$i_{sd} = i_d + i_{cd} \tag{2}$$

$$i_{sq} = i_q + i_{cq} \tag{3}$$

Where i_d and i_q are the average values of the d and q axis components of the current. i_{cd} is the output of the DC voltage controller and i_{cq} is the output voltage of the AC voltage controller. Three phase reference supply currents are derived using the sensed load voltages (V_{la}, V_{lb}, V_{lc}), terminal voltages (V_{ta}, V_{tb}, V_{tc}) and dc bus voltage (V_{dc}) of the DVR as feedback signals.

The synchronous reference frame theory based method is used to obtain the direct and quadrature axis components of the load currents.

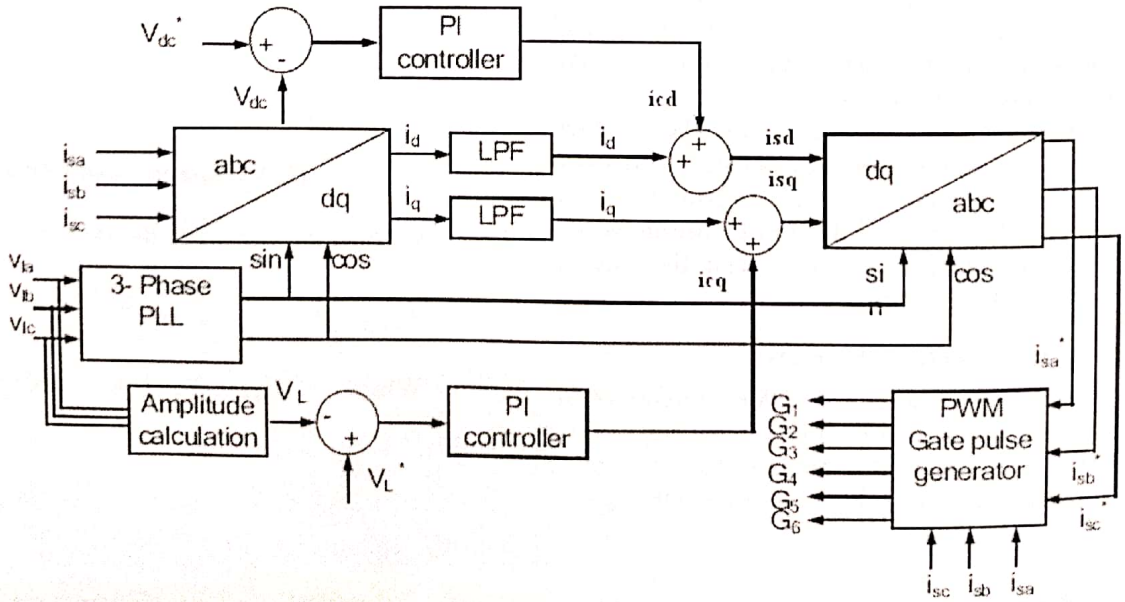

Fig 4: Control scheme of DVR

The load currents in the three phases are converted into the d-q-0 frame using the park's transformation as,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta+\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix} \quad (4)$$

A three phase phase locked loop (PLL) is used to synchronize these signals with the terminal voltages (V_{ta}, V_{tb}, V_{tc}). The d-q components are then passed through low pass filters to extract the transient components of i_d and i_q. The amplitude of the ac voltage at the load (V_L) can be calculated as,

$$V_L = \frac{2}{3}\left(\sqrt{(V_{la})^2 + (V_{lb})^2 + (V_{lc})^2}\right) \quad (5)$$

The amplitude of the load terminal voltage is employed over the reference amplitude and the output of PI controller added with the dc component of i_q. The error between the reference dc capacitor voltage and the sensed dc bus voltage of DVR is given to a PI controller of which output is considered as the loss component of i_d. Similarly a second PI controller is used to regulate the resultant currents which are again converted into the reference supply currents using the reverse Park's transformation. Reference supply currents (i_{sa}*,i_{sb}*,i_{sc}*) and the sensed supply currents (i_{sa}, i_{sc}, i_{sc}) are used in PWM controller to generate gating pulses for the switches.

IV. Modelling and Simulation of Test System

The DVR is modeled and simulated using the MATLAB / Simulink. A pulse width modulation (PWM) controller is used over the error between the reference source currents and the sensed source currents to generate gating signals for the IGBT's of the VSC of DVR. The load considered is a lagging power factor load. The VSC of the DVR is connected to the system using an injection transformer. Also a ripple filter for filtering the switching ripple in the terminal voltage is connected across the terminals of the secondary of the transformer. The simulink model of the test system is shown in Fig.5.

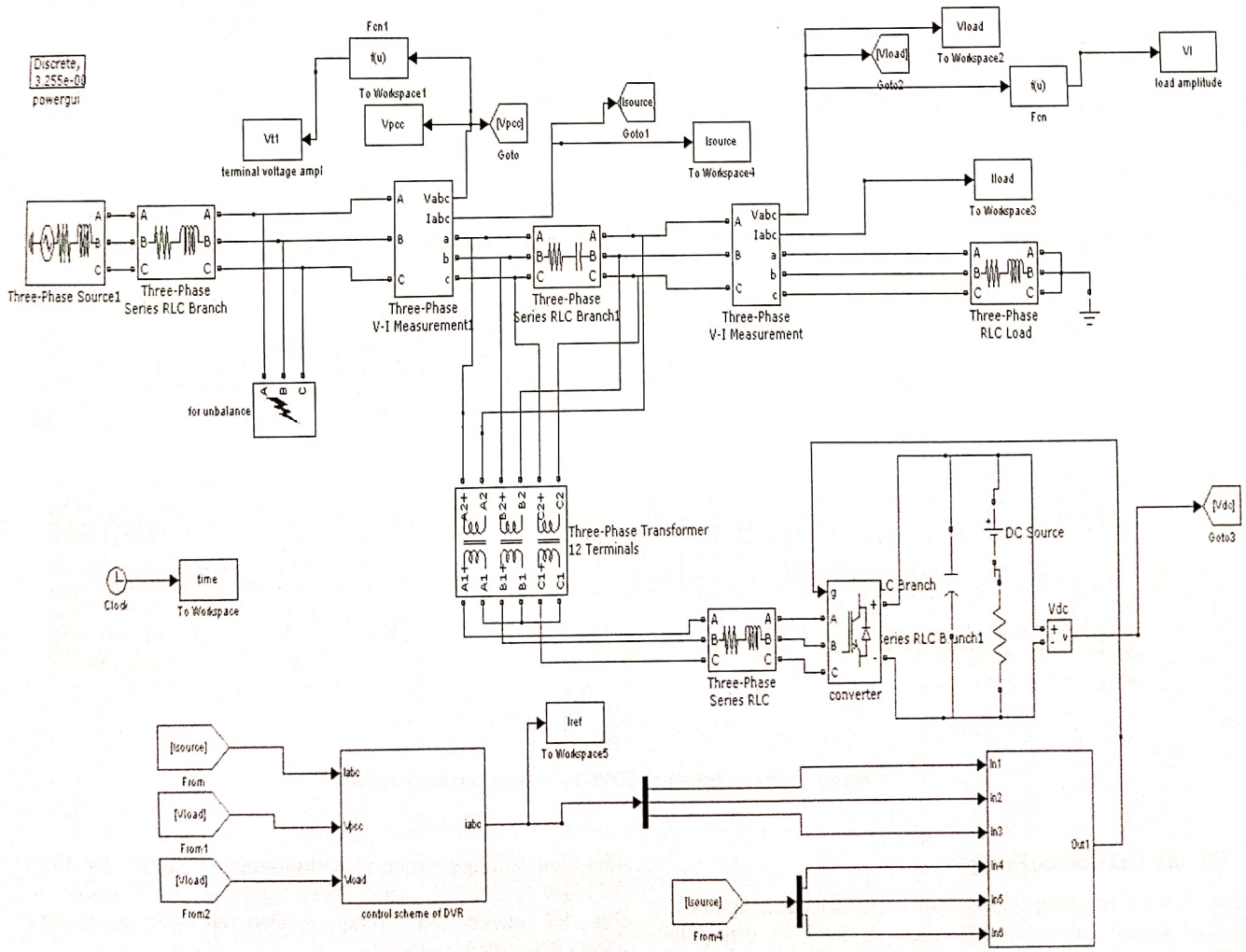

Fig 5: Simulink model of the Test System

V. RESULTS AND DISCUSSION

5.1 Under normal condition

The source voltage (V) under normal conditions is shown in Fig 6.1(a). In Fig 6.1(b) the Load voltage has sag at 0.1 sec and occurs up to 0.2 sec. the DVR injects a voltage in series with the terminal voltage. The load voltage which is maintaining at rated value from 0.1 sec to 0.2 sec after DVR compensation is shown in Fig 6.1(c). The load voltage is observed to be satisfactory for DVR compensation.

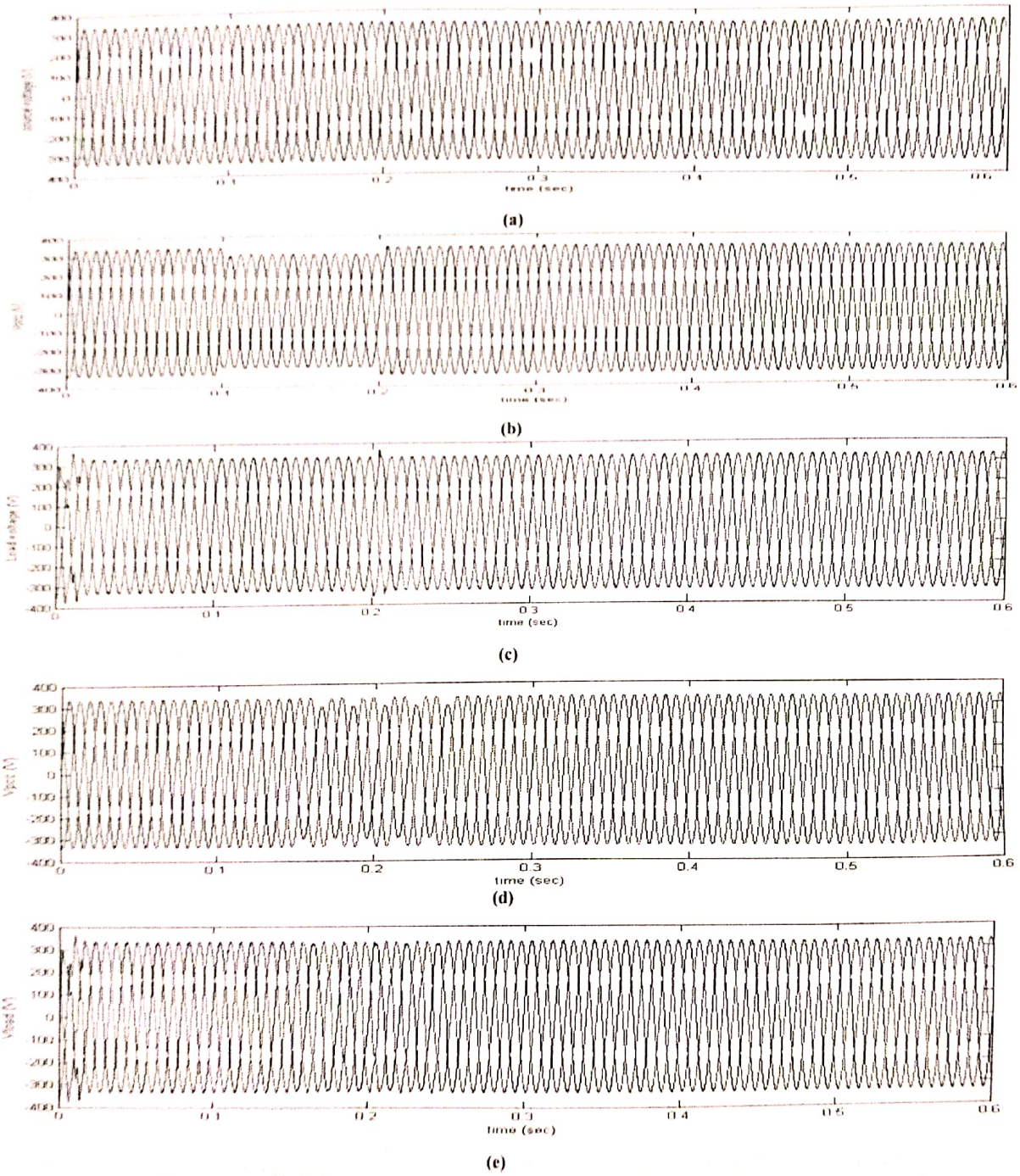

Fig 6.1: Dynamic behavior of DVR for Voltage sag compensation

5.2 During Unbalanced supply

In Fig. 6.1 (d) the load voltage has an unbalanced supply at 0.15 sec and occurs up to 0.25 sec with an L-G fault. The DVR injects a voltage in series with the terminal voltage. The load Voltage which is maintaining at rated value from 0.15 sec to 0.25 sec after DVR compensation is shown in Fig. 6.1 (e). The load voltage is observed to be satisfactory after DVR compensation

V. CONCLUSION

In this project a new control scheme based on synchronous reference frame (SRF) theory has been used for the DVR for three phase three wire distribution system to improve the performance during balanced voltage sag, and unbalanced voltage sag condition. The performance of the DVR has been observed to be satisfactory through simulation using MATLAB SIMULINK (Sim Power Systems tools) software for compensation of voltage sag, and unbalanced voltage sag.

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