Design and Implementation of Energy Efficient SAR Analog to Digital Converter

B. Satish, Prabhu G Benakop

Abstract: ***An energy efficient Successive Approximate Register Analog to Digital Converter (SAR ADC) is designed and implemented to meet the low power sensor applications using split capacitor Digital to Analog Converter (DAC). The split capacitor array DAC reduces the practical value of MSB Capacitor to 50%. The body bias based Dynamic Comparator is proposed for the SAR ADC to improve the linearity of ADC and to reduce the energy. The gate and Transistor level optimization is carried out using mixed logic technique for the reduction of transistors count in the digital SAR control logic block. Due to the split capacitor DAC, body biased comparator and mixed digital logic, the overall area and energy are reduced than the existing SAR ADC architectures.***

Index Terms: ADC, Low Power, dynamic comparator, DAC and Transmission Gate logic (TGL).

I. INTRODUCTION

The major characteristics of Successive Approximation Register (SAR) Analog to Digital Converter(ADC) are simple in architecture, lower power consumption per conversion, high efficiency in performance, occupies small area at chip level, minimum number of active analog blocks, moderate resolution and reconfigurable structure. Due to the above characteristics SAR ADCs are well suitable for Real time applications like distributed sensor networks, wireless sensor networks, biomedical applications, implantable medical devices and wearable health monitoring systems. In recent times, many SAR architectures were published to save energy consumption of Digital to Analog Converter (DAC), which is mostly effecting the overall energy consumption of SAR ADC. In [1], a low power SAR ADC is achieved by using a DAC with DC-DC step down switched capacitor. The capacitor of this nature can be charged during comparison phase of ADC from the reference voltage, so they have no effect while implementing the SAR control logic. In [2], energy efficiency is achieved by avoiding sampling buffers in the signal path from analog input to input to the comparator, otherwise more noise sources were introduced and demands high power in the sample and hold circuit. In [3], a non-linear capacitive DAC using MOS capacitors (MOSCAPs) is used to implement SAR-ADC to reduce the sensitivity against dynamic offset variations and noise. MOSCAPs are highly non-linear, more sensitive to thermal noise and dynamic offset voltages, but they have merits on their side like, they don't require additional steps in fabrication, so fabrication cost is less. They have better matching properties and high capacitor density i.e. a large capacitance can be fabricated in comparatively less area, so DAC area is reduced.

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In all above energy efficient schemes, an intermediate power supply (V_{cm}) is used along with reference voltage (V_{ref}) and ground. A capacitive DAC is implemented with above three voltages leads to more energy consumption. In this work, a constant intermediate voltage, named common mode voltage (V_{cm}) is used, whose value is exactly half of reference voltage (V_{ref}). So the energy consumption of proposed DAC is reduced and also the comparator block is implemented with a dynamic comparator with body bias effect for few MOS transistors to reduce dynamic offset voltage of comparator, which in turn increases effective number of bits (ENOB) and performance of SAR ADC.

The rest of the paper is organized as SAR ADC architecture is described in section II. The operation and implementation of split capacitor DAC of proposed work is presented in section III. Section IV presents the experimental simulation results and comparison with previous works. Conclusion is finally described in section V

II. ARCHITECTURE OF SAR ADC

In this section, the basic architecture of SAR ADC is described and shown in Fig.1. General architecture of SAR ADC has four main blocks namely sample and hold circuit (SAH), digital logic controller (also called SAR control logic), comparator and DAC.

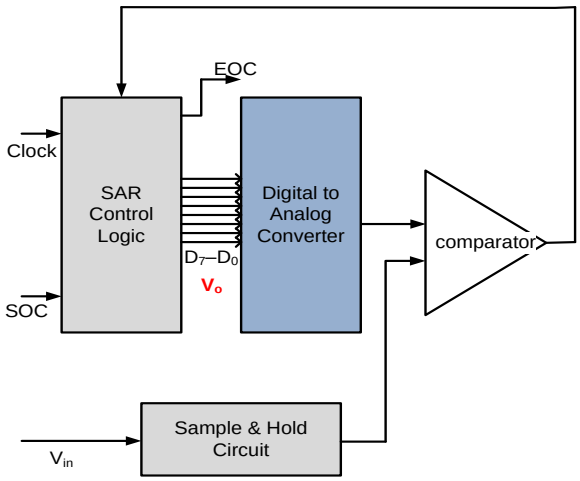

Fig.1 General Architecture of SAR ADC

SAH is used to acquire the sample of analog input voltage to be converted into equivalent digital code. Comparator compares the sampled input voltage i.e. output of SAH with the output of the DAC. The result of comparator is fed to SAR control logic. SAR control logic internally consists of N-bit shift register, whose contents are modifies based on binary search algorithm and the output of the comparator. The contents of SAR shift register becomes valid digital code for the given input after N clock cycles. So the conversion time of N-bit SAR ADC is equal to N clock cycles.

During the conversion time, the contents of SAR shift register are given as input to DAC, which converts it into equivalent analog input. With the help of comparator, this signal is compared with actual analog input voltage sampled and the output of comparator is fed again to SAR control logic, which modifies the contents of the N-bit shift register and the process continues for N clock cycles.

The processing steps of N-bit SAR ADC is as follows: Assume Vin as analog input sample to be converted into equivalent digital code and Vo as the output of the DAC.

1. *Initially reset the N-bit SAR shift register*
2. *Assume K = 1. Set the MSB bit (N – K) of shift register.*
3. *Calculate Vo for the contents of shift register.*
4. *Compare Vo and Vin.*
   a) *If Vo < Vin, then*
      Keep the (N-K) bit as it is
      Go to step 5.
   b) *If Vo > Vin then,*
      Clear the (N-K) bit
      Go to step 5
5. *Increment K by 1.*
6. *Set (N – K) bit*
   Go to step 3 until K = N i.e. LSB bit (N – K) = 0
7. *SAR shift register now contains the valid digital code for the given analog input.*

III. SPLIT CAPACITOR DAC

In a fully differential binary weighted capacitor array DAC, an N bit resolution SAR ADC can be implemented using N-1 bit DAC. In the proposed DAC, a single constant voltage (V_{cm}) is used in implementation, whose value is half of reference voltage (V_{ref}).

The conventional capacitor array is split into two arrays, such as MSB capacitor array and LSB capacitor array [4]. The largest capacitance in each capacitor array is 2^{N-3}C. for an 8 bit SAR ADC, the largest capacitor value is 2^5C.The minimum or unit capacitance C value selected with respect to parameters like noise, precision, fabrication process and mismatch. We can select very minimum Capacitor to reduce the power consumption of the DAC. But a bound on the minimum value is there to achieve good signal to noise ratio.

MSB (2^{N-2}C) capacitor is implemented as a sum of binary weighted capacitors as $C + \sum_{k=3}^{N} 2^{N-K}C$ [5]. The reason behind this is to reduce the total area of capacitors. In binary weighted capacitor array, most significant bits occupy smaller area compared to lower significant bits. So if the large capacitors are split into sum of smaller capacitors, area overhead is reduced and accuracy of ADC is maintained, as the variation in the area of large capacitor doesn't affect the accuracy and performance of ADC. This process reduces the area of total capacitance by a factor of two.

The complete structure of the split array DAC is shown in the Fig.2. The differential inputs V+ and V- are sampled on lowest capacitor value of upper and lower capacitor arrays respectively. Both MSB capacitor arrays are connected to V_{cm}, and the corresponding voltages on inputs of comparator becomesV_{NIN}andV_{IN} as given in the equations (1) and (2).

$$V_{NIN} = \frac{V_{ip}}{2} + \frac{V_{cm}}{2} \quad (1)$$

$$V_{IN} = \frac{V_{in}}{2} + \frac{V_{cm}}{2} \quad (2)$$

Based on the comparator output, MSB digit is decided as shown in equation (3).

$$D_{N-1} = \begin{cases} 0 \;\; if \;\; V_{NIN} \leq V_{IN} \\ 1 \quad\quad otherwise \end{cases} \quad (3)$$

This MSB digit is used to decide the next bit in the switching transition. If D_{N-1} is high, voltage at non inverting terminal V_{NIN} is higher than voltage at inverting terminal V_{IN} so, we need to increase voltage at inverting terminal. This can be done by connecting V_{cm} to highest capacitor of upper LSB array and ground is connected to highest capacitor of lower MSB array.

If D_{N-1} is low, the highest capacitor terminal of lower LSB array is connected to V_{cm} and highest capacitor terminal of Upper MSB array is connected ground. The effective voltages at both the terminals of comparator will become as given in equations (4) and (5)

$$V_{NIN} = \frac{V_+}{2} + \frac{V_{cm}}{2} + (-1)^{D_{N-1}} \frac{V_{cm}}{4} \quad (4)$$

$$V_{IN} = \frac{V_-}{2} + \frac{V_{cm}}{2} - (-1)^{D_{N-1}} \frac{V_{cm}}{4} \quad (5)$$

Based on difference between above voltages D_{N-2} bit is obtained. If $V_{NIN} > V_{IN}$ then D_{N-2} is '1' otherwise '0'. The above process is continued for determination of next bits until D_1 is obtained. To determine the D_0 (LSB bit), the unit capacitor C in MSB array and D_1 are used. If D1 is '0' i.e. when $V_{NIN} < V_{IN}$, the capacitor C in upper MSB array is connected to ground, otherwise the capacitor C in lower MSB is connected to ground.

The total energy consumption of SAR ADC proposed depends on digital code at the output. The energy consumption during each bit determination depends on the previous output of comparator. The total energy is calculated using the equation (6).

$$\sum_{k=2}^{N-1} [2^{N-k-3} - 2^{N-2k-2} - (-1)^{D_{N-k+1}} . x_{k-1}] . CV_{ref}^2 \quad (6)$$

and $x_k = (-1)^{D_{N-k+1}} . 2^{N-k-1} + x_{k-1}$

k = 2,3,4,....(N-1) and $x_1 = 0$

While calculating the total energy consumption of proposed capacitor DAC, energy consumed during reset state and energy consumed by parasitic capacitances were neglected.

The proposed capacitive switching DAC uses only one constant voltage (V_{cm}), whereas other switching schemes built using two voltages V_{cm} and V_{ref} for implementation of capacitor DAC. If both voltages are used, then the mismatch between them results in non-linear operation of DAC, so non-linearity of DAC increases. The linearity of the proposed DAC is improved as it uses only one voltage and it maintains as constant to improve tolerance towards comparator dynamic offset.

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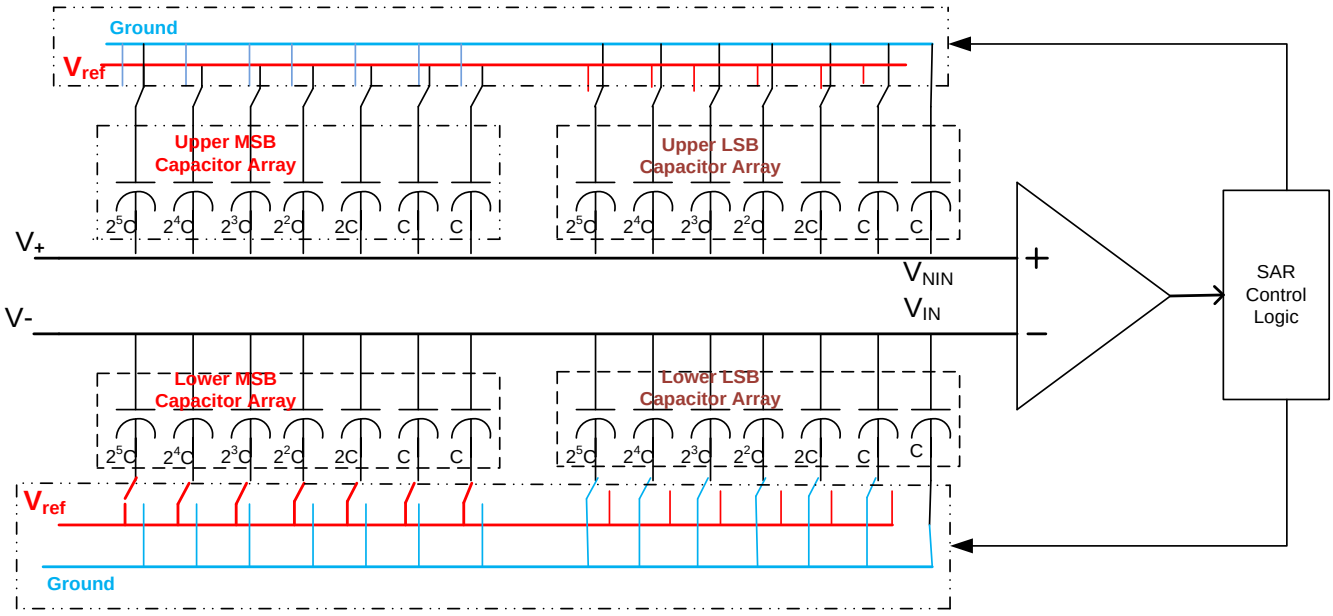

Fig.2 Structure of the split capacitor array DAC.

a) Dynamic Comparator with Body Bias Effect

Body bias dynamic comparator is proposed in this section to reduce the dynamic offset voltage [6]. The transistor level diagram of the comparator is presented in the Fig. 3. It consists of a Preamplifier stage and a Latch. Whenthe clock is high, the A and B nodes are pre-charged to VDD and C and D nodes are pre-charged to GND. When the clock is low, the difference voltage between the nodes C and D is amplified by the preamplifier stage with respect to input voltages. It causes to increase in the common mode voltage atC and D. Next, the transistors of latch stageN5 and N6 will be on and the regeneration starts in the latch stage to produce the outputs V_o^+ and V_o^-. The transistor P_{bias} acts as biased current source, which provides sufficient current for the preamplifier stage to reduce the dynamic offset of the comparator.

In the existing dynamic comparators the body bias technique is not used for the preamplifier and latch stages. In this proposeddynamic comparator, the body biasing is introduced in the preamplifier and latch to prune the charging delay in comparator. The overall operating speed of the comparator is improved using this body bias technique.

The body bias transistors with low threshold voltage are used in the dynamic comparator to reduce the charging delay of preamplifier stage and regeneration delay of latch stage. Total delay is defined as the sum of regeneration and charging delay of input nodes at latch stage (t_1), pre amplifier stage (t_2) and cross coupled inverter stage (t_3) as given in the equation (7)

$$Total\ delay = t_1 + t_2 + t_3 \qquad (7)$$

Where $t_1 = \frac{2C_pV_{tn}}{I_1}$,

$t_2 = \frac{C_pV_{tn}}{I_2}$ and

$$t_3 = \frac{C_p}{g_{m,eff}} \ln\left(\frac{V_{DD}I_2}{4V_{tn}g_{m1,2}\Delta V_{in}}\right)$$

$g_{m,eff}$ is effective trans-conductance of NMOS load transistors and $g_{m1,2}$ is the trans-conductance of differential pair. As V_{th} increases, the proposed dynamic comparator reduces the charging delay of preamplifier stage on linear scale and the regenerative delay of latch stage on exponential scale.

b) SAR Control Logic block

A complex control logic block based on the binary search algorithm is required for the implementation of SAR ADC. The optimized digital logic is implemented in this control block as shown in the Fig. 4. Three different D Flip-Flops are considered for the logic implementation. In order toimplement the Flip-Flops, gate level and transistor level optimization is achieved using mixed logic. Transmission Gate logic (TGL) and CMOS logic are used to realize the gates. The TGL gates reduce the number transistors and switching activity of the each gate. Hence the power and area required for the Flip-Flop and entire SAR control logic block are reduced.

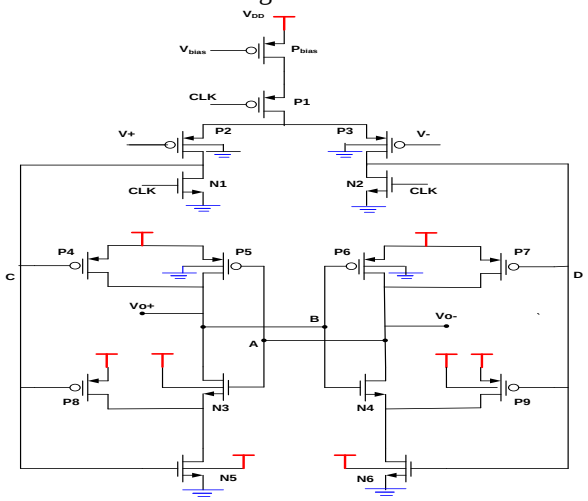

Fig 3. Transistor level diagram of Dynamic Comparator.

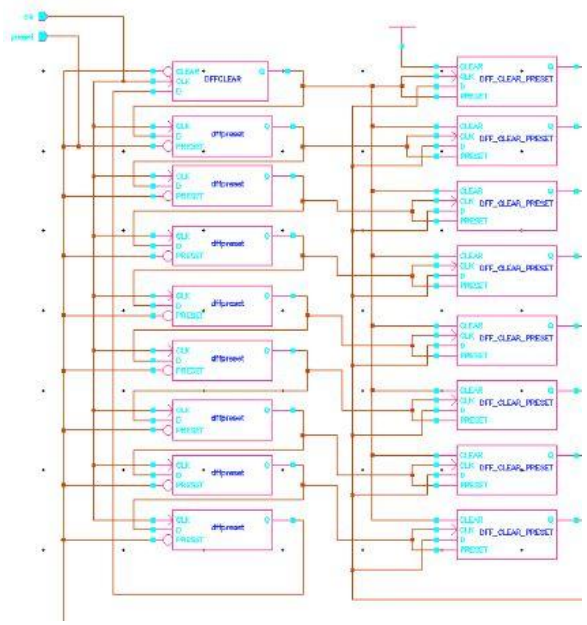

Fig.4 Practical structure of SAR Control Logic

IV. SIMULATION RESULTS

The designed SAR ADC is implemented in CMOS 90nm Generic library using CADENCE tools. The power supply voltage V_{DD} is 0.8 Volts and number of bits are 8. The implemented SAR ADC consumes power of 260nW at sampling frequency of 30 KHz. The Integral Non Linearity (INL), Differential Non Linearity (DNL) and Signal to Noise and Distortion Ratio (SNDR) value are shown in the Table. I.

The power consumption of proposed SAR ADC architecture is 35% less than comparatively [7] and very much less with other existing ADCs with sampling frequency of 30KHz. The INL, DNL and SNDR are improved with effective number of bits 7.41 comparatively state of art methods.

Table. I Comparison of ADC architecture parameters with existing architecture architectures.

	Proposed Architecture	A. Khalid. et al [7]	Jalaja et al [8]	Huang et al [9]	Zou et al [10]	Reyes et al[2]
Sampling Rate (S/s)	30K	10 K	250	-	1 K	3.2 G
Resolution	8	8	10	-		8
ENOB	7.41	7.23	-	-	10.2	6.36
Power Consumption	260 nW	400 nW	0.267 mW	0.328 mW	230 mW	105 mW
DNL	0.20	0.23	0.21	0.29	-	-
INL	0.19	0.46	0.22	0.24	-	-
SNDR (dB)	42.3	47.1	53.2	49.7	-	-

V. CONCLUSIONS

The energy efficient and low area SAR ADC architecture is implemented using split capacitor array DAC and body biased dynamic comparator. The digital SAR control logic is optimized using TGL and CMOS logic gates for the reduction of transistors count and switching activity of the SAR control block. The power and area will be saved due to this mixed logic gate s implementation. The Architecture is implemented in CMOS 90nm technology using generic library at supply voltage of 0.8 volts. The proposed SAR ADC architecture consumes less power and less area comparatively existing ADC architectures.

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