

Design and Implementation of Single PHASERV Topology Five Level Inverter

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Abstract—Multi-level inverter innovation organization need risen as of late similarly as a essential elective in the territory for high-potential high-voltage vitality control. In this way multi-level inverters have been broadly utilized to high-potential high-voltage drive requisitions. Because of higher amount about sources, easier emi, more level % thd for yield voltage Furthermore less anxiety for insulation, they are broadly utilized. However, it need a portion Hindrances Similarly as convoluted pwm controlling method, expanded number of segments Also voltage adjusting issue at impartial purpose. In this paper another topology known as reversing voltage will be actualized will move forward the multi-level execution by compensating those Hindrances only said. This topology obliges fewer parts contrasted with accessible multi-level inverters (especially for higher levels) Also obliges less bearer signs Also doesn't necessity differentiate system for adjusting of the capacitor voltages. Suggested incitement engine drive structure offers diminished gadget count, basic power-bus structure at contrasted with a routine five-level npc Furthermore flying capacitor inverter nourished incitement engine drives. The topology and the control technique In view of spwm would indicated and the needed segments need aid also contrasted with different topologies to demonstrate the prevalence of the topology. At long last reenactment Furthermore test effects looking into distinctive sorts about loads would introduced and talked about.

Index Terms— RV TOPOLGY, SPWM MATLAB 2015 9.0.

I. INTRODUCTION

Multilevel control transformation might have been principal presented more than two decades prior. Those general idea includes using a higher amount for dynamic semiconductor switches to perform those energy transformation over little voltage steps. There need aid a few points of interest should this methodology when compared with those routine energy change approach. The more diminutive voltage steps prompt the generation for higher control personal satisfaction waveforms and likewise diminish voltage (dv/dt) stress on the load and the electromagnetic similarity worries. An alternate essential characteristic about multilevel converters will be that the semiconductors need aid wired over a series-type connection, which permits operation in higher voltages. However, that arrangement association is commonly produced for clamping diodes, which dispenses with overvoltage worries. Furthermore, since those switches would not positively arrangement connected, their exchanging can be staggered, which diminishes the exchanging recurrence

Furthermore In this way those exchanging misfortunes. Person reasonable disservice for multilevel energy transformation is those higher number of semiconductor switches needed. It ought further bolstering be pointed out that easier voltage rated switches could a chance to be utilized within those multilevel converter and, therefore, those animated semiconductor expense may be not appreciably expanded at compared for the two-level instances. However, each dynamic semiconductor included obliges connected entryway drive circuits What's more includes further multifaceted nature of the converter mechanical design.

To late years, there need been a considerable increment in enthusiasm will multilevel energy change. Late investigate need included those presentation about novel converter topologies and interesting regulation methodologies. However, the generally significantly utilized inverter topologies, which need aid primarily tended to Likewise pertinent multilevel inverters, need aid course converter, neutral-point clamped (NPC) inverter[1], What's more flying capacitor inverter..

A percentage provisions for these new converters incorporate modern drives, adaptable ac transmission frameworks (FACTS), What's more vehicle propulsion. One range the place multilevel converters need aid especially suitability is that from claiming renewable photovoltaic vitality that effectiveness and force caliber need aid from claiming extraordinary worries for the analysts[2]. Some new methodologies have been as of late proposed for example, such that those topology using low-switching-frequency high-potential units. Despite the topology need exactly change to decrease yield voltage distortion, the general disservice about this system will be that it need critical low-order present sounds. It is likewise unabated should precisely control those extent from claiming yield voltage because of an embraced pulse width regulation (PWM) system. In the multilevel yield may be created for a multiwinding transformer. However, the configuration what's more manufacturing of a multiwinding transformer need aid was troublesome what's more expensive for high-potential provisions. A novel four-level inverter topology is likewise proposed, Furthermore it is substantial to inverters for indeed number of voltage levels What's more not fit from claiming outputting a zero-voltage state. As a result, those inverter yield period voltage for zero regulation indexes is a bipolar waveform bringing two unique qualities and exhibits secondary rms quality and respectable symphonious vitality moved in those exchanging recurrence. This will be an inconvenience of the suggested inverter, especially when it ought to further bolstering yield low alternately zero voltage on a load.

A. Necessity of power converters

On late years, business need started to interest higher control equipment, which notwithstanding achieves the megawatt level. Regulated ac drives in the megawatt range are typically associated with the medium-voltage system. Today, it will be tricky to interface a single control semiconductor switch straightforwardly to medium voltage grids (2. 3, 3. 3, 4. 16, alternately 6. 9 kV). To these reasons, another crew for multilevel inverters need rose concerning illustration the result for attempting with higher voltage levels. Multilevel inverters incorporate an exhibit of control semiconductors Also capacitor voltage sources, the yield of which produce voltages with stepped waveforms. The substitution of the switches permits s were as of the capacitor voltages, which arrive at secondary voltage during the output, same time those energy semiconductors must withstand best lessened voltages. Fig. 1 reveals to a schematic outline from claiming one period leg for inverters with distinctive numbers of levels, for which the activity of the force semiconductors will be spoke to Eventually Tom's perusing a perfect gas switch with a few positions. A two-level inverter generates a yield voltage with two values (levels) with admiration to those negative terminal of the capacitor [see fig. 1(a)], same time those three-level inverter generates three voltages, et cetera.

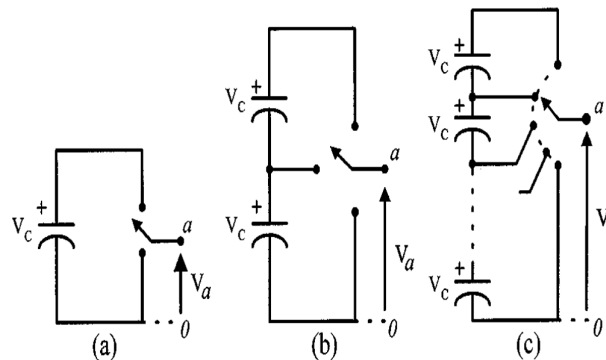


Fig. 1. 1- Phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels[3]

II. NEW MULTI-LEVEL TOPOLOGY

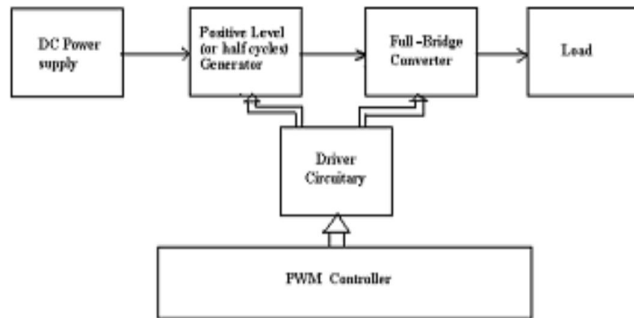


Figure 2.1 block diagram of multi-level inverter using Reversing Voltage topology[4]

Alternate a component will be called polarity era a component Furthermore is answerable for generating the polarity of the yield voltage, which may be the low-frequency piece working In transport recurrence. The topology combines those two parts (high recurrence Also low frequency) with produce the multilevel voltage yield. So as on produce a finish multilevel output, the certain levels are created Eventually Tom's perusing those High-recurrence part (level generation), Furthermore then, this a major aspect is nourished with a full-bridge inverter (polarity generation), which will produce the obliged polarity to the yield. This will dispose of a lot of people of the semiconductor switches which were capable will produce those yield voltage levels to certain Also negative polarities.

The RV topology in seven levels is shown in Fig. 2.2. As can be seen, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 2.2 generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage.[5] This part, which may be named polarity generation, transfers those required yield level of the yield for those same bearing alternately inverse course as stated by those obliged yield polarity. It reverses those voltage bearing the point when those voltage polarity obliges will a chance to be transformed for negative polarity.

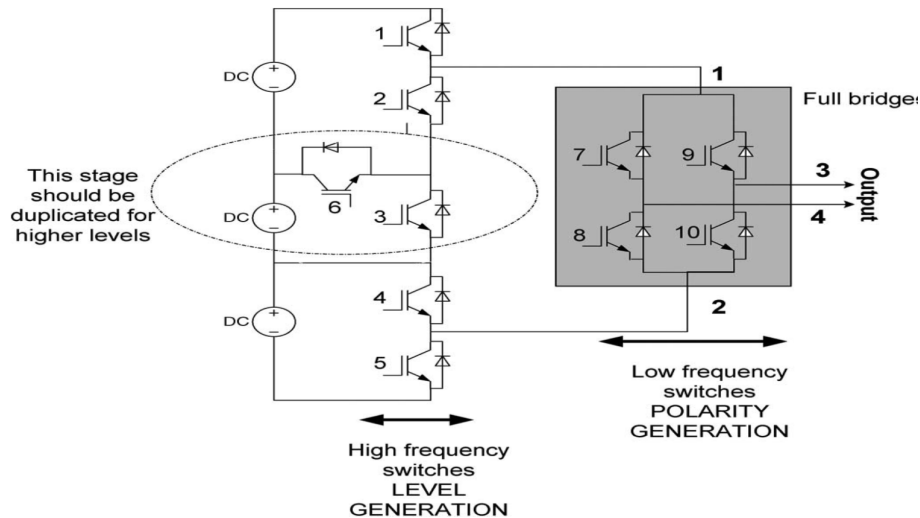


Fig. 2.2. Schematic diagram of a multi-level inverter (single phase).[6]

A. Switching Sequences

Exchanging successions in this converter would simpler over its counter parts. As stated by its intrinsic advantages, it doesn't compelling reason should produce negative pulses to negative cycle control. Thus, there is no require for additional states for controlling those negative voltage. Instead, that reversing full-bridge converter performs this task, and the needed level may be generated by those high-switching-frequency parts from the inverter. Then, this level may be translated on negative or certain as stated by yield

voltage prerequisites. This topology may be excess what's more adaptable in the exchanging arrangement. Diverse exchanging modes over generating the obliged levels for a seven-level RV inverter would demonstrated on table i.

TABLE I. SWITCHING SEQUENCESMODES FOR EACH LEVEL

Level \ Mode	0	1	2	3
1	2,3,4	2,3,5	1,4	1,5
2		2,4,6	2,6,5	

In Table I, the numbers show the switch according to Fig. 2.2 which should be turned on to generate the required voltage level. According to the table, there are six possible switching patterns to control the inverter. It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work [7]. In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation. According to the aforementioned suggestions, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively[8]. These sequences are shown in Fig. 3. As can be observed from Fig. 2.4, the output voltage levels are generated in this part by appropriate switching sequences. The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold.

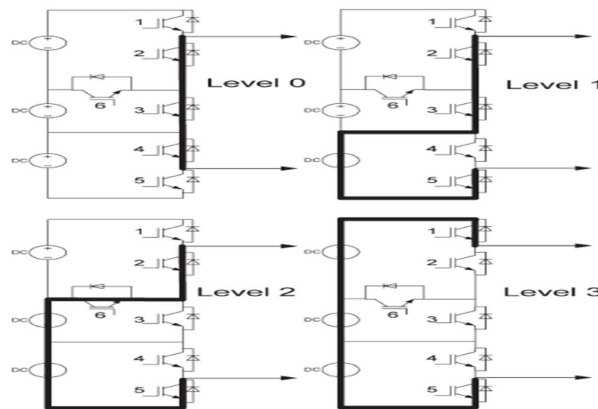


Fig. 2.4. Switching sequences for different level generation

III. PRINCIPLE OPERATION OF 1-@ FIVE-LEVEL INVERTER USING REVERSING VOLTAGE TOPOLOGY[9]

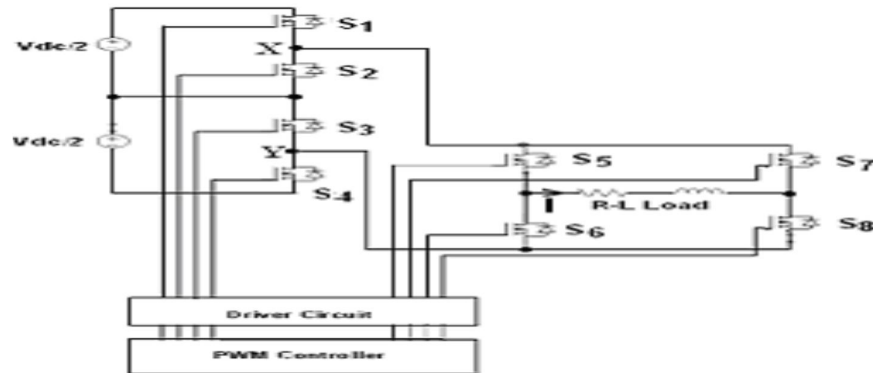


Figure .3.1 Schematic diagram of 1-@ five-level inverter for R-L load

Operation can be easily explained with help of fig. 3.1 and table II the output voltage V_{XY} will be $V_{dc}/2$ when switches S_2 and S_4 are turned “on” as shown in fig.3 (a). When S_1 and S_4 are turned “on” the output voltage V_{XY} is V_{dc} as shown in fig. 3(b). By proper switching combinations of S_1 , S_2 , S_3 and S_4 , the positive half cycles shown in fig.3(c) can be obtained. The voltage blocking capacity of each switch is $V_{dc}/2$. The output line voltage is shown in fig.3.2. Switches S_5 and S_6 are complementary, similarly S_7 and S_8 are also complementary. When S_5 and S_8 are switched “on” together (for duration 10 ms) positive half cycle can be obtained and when S_6 and S_7 switched on together (for duration 10 ms) negative half cycle can be obtained across load as shown in fig.3(d). This topology requires half of the required carriers for PWM controller because it works only in positive polarity and does not generate negative polarities[10].

TABLE II. SWITCHINGSEQUENCE TABLE

Output voltage V_{XY}	S_1	S_2	S_3	S_4
0	0	1	1	0
$V_{dc}/2$	0	1	0	1
V_{dc}	1	0	0	1

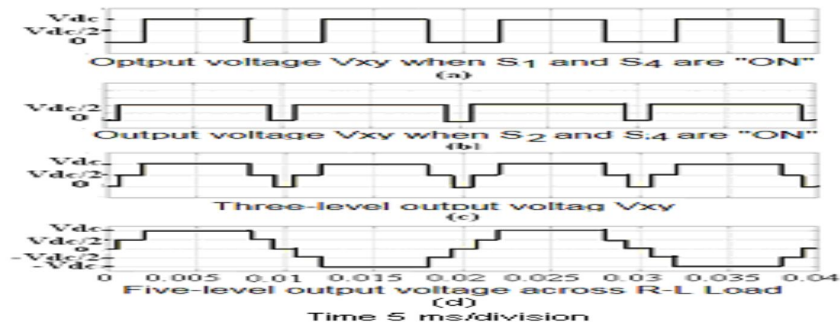


Figure 3.2.1 Output voltage waveforms synthesis (single-phase)

IV. CONCLUSION

Principle and operation of the reversing voltage topology of single phase multilevel inverter is studied. Mat lab-Simulink models of a single phase five level, seven level and nine level inverters with RV topology are developed and output voltage and current waveforms are observed for both R and RL loads. The total harmonic distortion for both R and RL loads are also obtained. The switching pulses are derived based on phase disposition of sinusoidal pulse width modulation[11].

Single phase five level inverter with RV topology hardware is implemented by phase disposition pulse width modulation technique (PD-SPWM) and the output voltage at the resistive load will be shown[12]. Hardware implementation is done with all analog ICs. Power circuit is made with IRF 640 MOSFETs.

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